PC-BASED METHOD FOR THE MEASUREMENT OF INSTRUMENT TRANSFORMER ERRORS

Jagadeesh Kumar V(1), *Sunil C and Sankaran P*(2)
(1) Department of Electrical Engineering, IIT Madras, Chennai 600 036, India.
Phone (44) 445 8380 Fax (44) 235 0509 email: vjk@iitm.ac.in
(2) Faculty of Engineering and Technology, Mutimedia University, Melaka Campus, 75450 Malaysia
Phone 606 252 3529 Fax 606 231 6552email: panchapagesa.sankaran@mmu.edu.my

Abstract – *Instrument transformers, namely, current and voltage transformers, are characterized by their ratio and phase errors. The comparison method of measurement of instrument transformer errors is a convenient one and has been in vogue for several decades. Conventionally, the comparison method is implemented with either an ac potentiometer or an ac bridge. We now propose a personal computer (PC) based implementation of the comparison method that dispenses the use of either an ac potentiometer or an ac bridge. Dispensing the balancing procedure involves explicit measurement and computation, easily implemented with a PC. Test results on a prototype unit establish the feasibility of the proposed technique.*

Keywords - PC-based method – instrument transformers – measurement of ratio and phase errors -sampling technique.

1. INTRODUCTION

Instrument transformers, namely, current or voltage transformers (CTs or VTs), play a vital role in electrical measurements and particularly in power systems. An ideal instrument transformer is expected to transform the primary quantity (current or voltage) to the secondary side with a definite transformation ratio, preserving the phase. However, practical instrument transformers would posses an error in the transformation ratio and also introduce a small phase shift. Hence instrument transformers are characterized based on their ratio and phase errors [1,2].

The determination of the ratio and phase errors of an instrument transformer by comparing the test transformer with a reference transformer is known as the comparison method of testing. Conventionally, the comparison method is implemented employing an ac bridge or an ac potentiometer [3]. Errors are determined therein after balancing the bridge or potentiometer as the case may be. Manual balancing of an ac potentiometer or bridge is a tedious and time-consuming process. Automatic balancing and hence determination of errors with additional analogue or digital electronics had been reported [4-7].

We now propose a method based on sampling technique that avoids the use of either an ac potentiometer or an ac bridge. The proposed method is implemented with a personal computer (PC). Avoiding the use of either an ac potentiometer or an ac bridge can be achieved only with specific measurements and involved computations, both easily accomplished with a PC.

2. THE COMPARISON METHOD

In the comparison method, the errors of a test transformer are determined by comparing it to a standard transformer having the same ratio specification but possessing very low known errors. The comparison method of testing a CT is outlined here. Explanations and relevant expressions for a VT can be easily obtained by simply replacing ‘I’s with ‘V’s everywhere.

The primaries of the standard (reference) CT, CTS and the test CT, CTX are connected in series and energized from a current source. Their secondaries are also connected in series as illustrated in Fig. 1. Here $\underline{I}_{2S}$ is the secondary current of CTS, $\underline{I}_{2X}$ is the secondary current of CTX and the difference current $\underline{I}_D$ is equal to ($\underline{I}_{2X}$ - $\underline{I}_{2S}$). The ratio and phase errors of CTX can be derived as [3]:

$$\text{Ratio error, } F = \left(\frac{I_D \cos\theta}{I_{2S}}\right) \text{ x } 100\% \qquad (1)$$

$$\text{Phase error, } \delta = \tan^{-1}\left(\frac{I_D \sin\theta}{I_{2S}}\right) \text{ x } 3438 \text{ min.} \qquad (2)$$

Conventionally, either an ac bridge or an ac potentiometer is utilized to separate the inphase component ($I_D \cos\theta$) and quadrature component ($I_D \sin\theta$) of I_D with respect to I_{2S}. From these values the errors of the test CT, CTX are determined. The method proposed here obtains the samples of I_{2S} and I_D with the help of a PC based data acquisition

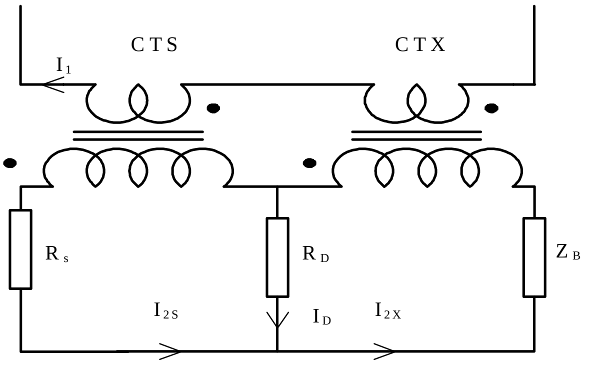


Fig. 1 The Comparison method of testing a CT

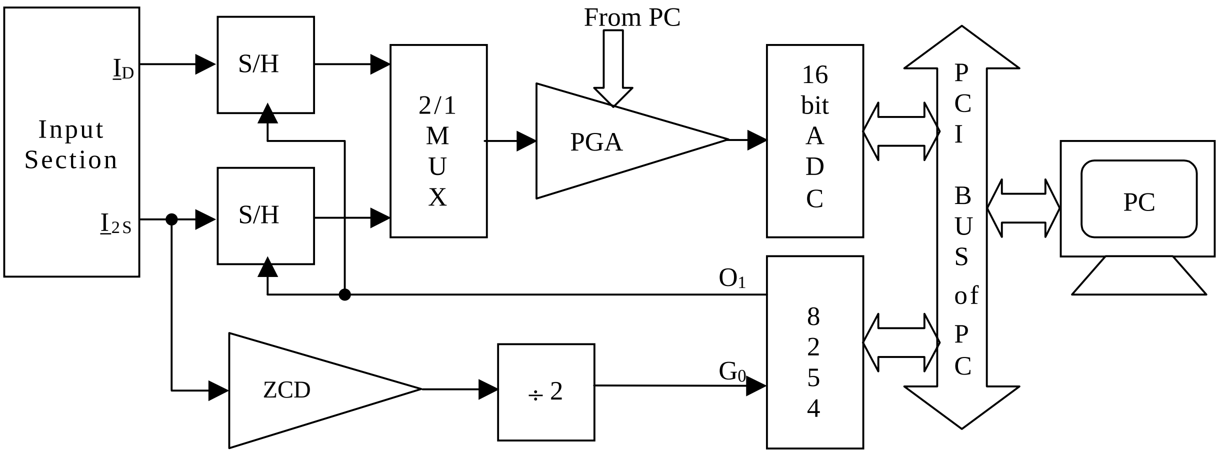
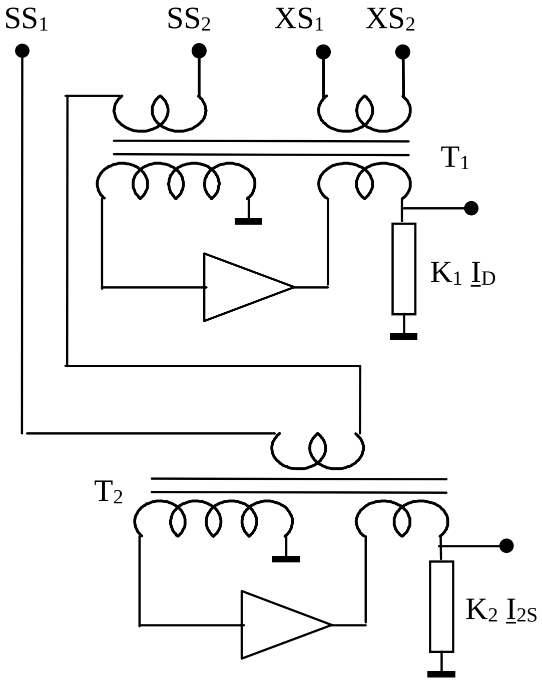


Fig. 2 Block diagram of the PC-based instrument transformer test set

system (DAS) and the errors computed from the digital samples as explained next.

3. THE PC-BASED CT/VT TEST SET

The block diagram of the proposed PC-based instrument transformer test set is given in Fig. 2. As explained earlier, the unit is obtained by cascading a PC-based DAS with suitable input circuitry. The input section for testing a CT is indicated in Fig. 3. The isolating transformers T_2 and T_1 are so arranged that voltages compatible to the DAS and proportional to standard current $\underline{I}_{2S}$ and the difference current $\underline{I}_D$ are available at the outputs. To reduce the errors introduced due to the insertion of the isolation transformers to insignificant levels, “zero flux” compensation is provided employing additional opamps [8]. The primary winding of these isolation transformers are multiple-wound, allowing CTs of different ratios to be tested with the same test set. For example, CTs with a nominal secondary current of 1A can be tested with standard CTs with a 5A nominal secondary and so on.



SS1-SS2 Terminals for connecting reference CT
XS1-XS2 Terminals for connecting reference CT

Fig. 3 Input section for testing a CT

The DAS consists of an ADC cascaded to a (software) programmable gain instrumentation amplifier(PGA). The input to the amplifier is tied to the output of a two-to-one analog multiplexer. The two inputs of the multiplexer are fed from two individual sample-and-hold circuitry. One of the sample and hold circuits is connected to the voltage proportional to $\underline{I}_{2S}$ from the output of the input section and the other connected to the voltage proportional to $\underline{I}_D$. The sample / hold pins of both the sample-and-hold circuitry are tied together to ensure simultaneous sampling of $\underline{I}_{2S}$ and $\underline{I}_D$. Apart from the ADC and PGA, the DAS contains a triple 16-bit counter-timer (8254) interfaced to the PC. The voltage proportional to $\underline{I}_{2S}$ is also fed as input to a zero crossing detector (ZCD). The output of the ZCD is given to a divide-by-two flip-flop and the flip-flop’s output tied to the gate input of counter 0 of the timer counter. A crystal controlled clock is fed to the clock inputs of counter 0 and counter 1. A suitable software controls the hardware, collects N samples of $\underline{I}_{2S}$ and $\underline{I}_d$, performs necessary computations to evaluate the errors of the test CT and displays the errors with suitable annunciation on the screen of the PC. To avoid errors due to sampling jitter and asynchronous sampling, the data acquisition system is configured and controlled to acquire N simultaneous and synchronous samples per cycle of $\underline{I}_{2S}$ and $\underline{I}_D$ by employing the timer-counter 8254 [9]. Let the samples thus obtained of I_{2S} and I_D be denoted as I_{2Sj} and I_{Dj}. With these samples, using integration by summation, (1) and (2) can now be expressed in the digital domain as

$$\text{Ratio Error} \quad F = \frac{\sum_{j=0}^{N-1} I_{2Sj} \; I_{Dj}}{\sum_{j=0}^{N-1} I_{2Sj} \; I_{2Sj}} \quad 100 \quad \% \qquad (3)$$

and

$$\text{Phase error} \quad \delta = \tan^{-1}\left[\frac{\sum_{j=0}^{N-1} I_{2S\left(j+N/4\right)} \, I_{D\,j}}{\sum_{j=0}^{N-1} I_{2Sj} \, I_{2Sj}}\right] \times 3438 \text{ min.} \quad (4)$$

A complete setup based on this principle has been built and tested and found to work well. Testing of VTs is exactly similar but for the change in the input section. In that case, the input section is so configured to provide signals proportional to $\underline{V}_{2S}$ and $\underline{V}_D$ (instead of $\underline{I}_{2S}$ and $\underline{I}_D$ for the case of a CT). The experimental results obtained on a prototype are given in the sequel and the inherent errors of the method are explained next.

4. ERROR ANALYSIS

Since the ratio and phase errors of the test transformer are determined from processing the samples of $\underline{I}_{2S}$ and $\underline{I}_D$, the error in obtaining the samples coupled with the computation determine the worst case errors. If ε_S and ε_D are the measurement errors in the samples of $\underline{I}_{2S}$ and $\underline{I}_D$, then the worst case errors in computing the ratio and phase errors using (3) and (4) can be derived as

$$\varepsilon_F = \frac{\varepsilon_S \sum_{j=1}^{N} \left| I_{2Sj} \, I_{Dj} - 2\,F\,I_{2Sj}^2 \right| + \varepsilon_D \sum_{j=1}^{N} \left| I_{2Sj} \, I_{Dj} \right|}{\varepsilon_S \sum_{j=1}^{N} \left| I_{2Sj} \, I_{Dj} \right|} \quad \text{and}$$

$$\varepsilon_\delta = \frac{\varepsilon_S \sum_{j=1}^{N} \left| I_{2Sj+N/4} \, I_{Dj} - 2\,F\,I_{2Sj+N/4}^2 \right| + \varepsilon_D \sum_{j=1}^{N} \left| I_{2Sj+N/4} \, I_{Dj} \right|}{\varepsilon_S \sum_{j=1}^{N} \left| I_{2Sj+N/4} \, I_{Dj+N/4} \right|},$$

where ε_F and ε_δ are the worst case errors in the ratio and phase errors respectively. Once a particular hardware with its associated accuracy is chosen the worst case errors in the determination of ratio and phase errors can be ascertained.

5. RESULTS AND CONCLUSIONS

A prototype unit was constructed with a data acquisition card (DAS) manufactured by CONTEC inserted into a PC and additional hardware [10]. The ADC employed in the DAS has a resolution of 16-bits and a conversion time of 10 µs. The additional hardware consisted of the input section, the simultaneous sampling section and the sampling frequency generating section. The isolating transformers were made out of Nickel-iron core and zero flux compensation was effected with power opamp µA759. Both transformers were wound with multiple primaries to handle industry standard CTs of 5A and 1A ratings.

The zero crossing detectors were realized with conventional opamps and comparators (LF356 and LM311). A 74LS76 served as the divide-by-two flip-flop. Suitable software was developed in C++ language environment employing the drivers provided by the manufacturer of the DAS card [10]. The software controls the DAS, obtains 512 simultaneous samples per cycle of I_{2Sj} and I_{Dj}, computes ratio and phase errors as per (3) and (4) and displays the results. To ensure that the 512 samples per cycle are equally spaced, within a cycle, the sampling frequency is generated with the timer counter 8254 to be exactly 512 times the input frequency. To achieve this, counter 0 of the 8254 is programmed to be in mode 0 and the width of the pulse T (equal to time period of the input frequency f) at its gate input is obtained. Counter 1 of the 8254 is programmed to operate in the rate generator mode and is loaded with a number T/512. It is easily seen that if the clock frequency given to both counter 0 and counter 1 is the same, then the output of counter 1 would be 512 f, thus providing the synchronous sampling frequency [8].

The principle of operation requires computation of (3) and (4) be performed with samples taken over one full cycle only. However, for the prototype it was observed that evaluating (3) and (4) over several cycles gave better performance in terms of precision. The enhanced performance for larger sample size is mainly due to the fact that the operation involved in (3) and (4) is nothing but obtaining the mean of the product of a set of samples. Hence one can expect a better performance if the set size is large.

Using the developed prototype, tests were then conducted on sample CTs. First known voltages were fed as input to the prototype and the constants in the software were adjusted to compensate for offset and gain deviations and thus the unit was calibrated. After the calibration, the prototype exhibited a full-scale accuracy of 0.1 % on the ratio error and 1 min. on the phase error. The prototype is then employed to measure the errors of sample CTs available in the laboratory. The standard CT employed is Koch and Sterzel, Germany make having a ratio error of 0.005% and phase error of 1 min. The readings of the prototype are compared with those obtained with a conventional ac potentiometer and are given in Table 1.

The results obtained establish the practicality of the proposed method. The method is quite convenient and provides near instantaneous result compared to the potentiometric method. Data gathering, multiple and repeated testing and archiving are quite easily accomplished with the proposed PC based instrument transformer test set.

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Table 1 Experimental results on a 200/5 A, 5 VA Class 1 CT

% I_1	Ratio error F %		Phase error δ, min.	
	Prototype unit	Potentio meter	Prototype unit	Potentio meter
120	- 0.909	- 0.90	34.12	34
100	- 0.901	- 0.90	34.66	35
50	- 1.093	- 1.09	41.00	39
20	- 1.512	- 1.50	44.23	44
5	- 1.769	- 1.77	48.28	47

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