Digital Wireless Data Communication Network for Distributed Measurement Applications: System Architecture and First Experimental Results

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Abstract: *In this paper the architectural design of a measurement system for remote sensing, based on 'ad hoc' Wireless Local Area Network (WLAN) concept is proposed. The system is conceived as a Code Division Multiple Access (CDMA) Spread Spectrum (SS) network operating in the unlicensed Industrial-Scientific-Medical (ISM) frequency band (2.4 GHz to 2.5 GHz). It makes use of a specific and extremely simplified communication protocol, whose characteristics allow simple implementation, without preventing of taking advantage from the processing gain associated with the waveforms. Then the critical hardware element of the system, the modem, is identified and potential applications of the complete system are discussed. The most meaningful aspects strictly related to the modem design are discussed and the hardware solutions are presented. Finally the experimental results descending from the test activity performed on some critical functional blocks of a couple of prototypes under design are discussed.*

Keywords - Distributed measurements, wireless network.

1. INTRODUCTION

Different applications require the measurement process to make use of a relevant number of sensors, spatially separated and distributed over the territory. For example, the numerous devices used in the production processes need to be monitored and maintained to optimize performance and reduce running costs. Moreover, the protection of the environment frequently requires collecting data from sensors distributed in a waste and rugged area [1, 2, 3].

Our basic idea is to build a measurement system on a wide area, by distributing the processing power, creating sensors and actuators with inherent processing capabilities that can communicate between them using numerical, fast and reliable transmissions (smart devices). This measurement architecture allows one to monitor a large plant and to verify the functioning of each single device from a remote location by means of high-level user interfaces [4, 5].

The connectivity of these sensors to the central processing unit of the measurement system becomes a primary problem, especially if a large numbers of long analog wires should be installed in harsh and hazardous environments.

Wireless automation is seen to be one of the fastest growing technological sectors today and in the last years several connectivity problems have found optimal solution through the definition of low-power RF wireless local area networks (WLAN). The application of this network concept to a specific problem of information transport has produced the idea of 'ad hoc' WLAN, where the information protocol and the signal characteristics are particularly matched to the needs of the application itself [6].

In the paper the problems related to WLAN implementation are discussed both from hardware architecture and software protocols points of view.

2. WLAN ARCHITECTURE

The 'ad hoc' WLAN concept represents the natural solution for distributed measurement applications. It provides many benefits, i.e. the significant reduction in number of installations, quick installation, modularity and expandibility.

Decisions related to the definition of the WLAN become critical when referred to the availability of frequency band and to the data transmission reliability. Taking into account the current degree of congestion of the RF frequency bands, it result almost mandatory to implement the unlicensed WLAN in the industrial, scientific and medical (ISM) band, at 2.4 GHz to 2.5 GHz, by adopting compact spectrum RF modulations and short duration communications.

To that order, a Minimum Shift Keying pulsed waveform and a reply-to-request (RTR) communication protocol represent a good response to those requirements. Moreover, the application of Spread Spectrum (SS) techniques to the RF waveforms allows of obtaining a certain degree of transmission reliability with reduced RF power levels [7, 8].

The architecture of proposed WLAN assumes that a master modem (MM) is associated to the measurement-processing unit (MPU) and manages the entire data acquisition. Under control of the MPU, the master modem sequentially interrogates, with addressed requests, all the slave modems (SM) associated to the remote sensors and only one slave modem at the time will provide its data. Association of a different data spreading code to each slave modem performs, in a single step, both the modem addressing and the SS process and a code division multiple access (CDMA) network results [9].

The crucial elements of the WLAN above defined are the MSK-SS radio modem, whose hardware architecture is shown in Fig.1, and the communication protocol, whose

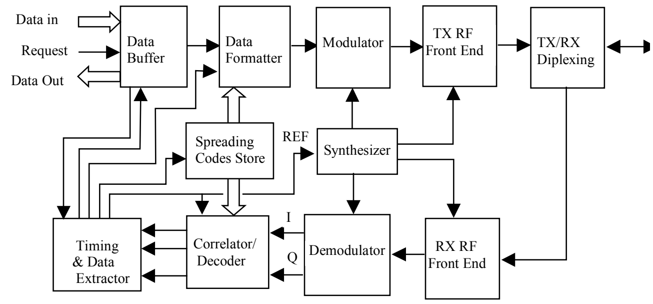


Fig. 1 - MSK-SS radio modem architecture

complexity determines the amount of data processing and development costs that are required.

From our application point of view an extremely simple RF protocol will privilege the link reliability without preventing of postponing to some external processing element (MPU, Personal Computer, or other) the possibility of managing a more complex data communication protocol.

3. SIGNALS AND DATA PROTOCOL

The transmitted waveforms of the radio link are designed for withstanding an information data rate up to 1 Mbit/s. Each elementary transmission has a duration of 64 µs and consists of a burst of 20 equally spaced pulses. Two of them, S1 and S2, define a synchronism preamble. The successive 16 data pulses, P1 to P16, carry out a total of 64 bits. A final pair, S3 and S4, define the end of transmission. Therefore a packet of 4 information data bits is associated to each data pulse.

The complete burst structure is shown in Fig.2.

A continuous data transmission will result in a continuous 50% transmit duty cycle. In addition to the saving of primary power, this limited duty cycle will produce a correspondent reduction in the average energy radiated in the space and, consequently, in the interference produced by the radio link.

From Fig.2 it descends that an effective symbol duration T=1.6 µs is required to satisfy the 1 Mbit/s effective data rate.

The bandwidth (first null) associated to the 1.6 µs baseband symbol is:

$$B_S = \frac{1}{T_S} = \frac{1}{1.6\,\mu s} \cong 0.625\,MHz \qquad (1)$$

Each bit quadruplet is regarded as one element of a 16-

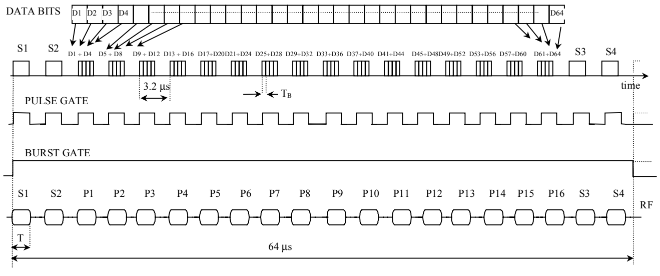
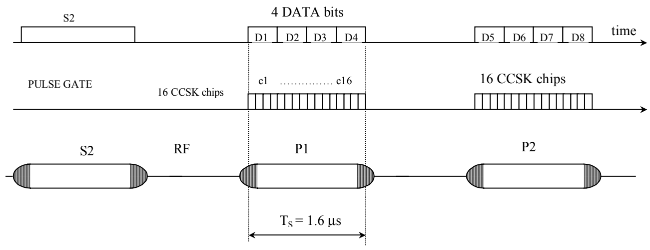


Fig. 2 - Definition of the data burst structure



$D_{i+3}D_{i+2}D_{i+1}D_i$ i=1,5,9,…,60	$c_1\ c_2\ c_3\ c_4\ c_5\ c_6\ c_7\ c_8\ c_9\ c_{10}\ c_{11}\ c_{12}\ c_{13}\ c_{14}\ c_{15}\ c_{16}$
0 0 0 0	$x_0\ x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}$
0 0 0 1	$x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0$
0 0 1 0	$x_2\ x_3\ x_4\ x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1$
0 0 1 1	$x_3\ x_4\ x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2$
0 1 0 0	$x_4\ x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3$
0 1 0 1	$x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4$
0 1 1 0	$x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4\ x_5$
0 1 1 1	$x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4\ x_5\ x_6$
1 0 0 0	$x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7$
1 0 0 1	$x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7\ x_8$
1 0 1 0	$x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7\ x_8\ x_9$
1 0 1 1	$x_{11}\ x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}$
1 1 0 0	$x_{12}\ x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}$
1 1 0 1	$x_{13}\ x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}$
1 1 1 0	$x_{14}\ x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}$
1 1 1 1	$x_{15}\ x_0\ x_1\ x_2\ x_3\ x_4\ x_5\ x_6\ x_7\ x_8\ x_9\ x_{10}\ x_{11}\ x_{12}\ x_{13}\ x_{14}$

Fig. 3 - CCSK encoding of 4 data bits

simbol alphabet and it is mapped into a 16-chip symbol by means of a Cyclic Code Shift Keying (CCSK) encoding. This process is schematically shown in Fig.3.

In order to meet the 1 Mbit/s data rate requirement, the chip duration must be T_c=100 ns, so that the effect of the CCSK encoding is the spectral spreading of the information. The resulting bandwidth (first null) of the chip symbol is:

$$B_{chip} = \frac{1}{T_c} = \frac{1}{100\,ns} = 10\,MHz \qquad (2)$$

Therefore the effect of the CCSK encoding in front of the MSK modulation is that of expanding the bandwidth of the transmitted symbol.

With a fixed bit-error-rate (BER) of the link, the unnecessary complexity added to the system with the CCSK encoding corresponds to the possibility of reducing the transmitted power by an amount equal to the processing gain. A theoretical estimation of it can be done by means of the symbol spectral expansion descending from (1) and (2):

$$PG = 10 \cdot log\left(\frac{T_S}{T_c}\right) = 10 \cdot log(16) = 12dB \qquad (3)$$

In order to take advantage of the available processing gain in (3) the spreading code of the CCSK modulation,

$$[\mathbf{C}]=[c_1\ c_2\ c_3\ c_4\ c_5\ c_6\ c_7\ c_8\ c_9\ c_{10}\ c_{11}\ c_{12}\ c_{13}\ c_{14}\ c_{15}\ c_{16}], \qquad (4)$$

is selected in such a way that the cross-correlation of any pair of sequences in the table of figure 5 results of minimum value. A suitable binary sequence is:

$$[C_D]=[1\ \ 1\ \ 1\ \ 1\ -1\ -1\ -1\ \ 1\ -1\ -1\ -1\ \ 1\ -1\ -1\ \ 1\ -1\ ] \qquad (5)$$

whose (sub-optimal) autocorrelation is shown in Fig.4.

A second choice must be done for the code spreading the double pair of frame pulses S1-S2, S3-S4. Whenever triggered by a Sync pair S1-S2 the SM starts a transaction during which a maximum number of 16 successive pulse are received and up to 64 data bit extracted. The pair S3-S4,

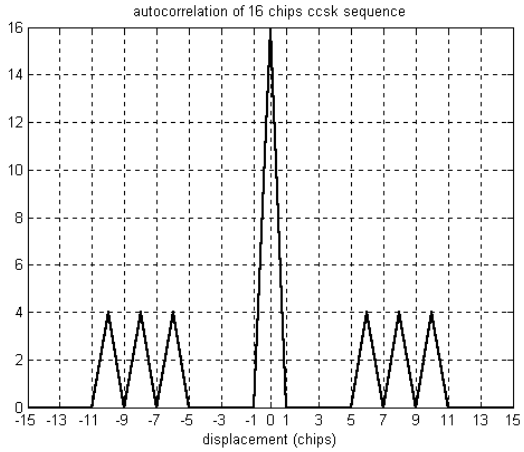


Fig. 4 - Amplitude of the autocorrelation function of sequence [C]

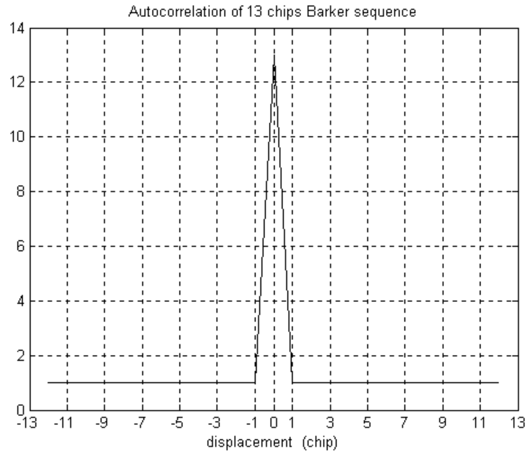


Fig. 5- Optimal autocorrelation function of 13 chip code.

which can occur up to 54.4 μs after the S2 signaling interval, closes the transaction.

If the final frame pair is not received within that interval, the SM automatically provides to complete the transaction in progress.

Because 16-chip sequences have not exactly optimal autocorrelation (Fig.4), 13-chip sequences are selected for spreading the frame pairs. Several sequences having this length offer the optimal autocorrelation like that shown in Fig.5.

A well-known binary sequence of this category is the 13-chip Barker code:

$$[C_S] = [1 \quad 1 \quad 1 \quad 1 \quad 1 \quad -1 \quad -1 \quad 1 \quad 1 \quad -1 \quad 1 \quad -1 \quad 1] \quad (6)$$

The CCSK encoding applied to the selected sequence generates 13 different symbols, B1 to B13, having crosscorrelation of maximum value 1, which allow of defining 169 different pairs when the order of occurrence is taken in account. Half of them are used for spreading the Sync preamble S1-S2, the other half for the final pair S3-S4.

The initial Sync Preamble frame, S1-S2, allows implementing addressed requests from the MM toward one specific SM and addressed answers from one SM toward the MM.

4. THE LINK BUDGET

The essential elements of link budget are shown in Fig.6.

The channel center frequency is:

$$f = 2.45\,GHz \qquad (7)$$

and the free space wavelength:

$$\lambda = \frac{c}{f} = \frac{3 \cdot 10^8}{2.45 \cdot 10^9} = 0.122\,m \qquad (8)$$

The receiver bandwidth is a trade-off between noise power reduction and intersymbol interference.

For a 99% of signal energy:

$$B = \frac{1.2}{T_C} = \frac{1.2}{100 \cdot 10^{-9}} = 12\,MHz \qquad (9)$$

The noise level in the receiver bandwidth is:

$$N = 10 \cdot \log_{10}(k \cdot T \cdot B) = \\ = -174 dBm/Hz + 10 \cdot \log_{10}(B) = -103.2 dBm \qquad (10)$$

For a range D=700 m the propagation losses are:

$$L_{fs} = 20 \cdot log_{10}\left(\frac{4\pi D}{\lambda}\right) = 97.2 dB \qquad (11)$$

With a receiver Noise Figure of 7 dB the resulting noise floor is:

$$N_{RX} = -103.2+7 = -96.2\ dBm \qquad (12)$$

Assuming a bit error rate not exceeding 10^{-6} the required MSK signal to noise ratio is:

$$SNR = 10 \cdot log_{10}\left(\frac{S}{N}\right) = 11 dB \qquad (13)$$

and the corresponding Receiver Sensitivity

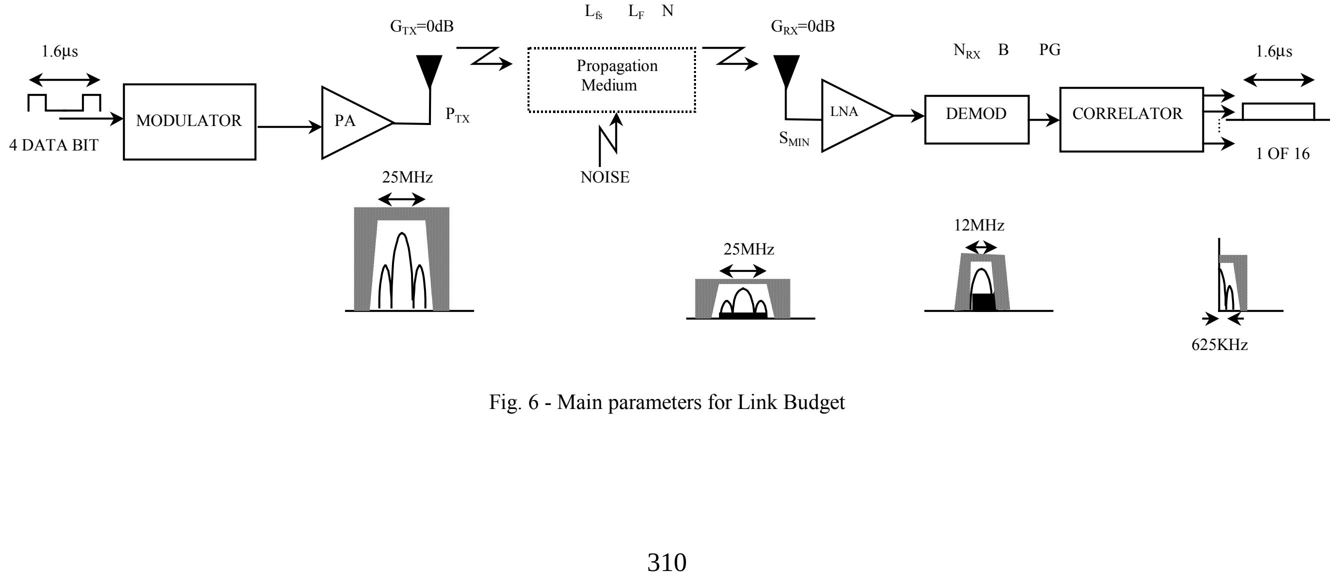


Fig. 6 - Main parameters for Link Budget

$S_{MIN} = N_{RX} + \text{SNR} = -85.2\ dBm$ (14)

With Antenna gains GTX = G_{RX} = 0 dB and Fading losses LF = 20dB the peak power level that the Transmitter must provide is

$P_{TX} = S_{MIN} + L_{fs} - G_{TX} - G_{RX} + L_F - PG = +19.96\ dBm$ (15)

5. CORRELATOR/DECODER STRUCTURE

The architecture of the Correlator/Decoder is shown in Fig.7. The upper blocks are the S1-S2 Sync Preamble

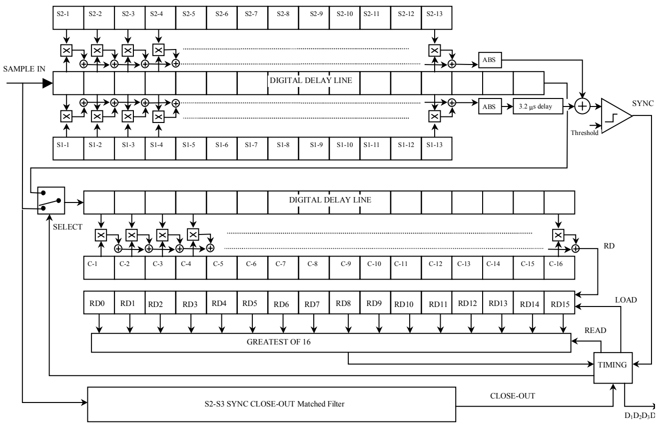


Fig.7 - Correlator/Decoder

matched filters. When a S1 correlation peak is followed by a S2 correlation peak having 3.2 µs delay, the Sync comparator is triggered and the timing block starts a transaction.

During the first half of the 3.2 µs signaling interval both the digital delay lines are loaded with 16 successive samples of the baseband signal. Then the selector block connects the output of the upper delay line to the input of the l delay line.

During the second half of the signaling interval, 16 successive values of correlation, RD0 to RD15, are sequentially loaded into the lowest shift chain. The greatest of the 16 successive correlation samples corresponds to the CCSK symbol and its position in the shift chain defines the quadruplet of information data bit. The operations are schematically shown in Figure 8.

The S2-S3 Close-Out matched filters are similar to the Sync matched filter.

6. RF FRONT ENDS

The operation based on the RTR protocol implies that at any time the radio modem is in one of two possible operation

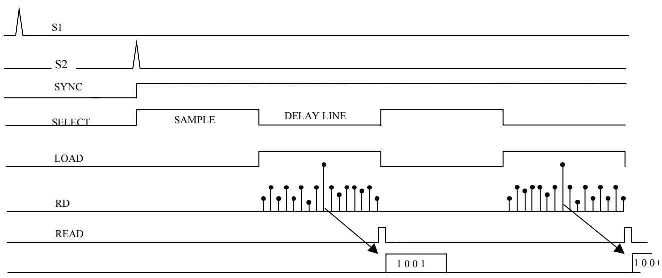


Fig. 8- Correlation process and data decoding

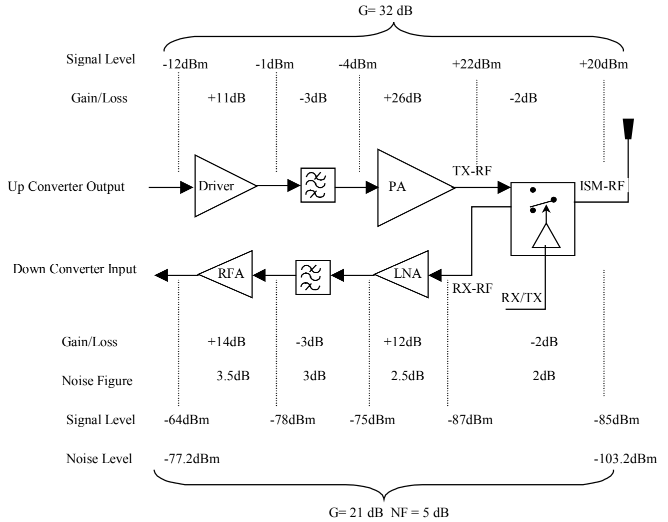


Fig.9 - Receive/Transmit RF Front-Ends

states: in the receive mode or in the transmit mode. This corresponds to a sort of half-duplex operation. The modem is connected to a single antenna and the RF diplexing reduces to a simple switching function.

Figure 9 shows the RF front-end block diagram with the associated characteristics and signal levels.

7. MODULATOR-DEMODULATOR

Both the modulator and the demodulator are based on the I-Q architecture, as shown in Figure 10. The I and Q baseband modulation signals are generated by means of direct digital synthesizers (DDS), in the transmit chain. The I and Q symbols (which nominally are sine half-waves having a relative offset of one chip interval) define the percentage of energy in the spectrum sidelobes. The DDS solution allows to refine the I and Q shaping obtaining a direct control on the transmitted spectrum confinement.

In the receive chain a hard limiting operation at intermediate frequency allows to avoid any automatic gain control.

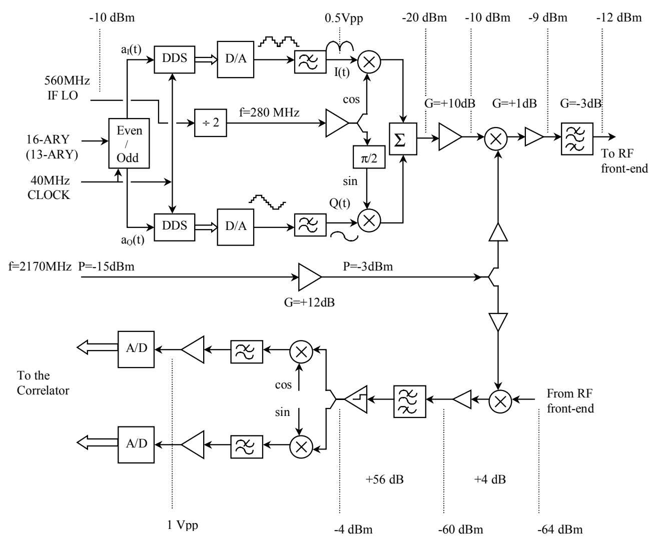


Fig. 10 - Modulation/Demodulation sections

8.HARDWARE DESIGN ASPECTS

The most critical elements of the radio modem are all the RF and IF functional blocks, fom which most of the modem performance descends.

Both the transmit and receive chains are implemented on a low cost substrate microstrip layout. The design of the major active blocks and frequency conversion functions is based on available off-the-shelf monolithic integrated circuits. The ISM band filters, of the coupled line type, are developed separately on a duroid substrate.

The intermediate frequency sections are realized with a combination of monolithic integrated circuits and passive concentrated element.

The timing function, DDS and all other baseband digital processing circuits (matched filters and correlators) are implemented on a pair of 800 Kgates FPGAs.

The Figs.11, 12, 13 and 14 show the results of the preliminary test activity, performed on prototypes of the transmit and receive chains.

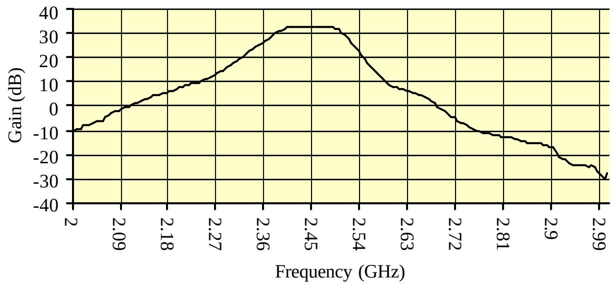


Fig. 11 - Transmit chain power gain vs frequency

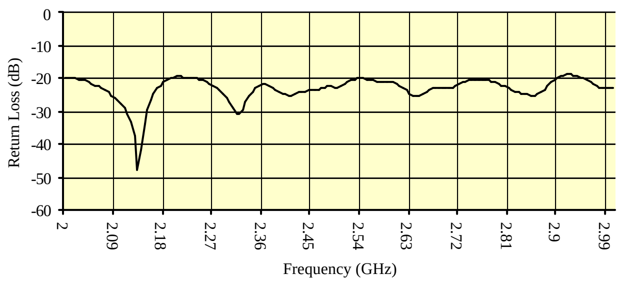


Fig. 12 - Transmit chain input return loss vs frequency

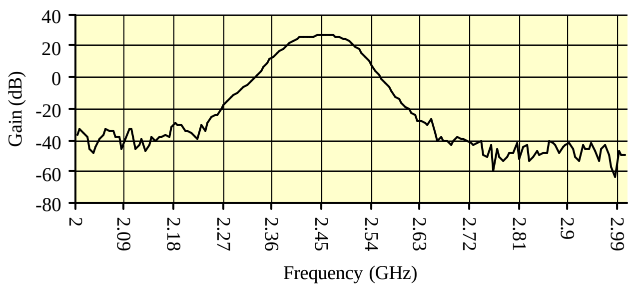


Fig. 13 - Receive chain power gain vs frequency

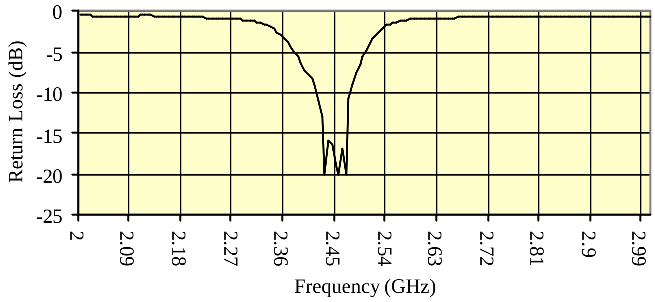


Fig. 14 - Receive chain input return loss vs frequency

CONCLUSIONS

Many applications such as the protection of the environment and the monitoring and control of production processes involve the use of a relevant number of sensors. They should be spatially distributed in a waste area, which frequently can be a harsh environment. These requirements suggest the adoption of a wireless link to transfer measurement information.

In the paper the architectural design of a measurement system for remote sensing, based on 'ad hoc' WLAN has been described. The system is conceived as a Code Division Multiple Access (CDMA) Spread Spectrum (SS) network operating in the Industrial-Scientific-Medical (ISM) frequency band (2.4 GHz to 2.5 GHz). The most meaningful aspects strictly related to the data communication device design are discussed and the hardware solutions are presented. Finally the preliminary experimental results descending from the test activity performed on some critical functional blocks are discussed.

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