EXTENDING DIGITAL INPUT/OUTPUT CAPABILITIES TO LOW-COST AND NON-LINEAR A/D CONVERSION

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Abstract - *A pulse width modulated analogue-to-digital converter (ADC) that provides a low-cost solution for low-speed applications is described. The proposed solution also provides automatic range selection and continuous auto-calibration capabilities. Simulation and experimental results are used to confirm the theoretical expectations of this ADC well adapted to strongly non-linear transducer interfacing.*

Keywords - analogue-to-digital conversion, non-linear ADC, transducers.

1. INTRODUCTION

Applications of measuring transducers requiring their interface to digital systems, namely to processor based systems, have increased in number and diversity. One of the elements widely included in those interfaces to bridge the analogue domain of the sensor to the digital domain of the system, is the ADC. Often the amplitude of the measured quantity changes slowly in time and thus the requirements of the ADC, in what conversion rate is concerned are, very low.

Digital signal processing has made possible the use of low cost but poor performing sensors, in particular, of highly non-linear sensors whose characteristic depends on several influence quantities. Furthermore, the inclusion of a processor for the implementation of processing algorithms allows increased functionally to the sensor (smart sensors).

Some devices, such as microcontrollers and digital signal processors, have the means needed both for A/D conversion and digital signal processing. Nevertheless, the two operations can be and often are separately performed: the analogue output of the transducer is first converted to digital by an ADC and then processed by some processor based system.

Non-linear A/D conversion can be an interesting alternative in particular when linearisation of the transducer characteristic in needed [1][2][3]. The converter reported now is a contribution to non-linear A/D conversion. It is a PWM-ADC designed around a processor and I/O ports usually available in the systems the transducer interfaces with. The architecture of the converter is such that its non-linearity can be easily adjusted, which enables the use of the converter with transducers whose characteristics are non-linear and parameter dependent.

2. SYSTEM DESCRIPTION

Figure 1 represents the basic hardware block diagram of the proposed PWM-ADC [4]. The circuit includes a set of digital input-output ports (DIO), a comparator (Comp.), a low-pass RC filter and an analogue switch (S). Three possible options can be considered for system control and data processing: a personal computer (PC), a microcontroller (μC) or a digital signal processor (DSP). Any of these options can be used in a time-sharing mode with other processing tasks, particularly if conversion speed is not a critical requirement.

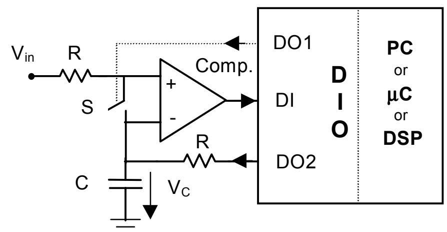


Fig. 1 - Basic hardware block diagram of the PWM-ADC (Comp.- comparator; DI- digital input; DO- digital output; DIO- digital input-output ports; PC- personal computer; μC- microcontroller; DSP- digital signal processor).

The ADC behaves like a closed loop control system. The set-point corresponds to the input voltage (V_{in}), the feedback block is the low-pass RC filter and the error signal obtained at the comparator output is the difference between the set-point and the controlled variable, which corresponds to the average value of the digital stream delivered by digital output (DO2).

Before conversion, switch (S) is closed in order to initialise capacitor voltage (V_C) with the input voltage amplitude (V_{in}) to be converted.

The synchronisation of the feedback loop established by the comparator, the digital input-output ports and filter, assures that the capacitor voltage at the end of the measurement cycle (T_C) is given approximately by [4]:

$$V_C(T_C) = V_{in} + V_{Ch}(T_C) + V_{Dch}(T_C) \qquad (1)$$

with $V_{Ch}(T_C) = n(V_H - V_{C0})(1 - e^{-T_{P1}/RC})$

$$V_{Dch}(T_C) = m(V_L - V_{C0})(1 - e^{-T_{P0}/RC})$$

where n represents the number of high pulses with duration equal to T_{P1} and amplitude equal to V_H, $m=2^B-n$ represents the number of low pulses with duration equal to T_{P0} and amplitude equal to V_L, delivered by DO2 during the conversion cycle (T_C). Conversion result (n) corresponds to the total number of high pulses delivered by the digital output (DO2) during the conversion cycle. The total number of high plus low pulses, delivered by DO2 during the measurement cycle, is always equal to 2^B, where B represents the converter number of bits.

Solving (1) for $V_C(T_C)=V_{C0}=V_{in}$, yields [4]:

$$V_{in} = \frac{nk}{(2^B - n) + nk} V_H + \frac{2^B - n}{(2^B - n) + nk} V_L \qquad (2)$$

where $k = \dfrac{1 - e^{-T_{P1}/RC}}{1 - e^{-T_{P0}/RC}}$ is a non-linear factor modulated by the ratio between positive and negative pulse duration of the PWM signal.

From (2) it is possible to conclude that the conversion range, resolution and linearity can easily be adjusted by software. Conversion range can be adjusted dynamically by software if high and low digital output signals are themselves PWM signals with a variable number of high (V_H) and low (V_L) pulses. Higher resolutions can be obtained by decreasing the conversion range or by increasing the number of pulses used during conversion cycle to estimate input voltage (V_{in}). Obviously, there is, in this case, a compromise between resolution and conversion rate. The non-linear factor (k) can also be easily adjusted by inserting a variable time delay in the software routines that control high and low pulse duration (T_{P1},T_{P0}).

Considering equal values for the duration of high and low pulses ($T_{P0}=T_{P1}=T_P$), the following relation must be verified:

$$T_C > 2^B T_P \qquad (3)$$

Assuming that the pulse time duration (T_P) corresponds to the minimum instruction time value (1 clock period), the maximum conversion rate (R_{max}) is given by:

$$R_{max} < \frac{F_{CLK}}{2^B} \qquad (4)$$

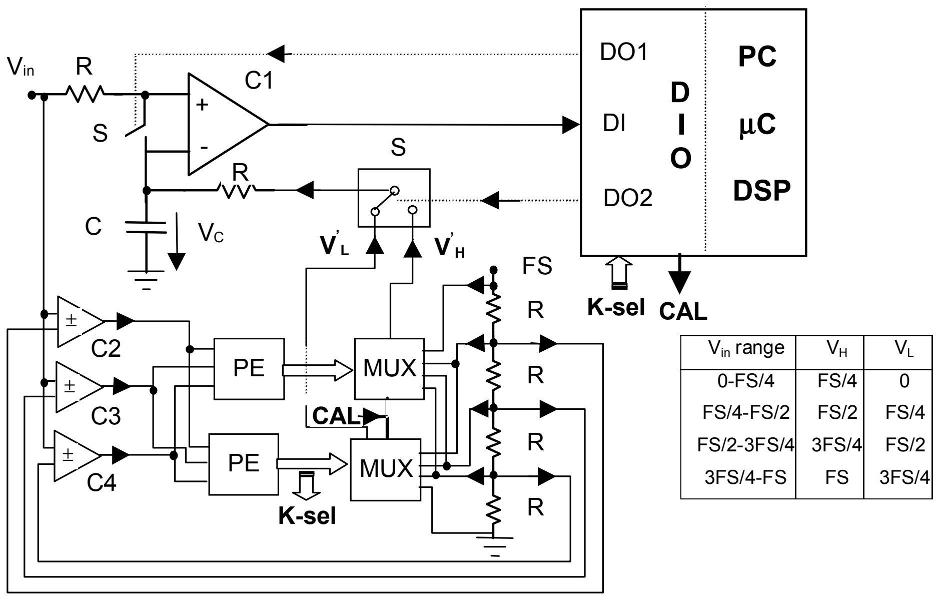
where, as before, B represents the number of bits of the ADC and F_{CLK} the clock frequency of the processor. At the same time, if no sample and hold is used, the signal amplitude variation during T_C must be lower than 1 LSB. This constraint implies that the input signal frequency, and thus converter bandwidth (BW_{ADC}), is upper bounded by:

$$BW_{ADC} < \frac{F_{CLK}}{4^B} \cdot \frac{1}{\pi} \qquad (5)$$

For F_{CLK} = 10 MHz and B = 8, BW_{ADC} < 50 Hz**.**

Finally, it is also important to refer that for very low-speed applications, the basic hardware block diagram of the PWM-ADC can be further simplified. The analogue switch (S) and digital output (DO1) can be removed and replaced by a dummy conversion cycle for initialisation purposes ($V_{CO}=V_{in}$).

The possibility of adjustment of the resolution and linearity factor of this type of ADC is exemplified in Fig. 2. In this case, expression (2) is still valid but for each input range sub-interval a specific set of values for V_L, V_H



Vin range	VH	VL
0-FS/4	FS/4	0
FS/4-FS/2	FS/2	FS/4
FS/2-3FS/4	3FS/4	FS/2
3FS/4-FS	FS	3FS/4

Fig. 2 - Hardware block diagram of the PWM-ADC with non-linear factor adjustment capability for each of four input sub-intervals (C1/2/3/4- four channel quad-comparator, S- analogue switch, DI- digital input, DO- digital output, MUX- multiplexer, PE- priority encoder, DIO- digital input-output ports, CAL-auto-calibration, PC- personal computer, µC- microcontroller, DSP- digital signal processor, FS- full scale.

and k is used. The $V_{H/L}$ voltage amplitudes are automatically selected by hardware and the k factor is selected by software, for each input range sub-interval.

3. RESULTS

A MATLAB simulator and a converter prototype are used in order to study the main characteristics and limitations of the proposed PWM-ADC.

3.1 Simulation Results

The main parameters of the PWM-ADC simulator are: the number of bits (B), the high voltage pulse amplitude (V_H), the low voltage pulse amplitude (V_L), the high pulse duration (T_{P1}), the low pulse duration (T_{P0}), the full-scale amplitude (FS) and the RC time constant. The simulator includes also a conversion time delay parameter and an input signal noise amplitude parameter that can be used to study, respectively, the dynamic behaviour and noise sensitivity of the converter.

As an example of simulation results, Fig. 3 represents the capacitor and digital output voltages, V_C and V_{DO2}, for an input signal amplitude equal to FS/4. The simulation parameters are B=6, V_L=0 V, V_H=1 V, FS=1 V and T_P/RC=1/32. As expected, if a dummy cycle is used before measurement, or if the capacitor voltage is initialised to the input voltage amplitude by closing S switch before starting conversion, the average value of the capacitor voltage is equal to the input voltage and the number of high pulses during 64×Tp is 16.

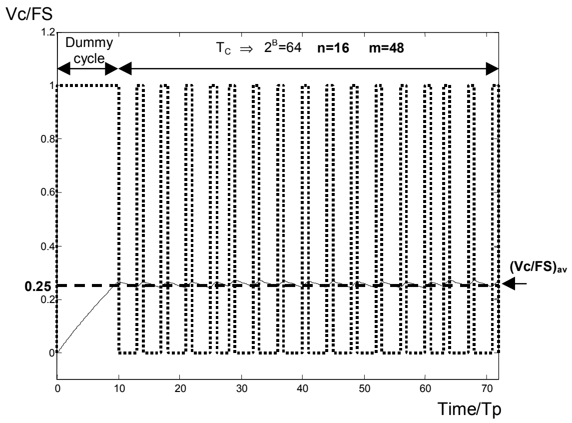


Fig. 3 - Capacitor and digital output voltage (V_C, V_{DO2}) for V_{in}=FS/4. Simulation parameters: B=6, V_L=0 V, V_H=1 V, FS=1 V and T_P/RC=1/32 (continuous line- capacitor voltage; dotted line- digital output voltage; dashed line- average value of capacitor voltage during measurement cycle).

Figure 4 represents the effect of the relative pulse duration (T_P/RC) for a given input voltage (V_{in}=FS/2). The simulation parameters are: B=6, V_L=0 V, V_H=1 V, FS=1 V and T_{P1}=T_{P0}. As expected, low values of the time constant RC generate a higher ripple of capacitor voltage and high values of the time constant makes conversion too slow. The best compromise, obtained by simulation, corresponds to a T_P/RC ratio that is associated with a ripple of the capacitor voltage in the range [1,2] LSB's.

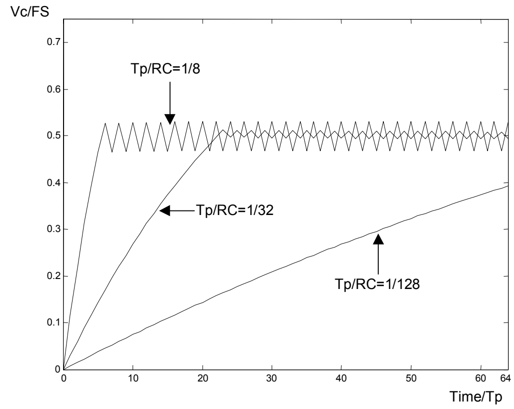


Fig. 4 - Effect of the relative pulse duration (T_P/RC) for a given input voltage (V_{in}=FS/2). Simulation parameters: B=6, V_L=0 V, V_H=1 V, FS=1 V and T_{P1}=T_{P0}=T_P.

Figures 5 and 6 represent the PWM-ADC transfer curve and the total conversion error (E_T), respectively, for 3 different pulse duration ratios, which means 3 different non-linear factors values: T_{P1}/T_{P0}=1/4, T_{P1}/T_{P0}=1 and T_{P1}/T_{P0}=4. The simulation parameters are B=6, V_L=0 V, V_H=1 V, FS=1 V and T_{P1}/RC=1/32.

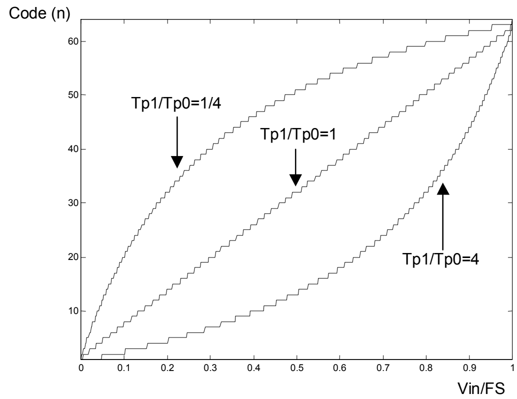


Fig. 5 - PWM-ADC transfer curve for 3 different pulse duration ratios: T_{P1}/T_{P0}=1/4, T_{P1}/T_{P0}=1 and T_{P1}/T_{P0}=4. Simulation parameters: B=6, V_L=0 V, V_H=1 V, FS=1 V and T_{P1}/RC=1/32.

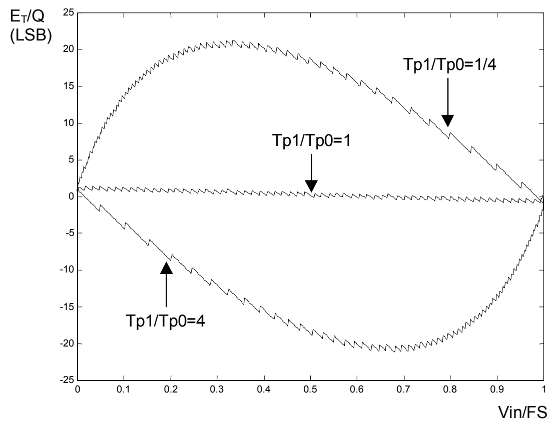


Fig. 6 - PWM-ADC total conversion error for 3 different pulse duration ratios: T_{P1}/T_{P0}=1/4, T_{P1}/T_{P0}=1 and T_{P1}/T_{P0}=4. Simulation parameters: B=6, V_L=0 V, V_H=1 V, FS=1 V and T_{P1}/RC=1/32.

The light slope of the conversion error**,** obtained for $T_{P1}=T_{P0}$, depends on T_P/RC and is caused by non-linear voltage variation of capacitor voltage whose effect is more noticeable near the input voltage limits of the converter range.

3.2 Experimental Results

In order to obtain experimental results, a prototype of the PWM-ADC based on a digital input-output board (PIO12/Keithley) was developed. Figures 7 and 8 represent the transfer curve of the ADC and its differential non-linearity error (DNL) when the converter input voltage varies between 0.40 and 0.82 of FS amplitude. A partial input voltage range of the ADC is considered in order to minimise errors related with the variation of the digital output voltage levels with average capacitor voltage. This present constraint should be overcome by using external buffers or current sources to drive the RC filter.

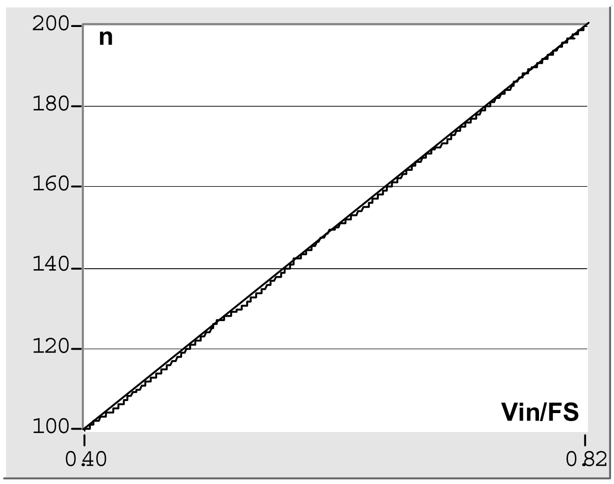


Fig. 7 - PWM-ADC transfer curve for an input voltage variation between 0.40 and 0.82 of FS amplitude.

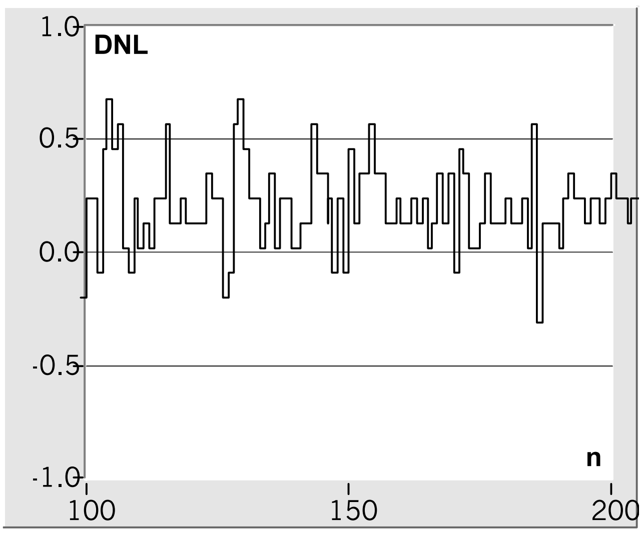


Fig. 8 - PWM-ADC differential non-linearity error for an input voltage variation between 0.40 and 0.82 of FS amplitude.

Figure 9 represents a non-linear characteristic for a T_{P1}/T_{P0} ratio equal to 0.78, which, by coincidence, corresponds to a non-linear factor also equal to 0.78.

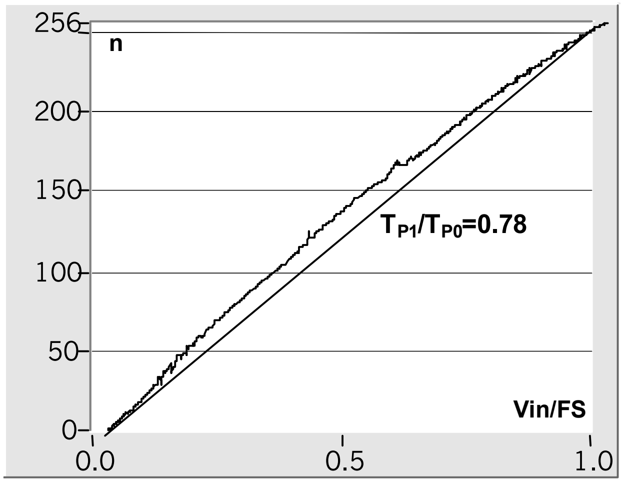


Fig. 9 - PWM-ADC non-linear transfer curve for a non-linear factor k=0.78.

The results obtained with the prototype implemented reveal some design limitations. Two aspects must be improved: (a) reduction of the level of interference produced mainly by the digital part of the circuit and to which the overall circuit is very susceptible, (b) increase current driving capability of digital output port (DO2) by using, if necessary, external buffers. As a result, we expect an increase in the functionality and performance of the converter, in particular of its resolution and accuracy.

4. CONCLUSION

The performance of a PWD-ADC introduced before [4] with adjustable non-linear transfer characteristic, range and resolution was now evaluated by simulation and experimental values of some figures of merit of a prototype were obtained.

While generally agreeing with simulation results, experimental values evidence implementation limitations whose causes are mostly detected. Solutions for some of the limitations are identified, are under implementation and will be reported in the future.

As it is proposed, the converter figures of merit have values quite low: resolution equal to 16.8 mV, effective number of bits equal to 6.7, INL calculated using terminal based definition [5] is equal to 0.8 LSB and a conversion rate lower than 50 samples/s. Nevertheless (a) the possibility of adjustment of both its resolution, range and particularly its transfer characteristic, (b) the hardware and software involved in its implementation, make this converter very attractive for signal conditioning of measuring transducers, a domain that is at the origin of the design and development of the converter and where its application is presently under way [6].

The continuous auto-calibration of the converter is made possible by using two additional measurements of reference voltages, usually ground and FS, whose conversion results can be used to cancel offset and gain errors [4][7]. This capability is a further asset of the converter when a smart sensor is designed.

Apart from the improvements required to increase the converter performance, future work includes the reduction of the number of discrete output components by using a microcontroller-based implementation with internal comparators.

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