AFTER IEEE STD 1241: WHAT'S NEXT?

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Abstract – While the release of IEEE Std 1241-2000 [1] early in 2001 is a major milestone, it is not the end of the ADC standards project. Work continues on improving test methods. A common thrust is to reduce test time (and cost) while maintaining or improving the precision and accuracy of the result. Examples of methods under consideration include a more efficient means of determining offset, equivalent-time testing with imprecise pulses, and automatic sine wave fitting. This paper presents progress to date.

Keywords – ADC, Sinefit, FFT, histogram, step response, equivalent time sampling, IEEE Std 1241-2000, IEEE Std 1057-1994

1. BACKGROUND

Test methods for the recently published IEEE Std 1241-2000, "Standard for terminology and Test Methods for Analog-to-Digital converters" [1] (Std 1241), were frozen over a year ago so that the existing methods could be reviewed and refined for publication. Separately, new methods and improve-ments to existing methods are being developed. The work generally focuses on performing the test in less time, or with less expensive test equipment, or more reliably. This paper presents three new test methods for: 1) deriving offset and gain from histograms; 2) automatically fitting sine waves; and, 3) deriving bandwidth from step response using a common square wave generator.

2. ADC OFFSET AND GAIN ERROR MEASUREMENTS FROM HISTOGRAM

It is highly desirable to make offset and gain measurements in the shortest time possible. For high-speed converters, such as the one presented here, the linearity measurements are made using a sine wave histogram technique. Since this method already measures all differential and integral linearity errors of the ADC while estimating each code transition location, it would be a great time saving to obtain a reasonably accurate estimate of the ADC offset and gain errors from this test method.

The test setup for these histogram offset and gain error measurements is shown in Fig.1 (Std 1241 Fig.3). As a baseline for comparing the measurement uncertainties from this test method, data were taken on the same converter(s) using more traditional DC open loop techniques such as a pseudo binary/linear search and a 2-point static technique. These are similar to the closed loop feedback, transition location detection method described in clause 4.1.6 of Std 1241.

2.1. TEST METHOD 1: PSEUDO BINARY/LINEAR SEARCH

The pseudo binary/linear search method uses a stable DC source as the input to the ADC

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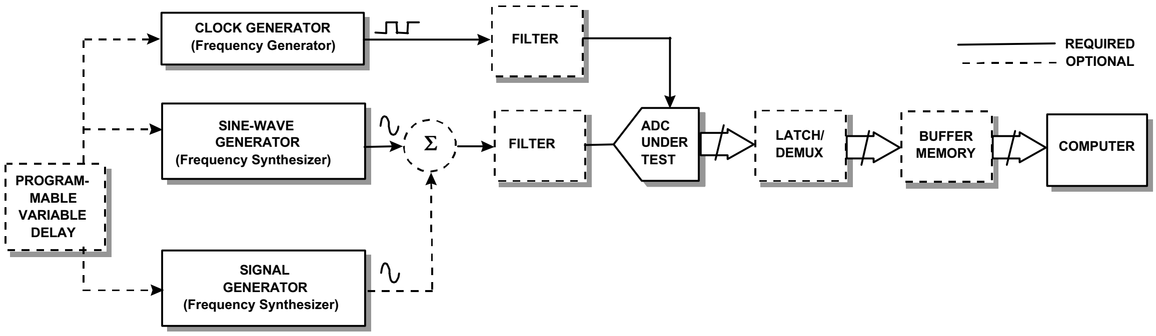

Fig.1 - Test Setup for Sine-Wave Testing

and increases or decreases the input voltage until the transition being sought is crossed and the input voltage is then recorded for each transition location. The binary portion make binary weighted approximations with the DC source to get close to the target transition location and then switches into a fine linear search to settle within some fraction of the least significant bit of the ADC. This data is then used to calculate the offset and gain of the converter using (59) and (60) of Std 1241.

2.2. TEST METHOD 2: TWO-POINT STATIC APPROXIMATION

Although not included in Std 1241, similar methods have been used in industry for many years. The DC open loop static approximation technique simply inputs two calibrated DC voltages (Voltage High & Voltage Low), the lower value slightly above the bottom reference of the ADC and the higher value slightly below the top reference of the ADC. A record of data is taken at each input value and the average output code of the ADC is recorded for each (CodeAvgLow and CodeAvgHigh respectively). Then the Average Step Width (ASW) is calculated per (1).

ASW = Average Code Bin Width = (CodeAvgHigh – CodeAvgLow) / (Voltage High – Voltage Low) (1)

First the 1st transition voltage level T[1] is estimated by multiplying the ASW times the code difference from the 1st transition and the CodeAvg Low and adding the result to the bottom reference level (2). Then the last transition voltage level is calculated by multiplying the ASW times the code difference from the last transition $T[2^N -1]$ and the CodeAvg High measurement and subtracting it from the ADC top reference level (3).

$$T[1] = ASW \cdot (CodeAvgLow - 1) + V_{Bottom}REF \quad (2)$$

where $V_{Bottom}REF$ is the measured bottom reference voltage.

$$T[2^N -1] = V_{Top}REF - ASW \times (2^N -1 - CodeAvgHigh) \quad (3)$$

where N is the resolution of the ADC; and $V_{Top}REF$ is the measured bottom reference voltage.

The offset error is calculated by subtracting the ideal 1st transition from the estimated 1st transition T[1] as shown in (4).

$$\text{Offset error} = T[1] - V_{Bottom}REF – 0.5 * ASW \quad (4)$$

Gain error is then calculated by subtracting the 1st transition voltage from the last transition voltage and comparing it to the specified ideal gain of the ADC which is full-scale range (FSR) – 2 LSB's as shown in (5). The 2 LSB's are subtracted as the two transitions estimated are ½ LSB above negative full-scale Range and 3/2 LSB's below the positive full-scale range of the ADC.

$$\text{Gain error} = V_{Top}REF – T[2^N -1] – 2 \times ASW \quad (5)$$

2.3. TEST METHOD 3: HISTOGRAM METHOD

The histogram test method uses the data taken for the linearity test histogram record(s) and computes the offset and gain error by estimating the T[K] transitions for the ADC using (6) taken from (63) of Std 1241. T[1] the 1st transition, is the offset voltage and $T[2^N -1]$ is the last transition. The last transition minus the 1st is the gain or span of ADC. Once the offset voltage and gain are known their errors can be calculated by using (4) and (5).

$$T[k] = C - A\cos\left[\frac{\pi \cdot H_c[k-1]}{S}\right]$$

for k=1,2,...,(2^N -1) (6)

where A is a gain factor,
C is an offset factor,

$$H_c[j] = \sum_{i=0}^{j} H[i],$$

H[i] = the number of histogram samples received in code bin 1,

$$S = \sum_{i=0}^{2^N-1} H[i] = \text{the total number of histogram samples}$$

If code bins 0 and $2^N - 1$ are excluded (defined as having zero width) then the expressions for C and A reduce to (59) and (60) of Std 1241.

The three methods yield comparable results. However, the additional time required for each method varies dramatically. While the two-point static approximation takes have the time of the pseudo binary/linear search, the sine wave histogram takes almost no additional time.

2.4. RESULTS AND CONCLUSIONS

Table 1 contains the measurements made with each technique on the Texas Instruments 10-bit, 40MS/s ADC model ADS822 and the additional test time required for each method. The pseudo binary/linear search method is used as the reference measurement for comparison.

We have shown that the offset and gain errors can be computed from the sine wave histogram linearity test. The accuracy of these measurements depend on several factors; number of points taken in the histogram, the accuracy of the measurement of the top and bottom reference signals applied to the ADC or output from the ADC, and of course system noise.

By taking the offset and gain results from the necessary linearity and reference tests, we can eliminate the static offset and gain measurement test methods and save some test time per ADC. This equates to a more cost-effective component and across several million ADC's can add up to considerable capital and labor cost savings.

3. AUTOMATIC SINE-FITTING

We have automatic sine fitting software which performs the 4-paraneter (unknown frequency) sine-fit from IEEE Std 1057-1994 and IEEE Std 1241-2000. The software makes its own initial estimate of the frequency. The estimate is derived from a calculation of the power spectrum of the input signal. With this initial estimate the algorithm has never failed to converge to the correct answer. It has been used on many hundreds of actual waveform recorder tests and on scores of test cases designed to stress it.

A LabView implementation of the program is described in [3], which also describes various practical applications of the program outputs. A MATLAB implementation is described in [4] and [5] and is available, free-of-charge, at [6]. The LabView program should be available, also free-of-charge, soon.

The automatic sine-fitting procedure works correctly on data that goes off scale, allowing one to use test signals that overdrive the device under test as discussed in [7]. It also accepts data with non-uniformly spaced time values. The wording of both of the standards includes these extensions, although neither standard specifically mentions them. Testing with sine waves that go slightly off-scale allow one to perform tests that exercise every code bin without being ultra precise with the signal amplitude.

The initial frequency estimate is based on interpolation of the DFT of the signal. The interpolation method used has a maximum error of ±0.05 code bin. It is shown in [8] that an initial estimate error of ± 0.3 code bins is adequate for convergence to the correct frequency.

Once the initial frequency estimate is made the program proceeds as specified for matrix-four-

Table 1 - Comparison of measurement methods for offset and gain error estimates

Measurement	Pseudo binary/linear search method	2-point static approximation	Sine wave histogram method
Offset Error	-14.08	-14.83	-17.39
Gain Error	5.13	0.86	-1.12
Additional Time	178mS	88mS	<1mS (Free)

parameter method in the standards. However, for overdriven signals only the in-range data is used, leaving gaps where the sine wave is clipped. The standards do not specify a precise termination condition for the iterations. The program uses a fixed, six iterations. This has always worked, and other criteria we have tried have all had occasional failures.

Figure 2 shows the modulo-T plot and the integrated power spectrum produced by recording a 419 MHz sine wave with a 2 Gs/S, 8-bit waveform recorder (DC240). The units are counts (LSB's.) This recorder consists of two interleaved ADC's sampling at 1 Gs/S. The modulo-T plot shows random noise, second harmonic distortion, and interleaving error. The interleaving error appears as the separation of the data from the two ADC's. If the interleaving error were about half the size, the separation wouldn't be apparent. In the power spectrum plot the interleaving error occurs at the difference between the interleaving frequency (1 GHz) and the signal frequency. The magnitudes of the three error sources can be read directly from the plot.

3. EQUIVALENT-TIME BANDWIDTH TEST: MIXED SQUARE WAVE

Std 1241 offers two test methods for measuring bandwidth (i.e., the passband of the frequency response between the upper and lower –3dB frequencies). The first method uses sine waves of known frequency amplitude. A sufficiently large group of sine waves at different frequencies is used to map the frequency response to the desired resolution. Since at least one record of data must be taken at each frequency, this method requires substantial test time. Alternatively, frequency response may be derived from the step response (see Std 1241, Section 4.7.3). Resolution is increased by equivalent time sampling (see Std 1241, Section 4.1.3). This method can yield bandwidth from a single record of data in much less test time than the multiple sine wave technique requires.

The quality of the step (or square wave for equivalent time sampling) used for the step response may restrict its use. If the square wave is perfect, the frequency response of the ADC is equal to the Discrete Fourier Transform of the derivative of the step response. Theoretically, this test would allow the frequency response to be measured over a spectrum of any size at once, with one record of data. Unfortunately, an average signal generator, such as the Hewlett Packard 33120A in the lab does not produce clean, high harmonics of the square wave, and as a consequence, that area of the spectrum will not yield accurate results above 100 MHz. By itself, this generator is inadequate for assessing a wide bandwidth (e.g., 200 MHz) ADC.

An alternative method [9] is shown in Fig.3. The conventional square wave is mixed with a sine wave LO to a higher frequency. Varying the sine wave frequency positions the frequency span of the square wave. The square wave response may be centered on the nominal –3dB frequency of the ADC or stepped across its entire frequency response.

Comparative data were obtained from a 10-bit

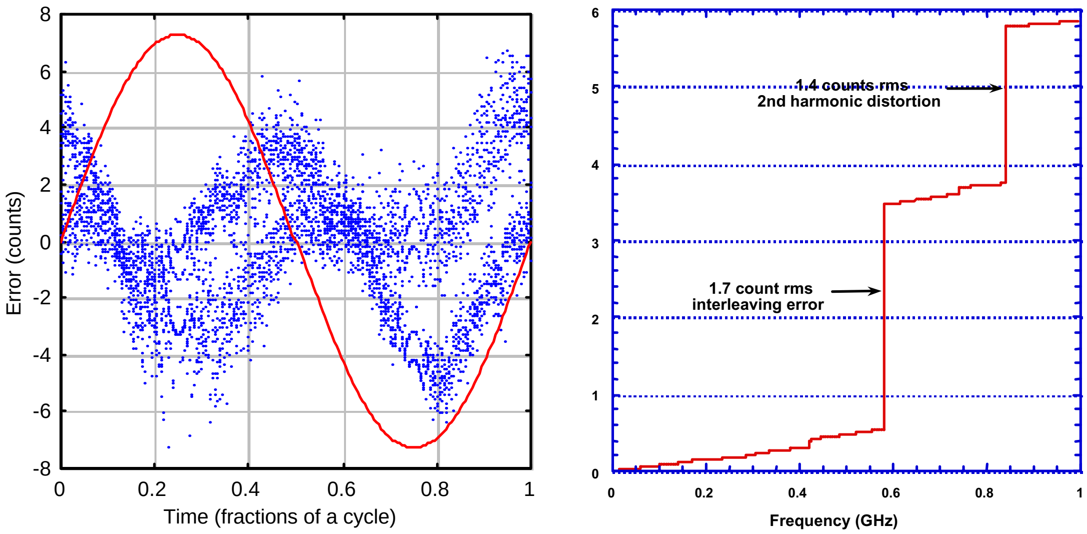

Fig.2. – Modulo Time Plot

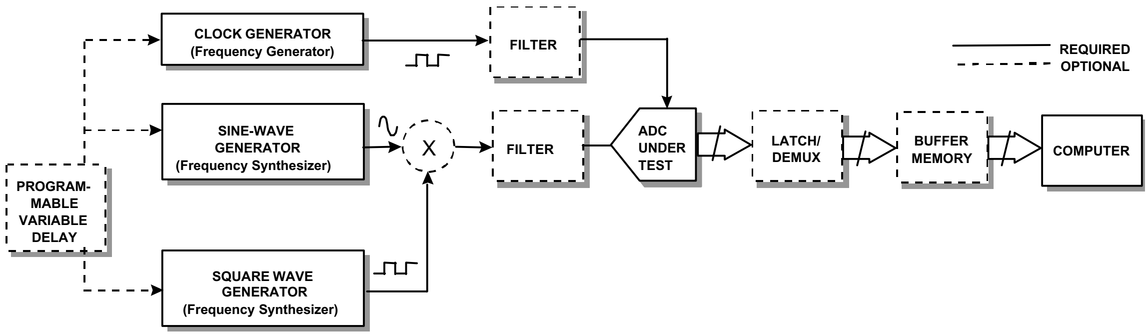

Fig.3 - Test Setup for Mixed Square Wave Testing

ADC (Texas Instruments TLC876C). Fig.4 compares the frequency response obtained with multiple sine waves with the frequency response obtained with the HP 33120A generating the square wave and with the HP 8643A producing the sine wave LO. These frequency responses are quite comparable and suitable for determining bandwidth. While the ADC sampled at 20.48 MHz, the effecting sampling rate was 162.94 GHz. Although not pursued to date, this method appears to be suitable for determining other frequency response parameters identified in Std 1241.

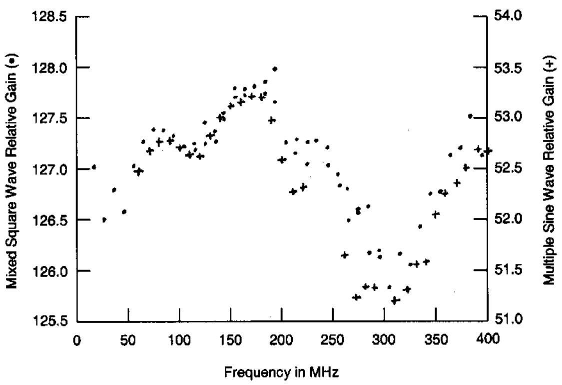

Fig.4 – Frequency Response from Multiple Sine Waves and Mixed Square Waves

5. SUMMARY

The ADC Subcommittee (Steve Tilden, Chair) of the Waveform Measurement and Analysis Committee (TC-10) (Tom Linnenbrink, Chair) continues to seek and develop new and improved techniques to test ADCs. Gain and offset data are derived in insignificant additional time when from a sine wave histogram acquired for other purposes. Sine waves are fit automatically with assured convergence. Wide bandwidth frequency response data is derived from a step response obtained from a common, modest bandwidth square wave generator. We continue to improve upon the test methods published in Std 1241 and welcome new ideas from all sources.

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