# A SURVEY OF TIMING JITTER MEASUREMENT

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**Abstract –** *The purpose of this paper is to provide robust experimental validations of timing jitter measurements and to derive some applications in the field of Analog-to-Digital Converter (ADC) characterisation. The timing jitter measurements are obtained by use of a recently proposed method, which is based on the use of two ADCs driven by the same input and clock signals.*

**Keywords –** A/D Conversion, Timing Jitter, A/D Testing.

## 1. INTRODUCTION

Timing jitter is commonly considered as a limiting factor in sampled systems. As far as the characterisation of ADCs is concerned, its influence has emerged especially with the improvements in both speed and accuracy of today's ADCs as the timing jitter noise gives rise to limitations in devices' performance evaluation. Although several methods have been proposed to measure the jitter contributions which appear in a dynamic test set-up for ADCs, it has only been possible to achieve measurements for the case where the input signal frequency is equal to the sampling frequency, as these methods use a locked histogram configuration [1,2]. Another approach overcame this limitation, but the separation of the different jitter contributions was still not possible [3]. To allow the separation of jitter contributions a method was developed [4] but it was difficult to implement because a carefully designed test board is required. Recently a new approach [5] has given the possibility to separate timing jitter contributions, the one produced by the test set-up and the one produced by the converter. This method satisfies the frequency requirements of dynamic characterisation of ADCs [6] and avoiding complex test developments.

The theoretical aspects of this new method will be reviewed in Section 2, with comments on the main statistical assumptions used in the original paper. In Section 3, some experimental results will be analysed in order to obtain robust validation of the method by comparing the actual results with theoretical models commonly encountered in the literature. Finally, in Section 4, the application of these results in the field of ADCs' characterisation will be demonstrated, by studying the behaviour of the Equivalent Number of Bits (ENOB) of an ADC under timing jitter (produced by the test set-up) influence. A solution for compensation of the test set-up jitter will be proposed.

## 2. REVIEW OF THE MEASUREMENT METHOD

In sine wave testing of ADCs, a sinusoid is uniformly sampled $N_0$ times with a sampling frequency $f_S$ whose value is determined, for an input frequency $f_0$, by

$$f_S = \left(\frac{N_0}{K_0}\right) f_0 , \tag{1}$$

where $N_0$ and $K_0$ are relatively prime numbers [6]. When timing jitter is taken into account, the sine wave is no more sampled using a deterministic scheme. The sampling instants ideally expressed by

$$t(n) = nT_S , \tag{2}$$

where n represents a discrete index describing the set $\{0,1,\ldots,N_0\text{-}1\}$, and $T_S$ the sampling period calculated from (1), should be modified to include errors produced by timing jitter and a suitable representation of the sampling instants is given by [7]

$$t(n) = nT_S + \delta t(n) , \tag{3}$$

where $\delta t(n)$ represents the $n^{th}$ Random Variable (RV) associated with the $n^{th}$ sample. Among the several timing jitter contributions which are encountered in a dynamic test set-up for ADCs, two main categories can be arbitrary found

- Contributions related to the signal sources, basically phase noises of the input and clock signals
- Contributions related to the ADC itself as aperture uncertainties of the sampling circuit, timing uncertainties produced by clock buffers, …

Although these contributions are mainly generated by noises with identical statistical properties, the statistical behaviour of the resulting jitter contributions will differ. For convenience, the statistical properties of these contributions are often assumed stationary in the literature. This assumption can be easily accepted for the jitter contributions related to the ADC, once the 1/f noise is neglected. On the other hand, the signal sources (*i.e.* synthesisers) are complex systems which are mainly based on the use of Phase Locked Loop (PLL) and the stationary assumption may become inadequate if some requirements are not fulfilled. As a complete treatment of this point is out of scope of this paper, the main point to focus on is that the duration of the acquisition (*i.e.* $N_0.T_S$) has to satisfy the relation :

ISBN 972-98115-5-5  

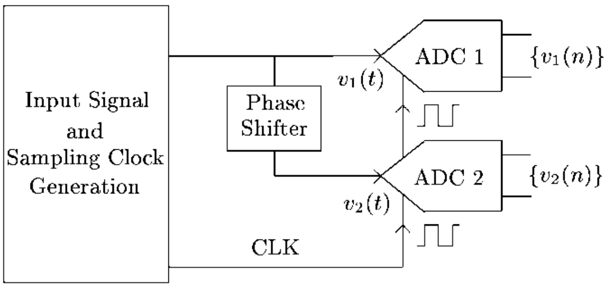


Figure 1: Double Channel Acquisition System [5].

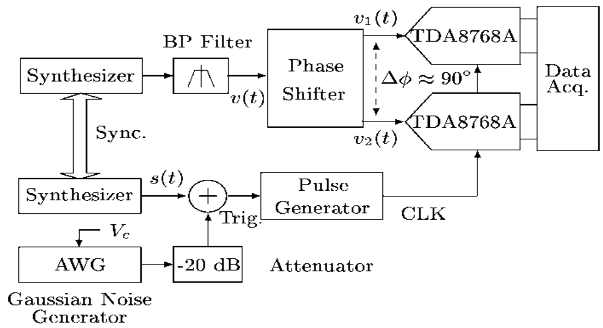


Figure 2 : Block Diagram of the Experimental Set-up [5].

$$N_0 T_S \gg \left(2\pi\omega_{PLL}\right)^{-1}, \quad (4)$$

where $\omega_{PLL}$ represents the band-pass of the PLL used in the synthesisers. Once (4) is satisfied, the stationary assumption of all jitter contributions is acceptable and will not lead to inaccurate results. According to the preceding classification, the random variable $\delta t(n)$ can be written as follows :

$$\delta t(n) = \delta t_{jSYS}(n) + \delta t_{jADC}(n), \quad (5)$$

where $\delta t_{jSYS}(n)$ represents a RV associated with jitter contributions related to the signal generation systems, and $\delta t_{jADC}(n)$ a RV linked to the internal jitter contributions of the ADC. These two contributions are assumed independent with zero means and variances $\sigma_{jSYS}^2$ and $\sigma_{jADC}^2$ respectively. To ensure an entirely random behaviour of the internal jitter we consider that this contribution is essentially generated by the clock buffer of the ADC [5], as for some hi-speed Sample & Hold (S/H) circuits the timing jitter may be causally related to the test signal. In [5] an approach was proposed to achieve an experimental evaluation of the two jitter contributions, the separation is realised thanks to the use of two ADCs driven by the same input and clock signals as depicted in Fig. 1. Using this double acquisition system and frequencies requirements expressed by (1), the nominal sampling phases, $\theta_i(n)$ (i=1,2), for the two channels are given by

$$\theta_i(n) = 2\pi \frac{nK_0}{N_0} + \phi_i, \quad (6)$$

where $\Delta\phi=\theta_2(n)-\theta_1(n)$ represents the phase difference introduced by the phase shifter. The sampled data streams $\{v_i(n)\}$ associated with the two channels are then given by

$$v_i(n) = V_i \cos\left[\theta_i(n) + J_i(n)\right] + b_i(n) + q_i(n) \quad (7)$$

where $V_i$ represents the amplitude of the input signals, $J_i(n)$ a phase uncertainty term produced by jitter contributions, while $b_i(n)$ and $q_i(n)$ are respectively thermal and quantization noises. Thanks to (5), the phase uncertainty terms, $J_i(n)$, are expressed by

$$J_i(n) = \left(2\pi f_0\right)\left[\delta t_{jSYS}(n) + \delta t_{jADC(i)}(n)\right], \quad (8)$$

where $\delta t_{jADC(i)}(n)$ (i=1,2) represents the internal jitter contributions associated with the two converters. Using Taylor series expansion, it can be shown [5] that each channel of the acquisition system is corrupted by an additive noise contribution

$$\varepsilon_i(n) = -\psi_i(n) J_i(n) + b_i(n) + q_i(n), \quad (9)$$

with

$$\psi_i(n) = V_i \sin\left[\theta_i(n)\right]. \quad (10)$$

The variance of the two channel noises, $\varepsilon_i(n)$ (i=1,2), can be obtained considering that the phase uncertainty term, thermal and quantization noise are independent, thus

$$\sigma^2\left[\varepsilon_i(n)\right] = \left(\sigma_0^2 + \sigma_i^2\right)\psi_i^2(n) + \sigma_{b_i}^2 + \frac{q^2}{12}, \quad (11)$$

with

$$\begin{cases} \sigma_0^2 = \left(2\pi f_0\right)^2 \sigma_{jSYS}^2 \\ \sigma_i^2 = \left(2\pi f_0\right)^2 \sigma_{jADC(i)}^2 \end{cases}. \quad (12)$$

The acquisition and the reorganisation of the samples, proposed in [5], allow to obtain an experimental evaluation of the two quantities defined in (12) to which are added a third one related to

$$\sigma^2\left[\varepsilon_2(n) - \varepsilon_1(n)\right] = \sum_{k=0}^{2} \sigma_k^2 \psi_k^2(n) + \sigma_{b_1}^2 + \sigma_{b_2}^2 + \frac{q^2}{6} \quad (13)$$

with

$$\psi_0(n) = V_2 \sin\left[\theta_2(n)\right] - V_1 \sin\left[\theta_1(n)\right]. \quad (14)$$

Hence, a linear least-square algorithm applied to the expressions (11) and (13) allows the estimation of the set of unknowns $\{\sigma_0, \sigma_1, \sigma_2, \sigma_{b1}, \sigma_{b2}\}$, and algebraic manipulations show that an optimal configuration is obtained for a phase shift between the two channels set to $\Delta\phi=\pi/2$ [5].

## 3. EXPERIMENTAL RESULTS

To obtain some experimental validation of the method described in Section 2, it is necessary to adopt a specific methodology as no jitter reference source can be found to validate the estimated values. Thus it was chosen to compare the estimated jitter values with well-known models which can be found in the literature. The main analysis focuses on the variation of the internal jitter of the ADCs while comparing the results of the measurement method with the model developed in [8]. According to theoretical results, the internal

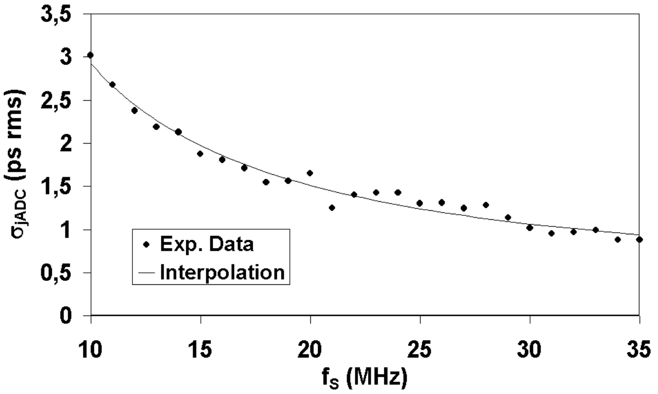


Figure 3 : ADC jitter measures as a function of sample frequency.

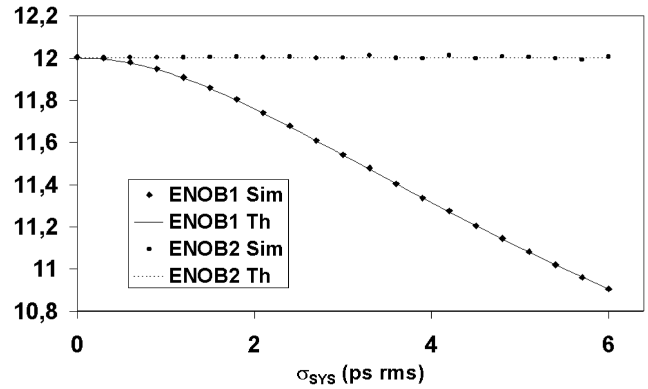


Figure 4 : Theoretical ENOB as a function of the test set-up jitter.

jitter of the clock buffer can be varied by means of the slope of the signal which is applied to its input. Ideally, when a sine wave is used as input signal, the timing jitter produced by a Clock Interface (CI) of an ADC is given, assuming equal values for the input DC value and threshold voltage of the CI, by

$$\sigma_{jADC}^2 = \frac{\sigma_n^2}{\left(2\pi V_S f_S\right)^2} + \sigma_{jB}^2 , \qquad (15)$$

where $\sigma_n^2$ represents the variance of the equivalent input noise of the CI, $V_S$ and $f_S$ are respectively the amplitude and the frequency of the signal applied to the input of the CI, and finally $\sigma_{jB}^2$ is a jitter contribution internally generated due to slew rate and thus independent of the clock signal frequency. To obtain an experimental evaluation of (15), the general test set-up given in Fig. 2 was slightly simplified as the measurements do not require the pulse generator and the Arbitrary Waveform Generator (AWG) originally inserted in the clock signal path. The measures were made using an actual 12 bit 70 MSPS ADC (Philips TDA8768A) with $f_0$=20 MHz, the estimated values of the internal jitter contribution associated with one converter, among the two which are used in the test set-up, are depicted in Fig. 3. The model, defined by (15), has been used to extrapolate the values of the contribution, $\sigma_{jB}$, for the two ADCs and leads to $\sigma_{jB}$=641 fs and $\sigma_{jB}$=960 fs. These values agree with the ones found in [5] when the pulse generator is used, as the slope of the associated signal is much larger than the one which is generated by a sine wave, and thus in this case the estimated value is nothing less than the extrapolated value $\sigma_{jB}$.

## 4. APPLICATION OF THE TIMING JITTER MEASUREMENTS

Among the several parameters used in the field of ADCs characterisation, the ENOB acts as a global indicator which takes into account all the defaults (thermal and quantization noises, distortion, …) associated with the converter. The interpretation and the evaluation of this parameter are inherently associated with the existence of a reference model describing the ideal behaviour of ADCs. A commonly accepted model is the one composed of an ideal S/H circuit followed by an ideal quantifier. Once an experimental evaluation of the Signal-to-Noise-And-Distortion (SINAD) ratio of an actual converter has been obtained, well-known calculations based on the preceding model give rise to the expression

$$ENOB_1 = \frac{SINAD - 10\log_{10}(3/2)}{20\log_{10}(2)} , \qquad (16)$$

where the value of SINAD is expressed in dB. It is also well known that the value, which is obtained by means of (16), represents the virtual number of bits that an ideal converter should have to match the SINAD characteristics of the actual ADC.

As the timing jitter generated by the signal sources are not included in the reference model, the induced defaults (*i.e.* induced noise contribution) will be implicitly set to the account of the ADC under test and will degrade the apparent performances. This point is illustrated considering that the ENOB of an ideal $N_B$ bits converter that can be evaluated from a hypothetical set-up with "jittered" signal sources is lower than $N_B$. As an example, a representation of the $ENOB_1$ of an ideal 12 bits converter as a function of the timing jitter is given in Fig. 4, where the discrete set of values has been obtained by means of simulation. To quantify the influence of this jitter contribution, the $SINAD_{S\&H}$ value associated with an ideal sampling circuit whose signal sources are perturbed by timing jitter with standard deviation, $\sigma_{jSYS}$, has to be calculated and is shown to be given for an input signal frequency, $f_0$, by the relation

$$SINAD_{S\&H} = 10\log_{10}\left(\frac{Q^2}{1-Q^2}\right) \qquad (17)$$

where $Q^2$ is defined by [7]

$$\log\left(Q^2\right) = -\left(2\pi f_0 \sigma_{jSYS}\right)^2 . \qquad (18)$$

As a consequence the $SINAD_{ADC}$ of an ideal converter with "jittered" signal sources is obtained by adding the quantization noise variance, $\sigma_Q^2$, to the denominator of (17), and leads to the relation

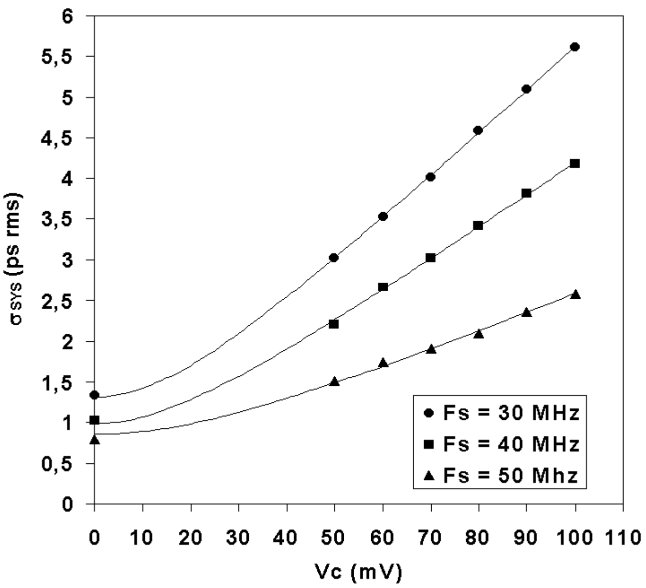


Figure 5 : Test set-up jitter, $\sigma_{SYS}$, as a function of the added noise.

$$SINAD_{ADC} = 10\log_{10}\left(\frac{\left(V_0^2/2\right)Q^2}{\left(V_0^2/2\right)\left(1-Q^2\right)+\sigma_Q^2}\right), \quad (19)$$

where $V_0$ represents the amplitude of the input signal. The use of (16) and (19) permits to obtain an accurate description of the $ENOB_1$ behaviour, as there is a good agreement between the simulated and predicted values as shown in Fig 4. Once the ideal value of $SINAD_{ADC}$ has been calculated, the ENOB parameter can be redefined in order to take into account the jitter influence of the signal sources. Assuming full-scale amplitude for the input signal and quantization noise variance set to $\sigma_Q^2=q^2/12$, the ENOB becomes

$$ENOB_2 = \frac{1}{2}\log_2\left(\frac{2}{3}\frac{SINAD}{Q^2-\left(1-Q^2\right)SINAD}\right). \quad (20)$$

An example of the modified definition $ENOB_2$, as a function of the test set-up jitter, is given in Fig. 4 for a simulated 12 bits ideal converter. The simulated and predicted values show good agreement as in the case of $ENOB_1$, and the results match the behaviour which should be the one of an ideal converter. Thus, once an evaluation of the test set-up jitter has been obtained, it is then possible to compensate its influence by using (20) in order to estimate the “true” performance of the actual converter. An experimental validation of the preceding calculations is found using the set-up described in [5] as depicted in Fig. 2, where the noise generator permits to vary the test set-up jitter by adding some arbitrary jitter to the intrinsic contribution. The measures of the test set-up jitter as a function of the command voltage of the AWG are shown in Fig. 5 for several sampling frequencies. As the variance of output noise of the AWG is given by

$$\sigma_n^2 = \alpha V_C^2 + \sigma_{n0}^2, \quad (21)$$

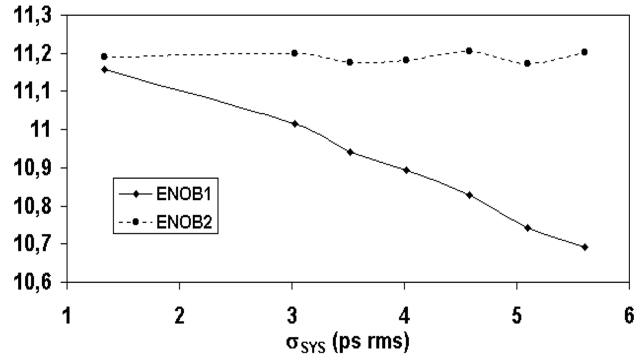


Figure 6 : Experimental ENOB as a function of the test set-up jitter.

where $\alpha$ represents a conversion factor and $\sigma_{n0}^2$ the variance of the intrinsic noise of the AWG. The use of (15) and (21) give rise to the interpolated curves depicted in Fig. 5 which seem to acceptably fit the experimental data[1]. The experimental results of the $ENOB_1$ and $ENOB_2$ evaluations are shown in Fig. 6 for an actual 12 bit 70 MSPS ADC (Philips TDA 8768A), these results confirm that it is possible to deduce the actual value of the parameter while the standard definition clearly under-estimates the performances.

## 5. CONCLUSION

Some experimental results have been added to those found in [5], and confirm the robustness of the recently developed method. Its application in the field of ADCs’ characterisation permits to investigate the behaviour of some performance indicators under jitter influence and propose solutions for compensation.

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