A METHOD FOR REDUCING BOTH STATIC AND DYNAMIC LINEARITY ERRORS IN A DIGITAL TO ANALOGUE CONVERTER

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Abstract - *Conventional methods for correcting linearity errors in a digital to analogue converter (DAC) rely on characterising the DAC first. This paper describes a technique that can increase linearity without characterising the DAC. It is in principle, able to remove completely deterministic errors. As no calibration is needed the improvement can track dynamically changing errors due for example to thermal effects.*

Keywords – Linearisation, Digital to analogue conversion.

1. INTRODUCTION

The best-fit linearity measurement procedure generates a line that represents the average linearity of a digital to analogue converter (DAC) when all of the points are considered. This concept, that "averaging" the levels in the DAC can produce a single response, may be extended to a practical situation. For example, if adjacent pairs of points in the DAC response are taken two at a time, then their averages constitute a characteristic that has less error. This is the same mechanism that allows a direct interpolation digital to analogue converter (DIC DAC)[1] to have better linearity than the target DAC. If more than two levels are averaged at a time, then the errors are reduced even further. In fact, when all of the levels in the response are averaged then there is no error in the characteristic at all; i.e. the result is a single point that is precisely placed on the "best-line".

It is unrealistic to use all of the levels in the DAC to eliminate linearity errors. However, when a smaller number of levels are taken for the averaging process, points will be left with a useful improvement in linearity.

2. THE LINEARISING RAMP PROCEDURE.

A technique by which the averaging process may be implemented is by using a "linearisation ramp" [2]. This is a digital signal that is added to the incoming data for each and every sample interval. A ramp can be added to the input data stream by using a conventional digital adder. It is preset at the start of the sample interval with the sample data value, and then counts up by a fixed amount for a number of "oversample" intervals. (Note - this process has nothing whatsoever to do with Oversampling, Noise Shaping or Interpolation, this is just another convenient misuse of the term).

2.1 Loss of Range with a Ramp Linearisation Technique

The ramp averaging technique, results in a loss of usable DAC range. This results in the dB signal to noise ratio (SNR) of the system being degraded in accordance with the dB loss in range. For a ramp technique using an increment of R-LSBs, for 2^L oversample periods the ramp peak-to-peak amplitude (A) in LSBs is:

$$A = R\left(2^L - 1\right) \tag{1}$$

The dB Loss of Range (LOR) for this ramp in an M-bit DAC is:-

$$LOR = 20\log_{10}\left(1 - \left(\frac{A}{2^m}\right)\right) \tag{2}$$

In order to justify the use of the system, an improvement in performance must therefore be produced which outweighs this loss in SNR.

2.2. Effect of the Linearising Ramp on DAC Linearity

The linearising system has different effects on the three main DAC error types. These are now analysed separately.

2.*2.1. Effect on DAC Random Errors*

It is known that the variance of a random sample set decreases in relation to the number of samples taken. This indicates that when the number of samples is multiplied by a factor of four, the standard deviation (rms value) is halved. If this result is applied to a DAC with truly random error characteristics, it implies that there will be a 3dB improvement in the linearity of the component for each doubling of the number of averaged levels. However, this result is only an approximation for the following reasons:

i) The DAC characteristic must be truly random,

ii) The DAC must have a large number of levels .

When these requirements are present, the dB Gain (G) in linearity is given by the number of averaged Levels (B):

$$G = 3.01\log_2(B) \text{ , B > 0} \tag{3}$$

(Note, B = 1 is the situation where no averaging is used; i.e. the normal level is selected for the duration of the sample interval).

The dB value obtained from this calculation may be added directly to the uncompensated THD figure to estimate the performance of the linearised system. This equation

indicates that the more ramp amplitude that is added to the system the more linear the system will become. The gain in linearity performance will be somewhat offset by the loss of range. In fact, a situation arises where the effects balance. Any extra ramp that is added beyond this amplitude causes degradation in the overall performance. This level may be calculated by equating the rate-of-change of Equation 2 with that of Equation 3. In this case it assumed that A = B; i.e. the ramp increment is one unit, and the number of averaged levels equals the ramp amplitude. This means:

$$\frac{d}{dA}(MR) = -\frac{d}{dB}(G)$$

$$\frac{d}{dA}\left(20\log_{10}\left(1-\left(\frac{A}{2^M}\right)\right)\right) = -\frac{d}{dB}\left(3.01\log_2(B)\right) \quad \text{dB}$$

Substitute $\log_Q R = \dfrac{\log_e R}{\log_e Q}$

$$\frac{d}{dA}\left(J.\log_e\left(1-\left(\frac{A}{2^M}\right)\right)\right) = -\frac{d}{dB}\left(K\log_e(B)\right) \quad \text{dB}$$

Where $J = \dfrac{20}{\log_e 10}$ and $K = \dfrac{3.01}{\log_e 2}$

So $$-\frac{J}{2^M - A} = -\frac{K}{B}$$

Substitute B = A,

$$A = \frac{K.2^M}{J+K}$$

i.e. $$A = \frac{2^M}{3}$$

This result shows that there is, in theory, nothing to be gained from using a linearisation ramp that exercises more than 1/3 of the DAC Levels. As a consequence of this result, the maximum improvement in linearity that can be reached with a specific component is related solely to the number of levels that it possesses. This means that higher resolution devices have a greater potential for improvement.

2.2.2. Effect on DAC Superposition Errors.

Superposition errors do not affect DACs in a clearly defined manner. Depending upon the type of error that is shown in the DAC, the linearisation process may, or may not, reduce the superposition problems. For example, Prazak [3] indicates that the finite input impedance associated with a DAC current-to-voltage output amplifier introduces a superpositional error. This type of problem does not affect the linearity of the DAC to the same extent, for example, as random errors; because the error is proportional to the total output current flow; i.e. it produces a gain error that does not degrade linearity. Some types of error that are often referred to as superposition errors are caused by secondary cumulative effects.

For example, the "bowed" or "S-shaped" characteristics that may be observable in some DACs are caused by the modification of primary superpositional errors according to secondary effects. For example, if the input impedance in the DAC output amplifier, just described, varies according to the current flow, then this will result in a non-linear superpositional effect. Such an error will cause problems. Furthermore, it will not be improved to the same extent as random errors by the addition of the ramp linearisation process. In this context, many secondary superpositional effects may be treated as special cases of random defects where there is high correlation between adjacent errors. For this reason they will be reduced in the manner described earlier; i.e. at much less than 3dB/octave.

2.2.3. Effect on Deterministic Errors.

It is upon deterministic errors that the linearisation system has the greatest beneficial effect. This is because the procedure has the ability, in theory at least, to completely eliminate deterministic errors from a DAC. The deterministic errors of interest to this section are caused primarily by mismatches within the generators of a segmented architecture. It is possible to model these errors with the structure shown in Fig. 1.

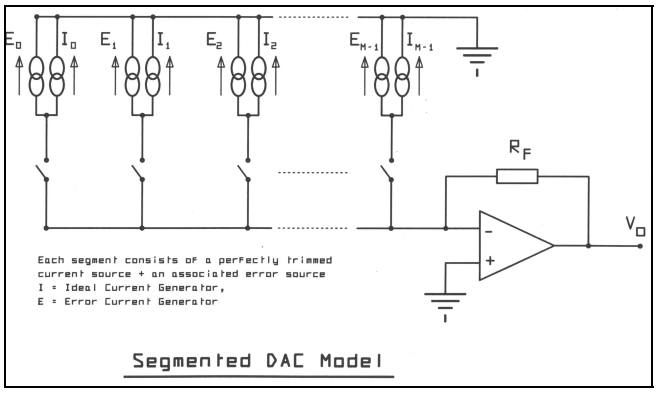

Fig.1 – Segmented DAC Model

In this respect the component may be thought of as being composed from perfectly trimmed generators and associated error sources. This model of the DAC is attractive because it shows in a straightforward manner how the error generators interact to produce the error characteristic peculiar to

segmented components. In this case it is quite clear that as many different errors may be produced as there are levels in the component. Given that so many errors are produced, and that these are far from random, how much of an improvement can be expected with the use of a linearising ramp? In order to understand the general effects of the linearising ramp upon segmented DAC linearity, it is best to first consider a specific case.

3. EXAMPLE OF LINEARISATION PROCESS

Consider that the model of Fig. 1 is used to mimic a 3-bit segmented DAC. Seven of the eight levels that this component produces will be in error according to the selection of the error generators. (The 0-level activates no segments and has no error). Consider now that this component is used with a ramp linearisation technique at "2-octaves"; i.e. four oversample intervals per sample period. Furthermore, let the selected ramp increment be 1 level, which means that four consecutive levels are selected in the DAC per sample interval .

When this linearisation scheme is used with this DAC, five levels remain within the coding range. The amplitudes of these levels can be calculated in the manner shown in Fig. 2.

Observation of the results of Fig. 2 shows that all of the five new levels are in error by different amounts. However, close observation of these values shows that each error can be divided into two parts. Firstly, each contains a $(E_O + E_1)/2$ term. Because this is common to all terms, it represents a constant offset of all the levels and may be neglected; i.e. it is an offset error that does not affect the linearity of the component. When this "offset" term is removed from each of the levels, the remaining errors may be described as K x $E_2/4$, where K is an integer in the range 0 to 4, and represents the identity of the new level. It can easily be observed that this is a linear equation dependent solely upon the values of K and E_2. As a consequence, it is concluded that the error in the linearised device increases consistently with the value of K. This means that it represents a "gain" error and does not affect the linearity of the component; i.e. it may be ignored.

When the gain and offset error terms have been removed from the levels of Fig. 2, it is observed that no further error terms remain. This means that the DAC has perfect linearity. In general, this result is the same for any segmented component of any resolution, provided it uses a linearisation ramp of half Range. In each of these cases, the "Offset" error term is the average of all error generator values (except the MSB); the "Gain" error is then dictated solely by the MSB error generator. Before it is concluded that this is a cure for all segmented DAC Linearity problems, there is a practical consideration that restricts the beneficial effects of this result. In practice this result is limited because it is rare that DAC errors are solely deterministic. In this respect, the segmented DAC will generate other errors with Random or Superpositional characteristics.

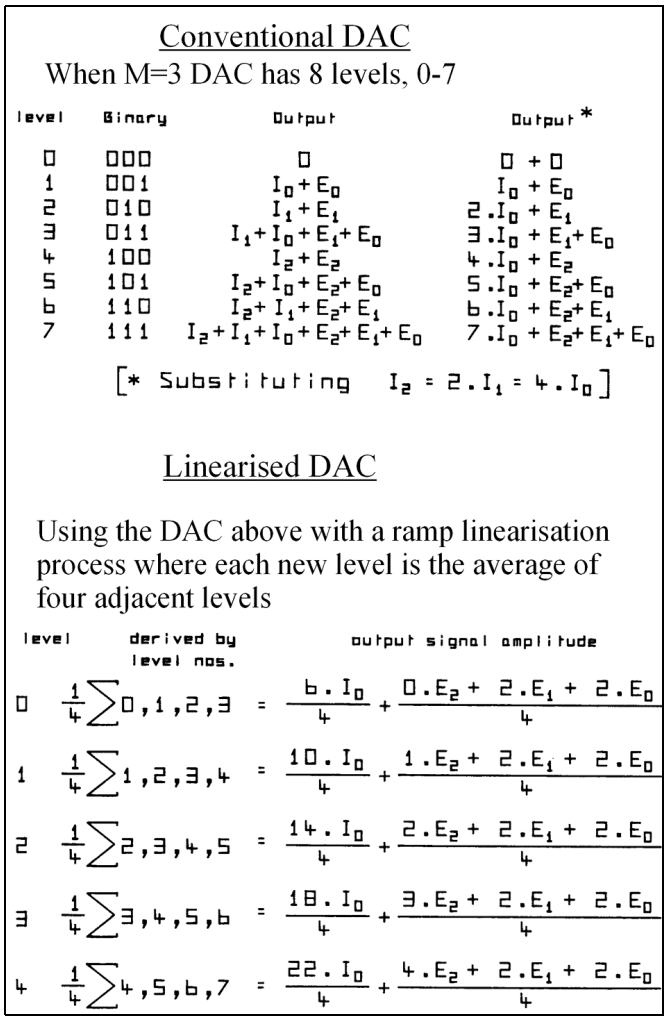

Fig.2 – Segmented DAC linearisation

Whilst the ramp linearisation process can completely eliminate deterministic errors, it will have much less of an effect upon the other error types.

In general, the quantity of linearisation required to eliminate the deterministic errors from a segmented component depends upon the error characteristics. Because the model of Fig. 1 is a general model, the result indicated is valid regardless of the error magnitudes. This means that the only deviation in operation occurs when the values of some of the error sources are zero. Under these circumstances, less levels need to be averaged to eradicate the linearity errors.

When all but one of the error generators have a zero value, then the number of levels that need be averaged in order to eliminate the deterministic error is reduced to just two. In this case, if the identity of the segment in error is Z, then the averages of pairs of levels which differ in magnitude by 2^Z will comprise a DAC characteristic of perfect linearity. For example, consider in the DAC model of Fig. 1 that all error sources produce zero error except the LSB. This segment has the identity "O", and introduces the error E_0. For this reason, only those Levels which use this generator will suffer from an error; i.e. only the binary codes which end in a "1", (XXXXXX1), will demonstrate an error. Furthermore,

those levels that are in error differ consistently from the ideal levels by the value of E_0. For this reason, the DAC transfer characteristic may be thought of as being composed from two responses of perfect linearity, separated by the value E_O. This is shown in Fig. 3.

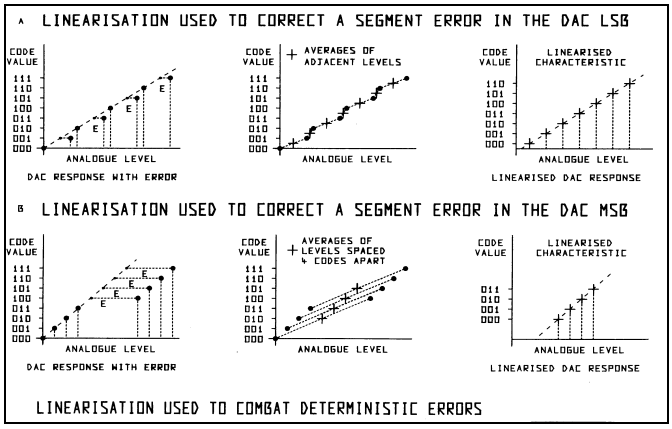

Fig.3 – linearisation of Deterministic Errors

The former definition indicates that under these circumstances a single, highly-linear transfer characteristic can be produced by taking the averages of pairs of points which differ in amplitude by 2^0 LSBs; i.e. differ by 1 LSB. When this is performed, a single characteristic is produced (Fig. 3). This response is consistently $E_0/2$ in error; i.e. linear but with an offset error. If the single segment in error is number (M-1), i.e. the MSB segment, then only the top half of the DAC range is in error. Once again because only a single segment is in error, only two levels need to be averaged. However, in this case, these need to be spaced by $2^{(M-1)}$ LSBs. By taking the averages of one point in the bottom half of the DAC range with one point in the top half, the error once again becomes distributed evenly across all the new levels. (This result indicates why it may become-necessary to use ramp increments that are greater than one.)

In these last two examples, even though only two levels are averaged on each occasion, the spacing between the levels varies according to the "significance" of the error source. For this reason, the loss of range required to linearise a component with a single segment error varies according to the identity of the error. (Notice that provision has been made for this already in Equations 1 and 3 by using different expressions for ramp-amplitude and number of averaged levels.)

In general, the minimum number of levels that must be averaged to remove the linearity errors from a segmented component is defined by the number of segments which are in error. In this case the number of averaged levels doubles for every segment in error. If K-segments are in error in an M-bit DAC then the number of levels which must be averaged (A) is given by:-

$$A = 2^K \qquad K < M$$

This expression correctly predicts that when there are no segments in error, only one level need be averaged; i.e. the single DAC level that is produced is correct and need not be averaged with any other. Furthermore, there is no point in averaging more than $2^{(M-1)}$ levels in the component because this has already been shown to remove all of the deterministic errors. When a DAC is linearised using this reduced number of codes, the levels selected must be distributed according to the identities of the segments in error. For example, if segments 0 and 2 are in error, then the ramp must contain increments with values 1 and 4. This can be achieved by using the ramp sequence 0, 1, 4, 5 (these are the offsets from the selected level). This sequence selects the errored segments with the same frequencies; i.e. two sets of levels in this sequence differ by the value 1, two sets of levels differ by the value 4.

4. CONCLUSIONS

A linearisation technique has been described that is able to compensate for DAC errors that vary with time as no absolute calibration system is used. It is able to remove completely errors that are deterministic and reduce those that are random.

If the DAC linearity characteristic is dominated by the deterministic errors associated with segment mismatching, then the addition of a linearisation scheme has the ability to completely eliminate these defects. In this case the DAC will become perfectly linear when a half-range ramp is added to it. Practical performance achievable in terms of bits of linearity and Nyquist rate can exceed that of conventional DACs.

5. ACKNOWLEGEMENTS

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6. REFERENCES

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