A METHOD FOR THE IN-CIRCUIT TESTING OF ΣΔ MODULATORS

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Abstract *— A method for characterizing ΣΔ modulators is described which can be built in large integrated circuits or systems-on-chip. The method can be used to measure gain and phase, as well as, total harmonic distortion and signal to noise and harmonic distortion ratio parameters. It is prone to be built in circuit, when computational resources such as digital signal processors or re-programmable logic are available, but can also be used in computer simulations making it easier to compare expected with measured performances.*

Keywords - ΣΔ converters, embedded test.

1. INTRODUCTION

Sigma-Delta (ΣΔ), or Delta-Sigma, modulators are key blocks in ΣΔ data converters. Their testing is a non-trivial operation, as usually a long data set has to be acquired and processed with specific algorithms. This task is even more difficult to be performed when converters are embedded within systems-on-chip (SoC) due to a more difficult access for testing.

Analogue design for testability schemes for ΣΔ converters have already been presented which provide either parametric (i.e. the measurement of characterization parameters) or structural test [1, 2, 3, 4]. In this paper a new method is presented that can be used to measure gain and phase, as well as, THD (Total Harmonic Distortion) and SINAD (Signal to Noise and Harmonic Distortion ratio) parameters which can also be applied for testing different analogue and mixed-signal transfer functions.

It is based on cross-correlating the output signal with sine and cosine forms of the test stimulus. As these operations can be implemented in-circuit reusing programmable logic available in the system, minimization of the final test circuitry overhead is allowed. In a system the use of reconfigurable hardware allows, at any time in the entire product life cycle, the implementation of the hardware modules needed for each test operation, thus warranting a much more efficient use of available resources. Furthermore, as the test processing operations are fully performed in the digital domain calibration needs are minimized, and complete digital blocks (e.g. digital filters) can also be included in the test path.

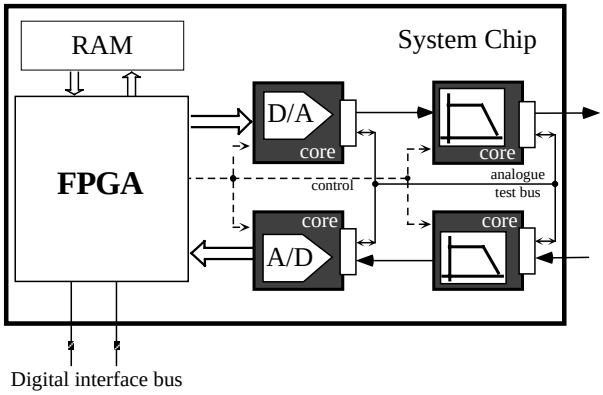

Figure 1: Architecture of a typical integrated system.

Fig. 1 illustrates the block diagram of a circuit architecture which can be found in many SoCs that have to interface with analogue signals. In this case a FPGA (Field Programmable Gate Array) is used to implement all mission logic like, e.g. signal processing, bus control, interface with other internal and external digital blocks, and the control of the A/D and D/A converters and of the programmable filters. Other common architectures may include different blocks. In any case advantage can be taken of the FPGA to implement the circuitry required to implement the test operations and thus decrease test circuitry overhead. A circuit with such architecture was used for the experimental evaluation of the method being proposed. The details concerning the progamming of the FPGA and the routing of the analogue signals are not under the scope of this paper, but standard infrastructures such as IEEE 1532 [5] and IEEE 1149.4 [6] could be used for this purpose.

Next section describes the method being proposed, and section 3 discusses implementation aspects and results obtained in the testing of a 2nd order ΣΔ modulator using

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a FPGA to performe the test operations. Section 4 ends the paper highlighting the main conclusions.

2. MEASURE OF GAIN AND PHASE

Conceptually the method being proposed to evaluate a transfer function's gain and phase at frequency ω is presented in fig. 2.

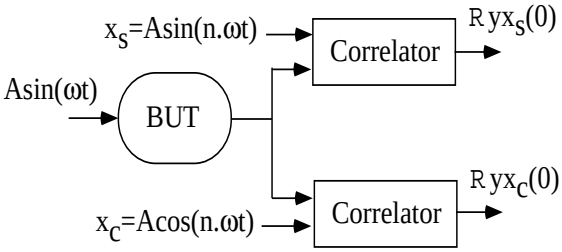

Figure 2: Correlation based transfer function analyzer.

This measurement is based on the computation of two cross-correlations. One is the correlation of the output signal y of the block under test with the input stimulus $x_s = Asin(\omega t)$, and the other with $x_c = Acos(\omega t)$, respectively, $\mathcal{R}_{yx_s}(0)$ and $\mathcal{R}_{yx_c}(0)$. It can be shown that from the values of these correlations at delay zero the gain and phase of the transfer function are given by, respectively [7]:

$$|H| = \frac{2}{A^2}\sqrt{\mathcal{R}_{yx_s}(0)^2 + \mathcal{R}_{yx_c}(0)^2} \quad (1)$$

$$\angle H = arctg(\mathcal{R}_{yx_c}(0)/\mathcal{R}_{yx_s}(0)) \quad (2)$$

Fig. 3 shows the evolution of gain and phase errors of a 2nd-order 64 oversampling ratio $\Sigma\Delta$ modulator computed from the difference between the values obtained by simulating the transfer function and by applying the present method. These values are given as a function of the number of cycles which define the data length and of the ratio between the stimulus frequency and the modulator's Nyquist frequency ($Normalised\,frequency = 1 \rightarrow f_{stimulus} = f_{sampling}/64$). It can be seen from the errors amplitude that the values obtained by correlation are in very good agreement with the expected ones. We can conclude that a small number of data cycles, independently of the stimulus frequency, is enough to obtain good accuracy, an important aspect to allow for the simplification of the resources required to implement this test in-circuit.

2.1. Measure of THD and SINAD

If $|H|$ values are obtained correlating the same previous output test response with harmonics of the input signal, i.e. $x_s(n\omega) = A.sin(n\omega t)$ and $x_c = A.cos(n\omega t)$, where $n = 2, 3, \ldots, m$, the output response can also be characterized in terms of distortion and noise related parameters.

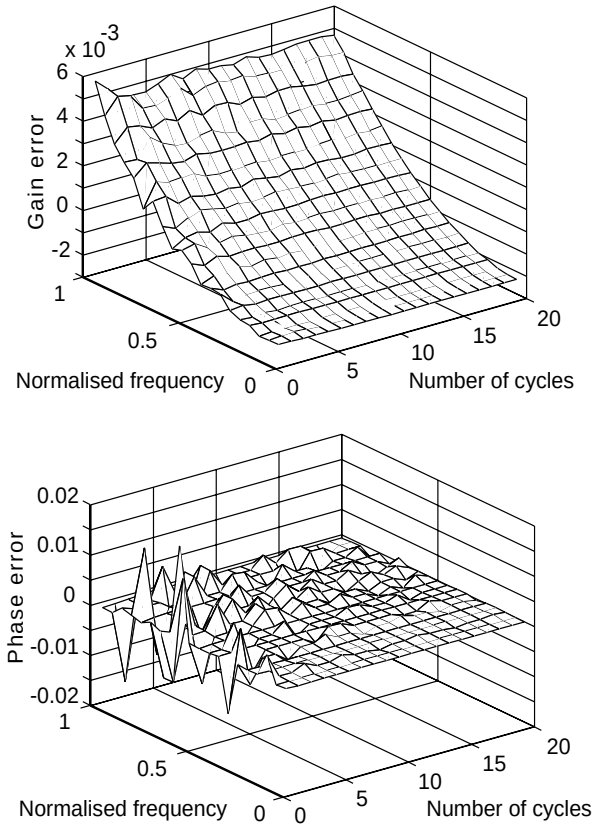

Figure 3: Gain and phase errors obtained with the proposed method, comparing to the expected theorectical values.

Being the amplitudes of all correlation input refence signals always the same (A), it becomes:

$$THD = \sqrt{\frac{\sum_{n=2}^{N} |H_n^{'}|^2}{|H_1|^2}} \quad (3)$$

where $|H_n^{'}|$ represents now the relative amplitude of the harmonic at frequency $n\omega t$. A similar approach can be used to calculate the SINAD parameter. SINAD is given by the ratio

$$SINAD = \sqrt{\frac{P_{fund}}{P_{noise} + P_{harmonic\,distortion}}} \quad (4)$$

$$SINAD = \sqrt{\frac{P_{fund}}{P_{\Sigma\Delta} - P_{fund}}} \quad (5)$$

where P represents power. Equation (5) expresses the fact that the sum of the powers of noise and harmonic distortion corresponds actually to the difference between the total power of the $\Sigma\Delta$ bit stream and the power of the fundamental component. Similarly it can be written

$$SINAD = \sqrt{\frac{V_{fund}^2}{V_{\Sigma\Delta}^2 - V_{fund}^2}} \quad (6)$$

$$SINAD = \sqrt{\frac{|H|_{fund}^{'2}}{1 - |H|_{fund}^{'2}}} \quad (7)$$

bearing in mind that the power of a $\Sigma\Delta$ bit stream with normalised amplitude (+1/-1) is constant and equal to one, and that $|H|_{fund}^{'}$ is calculated taking the amplitude of the bit stream as the amplitude of the correlation $\sin$ and $\cos$ input references.

Fig. 4 shows the evolution of THD and SINAD values obtained again for a 2nd order $\Sigma\Delta$ modulator with a 64 oversampling ratio, as a function of the amplitude resolution of the correlation input refence signal. It can be seen that for resolutions higher than the one corresponding to the expected effective number of bits of this modulator [8] the accuracy of the measures is very good. Similar results were obtained for first- and second-order modulators with different oversampling ratios.

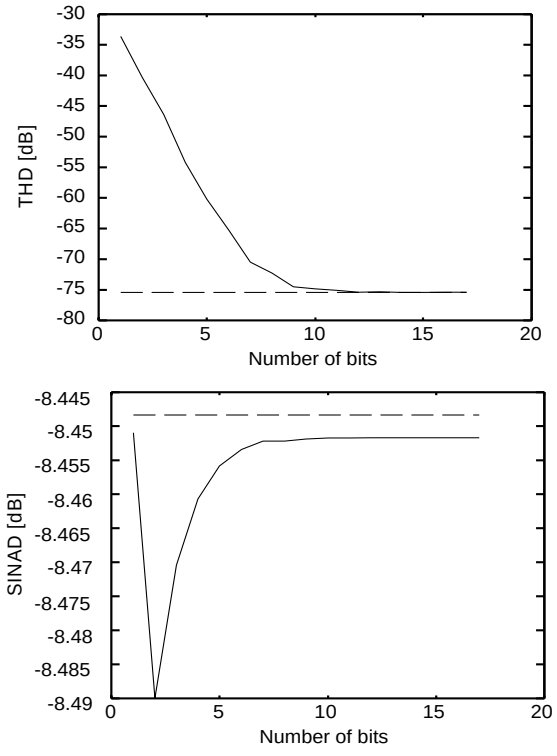

Figure 4: Evolution of THD and SINAD values obtained with the method being proposed.

The value of SNR (Signal to Noise Ratio) can also be obtained externally from THD and SINAD:

$$SNR = \frac{1}{SINAD^{-1} - THD} \quad (8)$$

3. IN-CIRCUIT IMPLEMENTATION

A circuit with an architecture similar to that one presented in fig. 1 was used to perform experimental measures. The external digital interface with the FPGA is provided by a PC (personal computer) bus which is used to download the FPGA configuration, to start the tests, and to upload the test results. A control mechanism built into the FPGA allows to control the normal operation and test modes of the four mixed-signal blocks. The availability of an analogue bus allows to route the test stimuli and responses according the path or block under test. This bus can be implemented in-chip with the IEEE 1149.4 infrastructure [6].

Correlators can be implemented using different alternative architectures which trade-off size for accuracy. The discreet correlation operation consists essentially of a sum of the multiplications between samples of the two signals being correlated. In our case, as the normalised samples of the $\Sigma\Delta$ bit stream present only $+1$ and -1 values, all that is performed is the accumulation of the samples of the reference signals after being multiplied by $+1$ or -1. Two's complement format is used to facilitate the implementation.

To calculate THD and SINAD parameters using only operations implemented with simple logic circuits, (3) and (7) were rearranged in a more convenient way. As the absolute value of THD is usually < 1 its inverse (THD^{-1}) is calculated in order to avoid scaling operations. Also, as the square root operation is difficult to implement, THD^{-2} is obtained instead. As far as SINAD is concerned the value which is actually obtained corresponds to $1024 \times SINAD^2$, being the multiplication by 1024 used to avoid operations with small numbers. The vales of THD and SINAD obtained this way in the circuit are then externally post-processed with simple operations to get the real ones.

Besides addition and two's complement operations, squaring and division operations are performed using bit serial architectures in order to minimize area as much as possible. These operations, together with the circuits required to control all computations, as well as the interface with a PC and an external RAM, were implemented within a XILINX 4010 FPGA. The RAM is used to store the samples of modulator's output and of the sine and co-sine reference signals.

Table 3 presents the values of THD and SINAD of a 2nd order $\Sigma\Delta$ modulator with a 64 oversampling ratio obtained with the method being proposed by simulation, by performing the computations within the FPGA, and by using a bench test instrument.

Table 1: Values of THD and SINAD [dB].

Parameter	Simulation	FPGA	Instrument
THD	-73.7758	-73.7758	-75.4052
SINAD	-8.4519	-8.4595	-8.4484

4. CONCLUSIONS

A method suitable for the in-circuit measure of functional parameters of $\Sigma\Delta$ modulators is presented. Having in mind the test of modulators embedded in integrated systems, it can be implemented by (during test mode) reusing programmable cores available on system, allowing thus to minimize test circuitry overhead and to provide in-circuit testability over the circuit's life-cycle. All test operations can be performed without using any additional auxiliary test instruments, other than a digital interface necessary to download the programmable logic configuration, trigger the tests, and to upload the resulting test signatures. As the method is applicable to different functional cores, it allows for taking the maximum advantage of the programmable resources available on-board.

This test method relies on cross-correlating the observed output signal with sine and cosine reference waveforms. It can be used to characterize the transfer function of a core or signal path under test in terms of gain and phase, as well as of the harmonic content of its output response. Results for THD and SINAD of a 2nd order $\Sigma\Delta$ modulator were obtained with small errors both by simulation and by performing the computations in-circuit within a field-programmable gate array.

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