FAISABILITY STUDY OF A SINGLE LOCAL OSCILLATOR DIGITAL RADAR RECEIVER

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Abstract - *High speed ADCs are considered more and more by ADC manufacturers. The aim of such components is that they are to be used in applications such as high speed data acquisition devices, digital oscilloscopes, digital RF/IF signal processing, digital RF down conversion... The application we target in this research is the last one, digital RF down conversion, by the use of a high speed ADC (8 bits – 1 GSPS) in a radar receiver. In this article, we present a brief comparison between two kinds of radar receiver architectures : the superheterodyne and the expected one. We also present the method to characterise the ADC working in radar mode and the conclusion of the research.*

Key words - Analog-to-Digital Converter, Digital Radar Receiver

1. INTRODUCTION

Up to now, most radar receivers work following the same architecture using an analog-to-digital converter (ADC) to digitise a low carrier frequency signal as shown in Fig. 1.

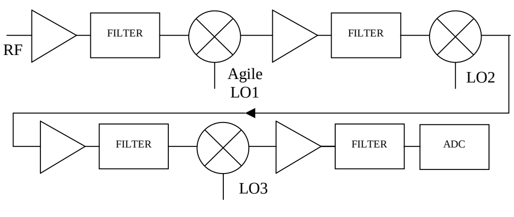

Fig. 1 – Superheterodyne receiver architecture

The development of high sampling frequency ADC, from one to several Giga Hertz, allows the prospect of new receiver architectures. Indeed, why don't we digitise the radio-frequency (RF) signal directly after the antenna ? Of course, this idea seems very interesting from a technical point of view as from the industrial one. It has already been written by Dietmar Matthes [1] and prototyped by William S. Song [2] but this architecture is already limited by the ADC bandwidth and quality (cf. Fig. 2). Studies under way are actually oriented toward receivers with only one frequency carrier transition level (cf. Fig. 3).

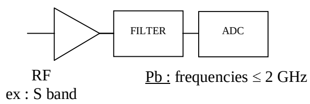

Fig. 2 – Ideal receiver architecture

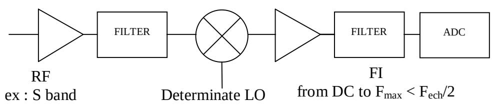

Fig. 3 – Optimal receiver architecture

The local oscillator (LO) used could stay agile but the advantage of the large Nyquist band would be partially lost, moreover an agile LO is more difficult to generate than a determinate one. Thus, we will rather choose to study a determinate LO receiver allowing the ADC to digitise the whole radar agility frequency band. The "agility frequency band" is the frequency range in which the carrier can operate.

As written above, in addition to the agile frequency generation abolition, such architecture results in a lower volume. This receiver concept could be developed if the kind of ADC we talk about, in addition to their high sampling frequency, had enough resolution bits (like in traditional ADC's). Unfortunately, that's not the reality. The components we expect to use have resolutions that are generally from 4 to 6 bits lower than those used today.

The aim of this research is to analyse if the restricted dynamic of these components is a problem for their use in the application we target. We also want to know what are the consequences of their defaults on their dynamic parameters and their ability to be integrated in a radar receiver processing line... The research has to validate the concept of radar receiver with a single determinate local oscillator.

The article will successively deal with the key component analysis, the concept validation on a prototype, the difficult points and finally the methods to resolve them.

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2. KEY POINT ANALYSIS : THE ADC

This part of the research allows us to better understand the phenomena that drive the final characteristics of the ADC, i.e. its dynamic parameters. So, first, we registered the main defaults of the converter. Then, we measured them on a real ADC available on the evaluation board, ATMEL JTS8388. After that, we have built a realistic ADC model [3].

Thanks to this model, we characterised the ADC by measuring its dynamic parameters versus the level of each default. This preliminary work permits us to know on which default we have to focus to reach the goal performances. This characterisation finished, we followed the same method by using a signal constituted from radar pulses (non-linear frequency modulated pulses) instead of a continuous sine wave signal. Default effects are observed all along the processing line and especially after the pulse compression tool and the Doppler filter.

2.1. ADC defaults : measurement and modelling

The defaults inserted in the ADC model are sampling clock jitter, internal noise and integral and differential non-linearity (INL and DNL).

2.1.1. Clock jitter

Clock jitter is an ADC intrinsic default which results in a random slight shift of the sampling time. In components considered, rms. jitter is about one picosecond. To model it, we added gaussian noise at the sampling moment of the signal to quantify. The standard deviation of the noise comes directly from the amount of jitter to insert.

2.1.2. Internal noise

The ADC internal noise comes from thermal noise of all the internal electronics. This noise additional to the quantification noise results in a practical SNR, 6 dB lower than the theoretical one. The Effective Number Of Bit (ENOB) is almost one bit under the physical one. To model this default, we add gaussian noise to the signal.

2.1.3. Non-linearity

The ADC transfer function non-linearity is the result of internal architecture adjustment components. In the case of a FLASH architecture, resistors are laser adjusted. Non-linearity moves the transfer function from the fine line one of Fig. 4, to the bold line one in the same Figure.

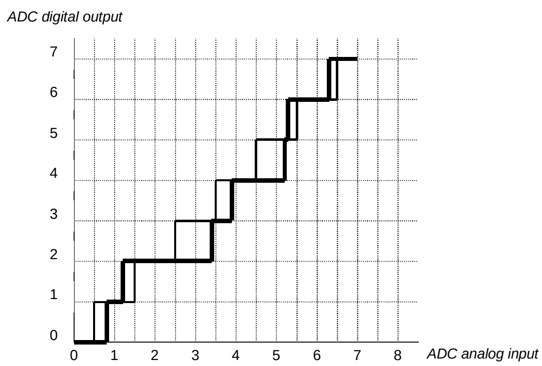

Fig. 4 – ADC non-linearity shown on transfer function

Non-linearity is characterised by two parameters : differential non-linearity (DNL) and integral non-linearity (INL) determinated for each output code. DNL gives the difference between the width of the theoretical analog step and the practical one for the i code. INL also gives, for each code, the difference between the practical and theoretical transfer function. A recursive algorithm models these defaults in a few recurrences starting from the theoretical transfer function and finishing with the practical one. The number of recurrences is linked to the DNL of the i code.

2.2. Default impact on the dynamic parameters

In this part, we evaluated, by simulation, each ADC default impact on its dynamic parameters. The parameters we talk about are SNR (Signal To Noise Ratio), SINAD (Signal to Noise and Distortion Ratio), SFDR (Spurious Free Dynamic Range) and THD (Total Harmonic Distortion).

The signal used for these measurements was a continuous sine wave which frequency is about ten times under the sampling one. This Results are shown in Fig. 6 to Fig. 10.

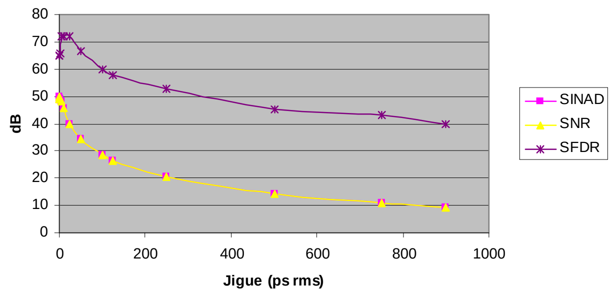

Fig. 5 – ADC dynamic parameters vs. Clock jitter level

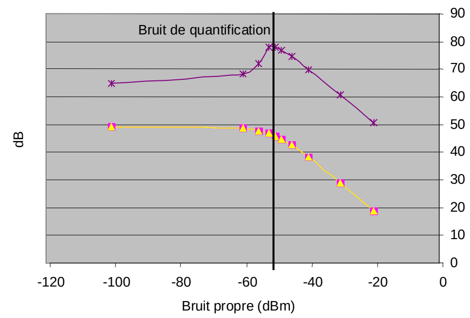

Fig. 6 – ADC dynamic parameters vs. internal noise level

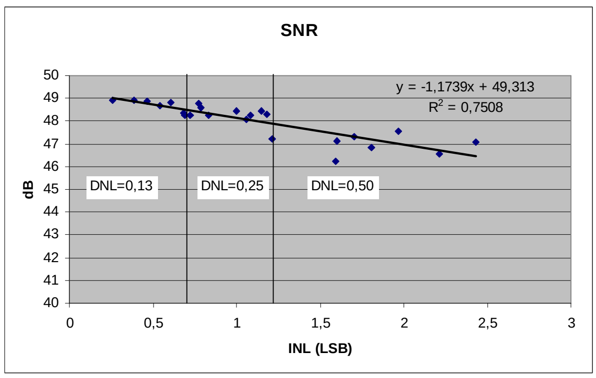

Fig. 7 – SNR vs. Non-linearity

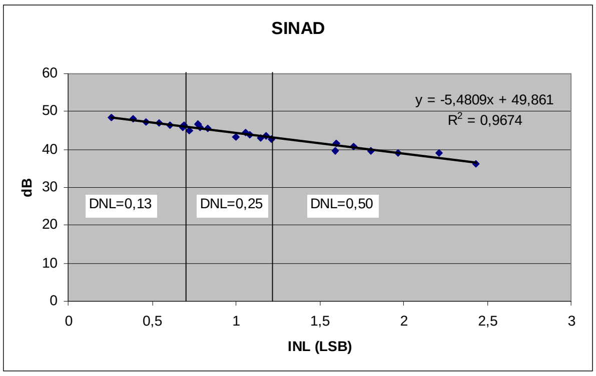

Fig. 8 – SINAD vs. Non-linearity

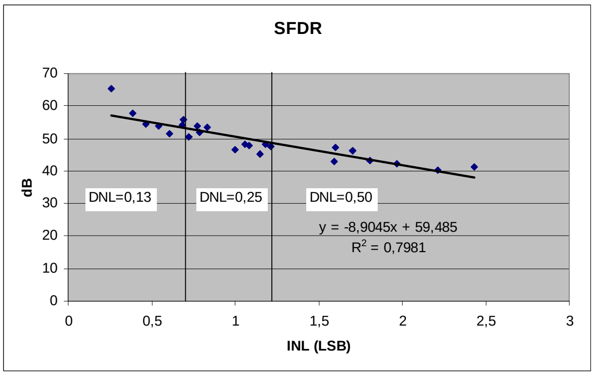

Fig. 9 – SFDR vs. Non-linearity

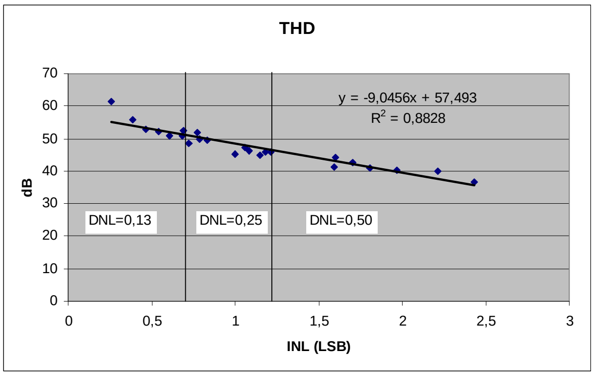

Fig. 10 – THD vs. Non-linearity

Theses experiments allowed us to show that clock jitter and internal noise affect dynamic parameters. Furthermore, an optimum value permits the improvement of the SFDR. Non-linearity decreases all parameters.

Some equivalent experiments where two defaults were inserted showed that there is no interaction between defaults. Indeed their effect are additive.

2.3. Default impact in radar mode

In order to observe default impact in radar mode, we built the basic modules of the radar processing chain on radar signals (non-linear frequency modulation pulse) and we observed the pulse compression output. The level of the sidelobes is compared to the level of the principal lobe. This last one is kept secret for confidential reasons. Each default impact is shown in Fig. 11 to Fig. 13.

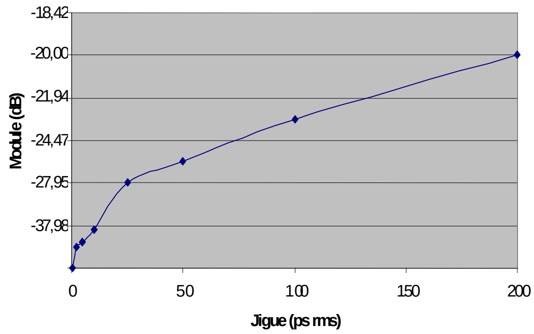

Fig. 11 – Sidelobes level vs. Clock jitter level

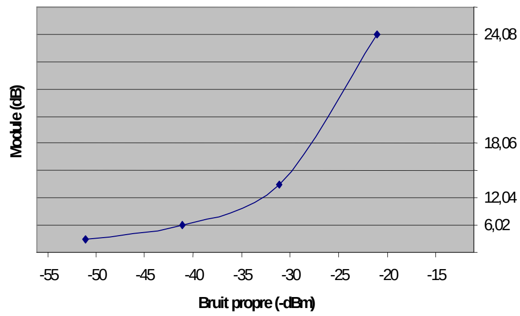

Fig. 12 – Sidelobes level vs. Internal noise level

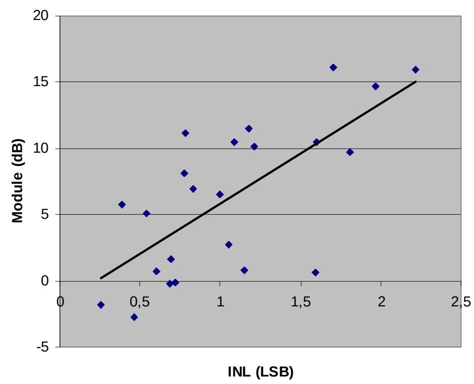

Fig. 13 – Sidelobes level vs. Non-linearity

The most cumbersome defaults, for typical values observed in fast ADC, are the non-linearity because of the side lobes they create that can be detected as a target. We have to decrease these defaults.

3. CONCEPT VALIDATION AND PROTOTYPE TEST

In order to validate the concept, we built a prototype of a radar receiver using a determinate local oscillator and a high speed ADC (8 bits – 1 GSPS). It is made from Components Off The Shelf (COTS). This is simply an assembly that moves the signal frequency from S band to a frequency range included in the Nyquist band. The ADC ends this assembly. The prototype is shown in Fig. 14.

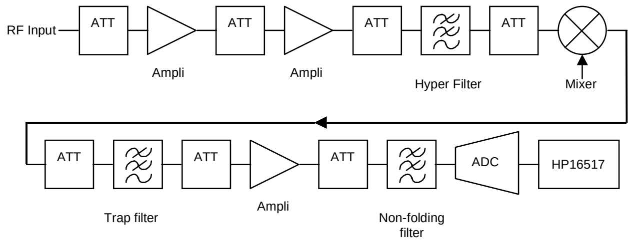

Fig. 14 – Single local oscillator digital radar receiver prototype

This prototype was compared to an operational radar receiver. The dynamic performance like SNR and SFDR are in the same range of values in the two cases. Spurious signal performances are 10 dB better on the prototype. The explanation is that in the same frequency analysis band, the larger the Nyquist band is, the fewer the number of folded spurs. However, this prototype cannot actually be used in a radar context. Indeed, single tone and two-tone linearity are not good enough (respectively 10 and 20 dB under requirement) and directly coming from the ADC non-linearity. This restriction was previously highlighted in the second paragraph. The only spurs we see are harmonics of the signal injected in the device. Due to lack of instrumentation, especially the available memory on logic analysis system, the experiment and the measurement was stopped.

4. CONCLUSION : LEARNING AND HARD POINTS

This research gave several facts. Straightway, it is necessary to linearise the ADC to reach the expected performance of radar applications. It can be done in two steps : first, it is necessary to separate the quantification noise from the input signal. Then, we can implement a learning method to modify the ADC transfer function toward the ideal one for reducing the harmonic level. The prototype creation has shown that it is necessary to optimise the processing by reducing the computing and look for new processing architectures. Indeed, the flow of data after the ADC is so important that real time processing of amplitude/phases demodulation and filtering is difficult. Technology evolution and processing optimisation will allow us to cerate radar receivers using this kind of analog to digital converters.

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