# Testing DNL and INL of ADC by the exponential shaped voltage

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**Summary -** *Testing of ADC's differential nonlinearity DNL(k) by the histogram method requires the signal generator with extremely low distortion and high stability of the parameters. Besides this condition generator must be connected to the input of the ADC under test with high suppression of the interfering noise on ground line of instruments. The new type of testing signal has been proposed of the exponential form which could be generated by discharging of the capacitor across the resistance. The acquired digital samples from the output of ADC under test allow determining the best fitted exponential signal. The histogram from the registered samples and that for the best fitted exponential shape allows determining the differential nonlinearity DNL(k) for any code level k. Practical problems with generating the pure exponential shape are shown in this paper. The proposed method has been experimentally verified and was compared with the standardized methods.*

**Keywords:** ADC Testing, Histogram Method, DNL and INL, Exponential Stimulus Signal

## INTRODUCTION

One of the basic parameters characterizing the uncertainty of ADC is their deviation from the ideal transfer characteristic. In generally, the uncertainty is characterized by differential and integral nonlinearity – DNL(k) and INL(k). These parameters could be tested by the standardized methods [1], [2], [3]. The static testing methods utilize the calibrated voltage source which determines transient voltage T(k) by a control feedback, where the occurrence of two neighbouring codes have co-equal probability. The dynamic methods utilize the assessment of the histogram acquired for a known stimulus signal where the occurrence carries the information about DNL(k) of ADC. Conceptually the histogram test is less time-consuming than static. This advantage carries contemporary the weakness to ensure a stimulus signal generator which accuracy meets the DC calibrator. Various approaches are proposed in the literature [4], [5], [6] allowing to overcome the mentioned problem. Testing DNL(k) of ADC's by the histogram method requires a signal generator with extremely low distortion and high stability of its parameters. The testing stand must be precisely built with the high reduction of the noise, interfering coupling with other instruments and electromagnetic interference generated on the ground wires. The new method of the testing signal generation, which achieves the requirements listed above, was described in the paper [7]. Testing signal has the exponential form and is obtained by discharging of the capacity across known resistance. The advantage of such a signal is in the easy circuit implementation that could be correctly connected to the input of the ADC under test and isolated from the common ground (Fig.1). Closeness of the real signal shape to the ideal one depends on quality of the capacitor.

## GENERATION OF STIMULUS SIGNAL AND CALCULATION OF DNL AND INL

The generator of the stimulus signal with galvanic separation from the control unit is shown in Fig.1.

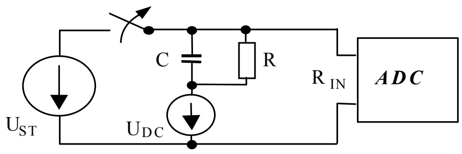


Fig.1. Circuit generating exponential stimulus signal.

The ideal shape of the discharging calibration voltage is

$$U_{IN} = U_{DC} + (U_{ST} - U_{DC})e^{-\frac{t}{RC}} \qquad (1)$$

The differential nonlinearity of ADC under test is estimated from the histogram of the registered samples using the well-known formula:

$$DNL(k) = \frac{H(k)}{H_{id}(k)} - 1 \qquad [LSB], \qquad (2)$$

where H(k) is the actual number of the histogram samples in bin k and $H_{id}(k)$ represents the number of histogram samples for ideal exponential shape of the stimulus signal. The acquired data from the ADC output (Fig.2) are represented by formula:

$$y(m) = \text{round}\left(B + A\, e^{\tau m}\right) \qquad m=0,....,M-1\ , \qquad (3)$$

where $B = \frac{U_{DC}}{Q}$ ; $A = \frac{U_{ST} - U_{DC}}{Q}$ ; $\tau = \frac{-1}{RCf_S}$ ;

Q is the ideal code bin width, $f_S$ is sampling frequency, round(.) is function of rounding to the nearest integer. M is the number of samples of this part of acquired data, which have the exponential form. Then the ideal number of histogram samples in the code bin k is

$$H_{id}(k) = \frac{1}{\tau}\ln\left(\frac{k - B}{k + 1 - B}\right) \quad \text{for} \quad k = 1,...,\left(2^N - 2\right), \qquad (3)$$

where N is the number of bits of ADC.

The ideal shape of the stimulus signal is unknown. Its parameters A, B and τ could be identified by fitting procedure from the acquired data using the least square fitting method. Then the ideal histogram $H_{id}(k)$ can be calculated by (3), DNL(k) by (2) and INL(k) using formula:

$$INL(k) = \sum_{j=1}^{k} DNL(j) \qquad [LSB] \qquad (4)$$

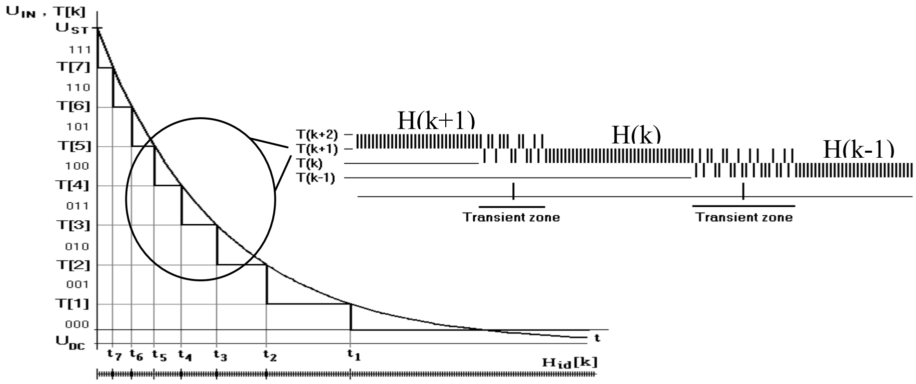


Fig. 2. ADC data record for exponential stimulus signal.

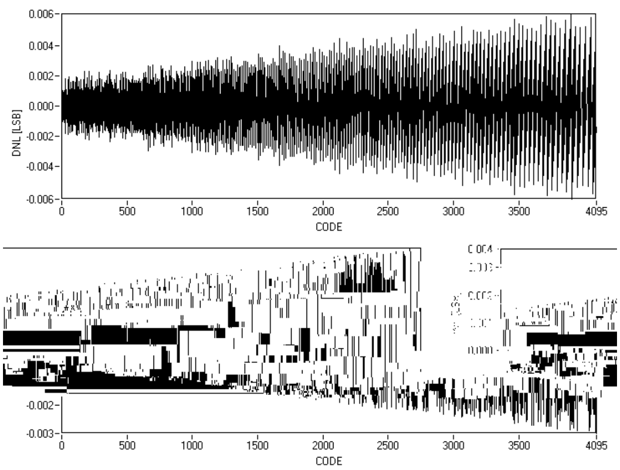


Fig.3. Accuracy of calculation of DNL and INL for full-scale range of 12bit ideal ADC. B= -2048, M=1Mil.

The accuracy of determining DNL and INL for each code bin k depends on the number of samples M and on value B. The first estimation of a minimal number of samples M for the required accuracy of DNL and for the full-scale range of ideal ADC can be determined by:

$$M \geq \left| \frac{\ln(-B) - \ln(2^N - 1 - B)}{\varepsilon\left(\ln(2^N - B) - \ln(2^N - 1 - B)\right)} \right| , \qquad (5)$$

where ε is the minimal required uncertainty of DNL in LSB. One example of simulation is shown in Fig.3.

## EXPERIMENTAL RESULTS

The first experiments with the proposed method were published in [7], where the method was verify at testing of 12bit ADC embedded on the microcontroller ADuC812 [8]. A huge number of samples acquired from single exponential pulse was needed for the full-scale range testing. It requires large values of C, R, $f_S$ and input impedance of tested ADC. In other to achieve similar occurrence the full-scale range was divided into some subranges. They were separately tested by the stimulus signals with the different time constants. The final DNL and INL for full-scale range was built from these particular DNLs. The main disadvantage of such process, which degrades the achieved results, is a "smoothing" in INL of tested ADC (Fig.6b and Fig.8 in [7]). The difference between DNLs was not notable (Fig.6a and Fig.8a in [7]).

The next testing was perform on the plug-in-board LAB-PC-1200 by National Instrument which provides 12bit ADC with four times higher sampling frequency (100kHz) and the input range is 0-10V (full-scale range). The components of the stimulus signal generator were: C= 10μF / 100V type 373 MKT,
R= 1M2,
$U_{DC}$= -9V,
$U_{ST}$= 11V / 15V (overvoltage protection of ADC board is ±35V).

The proposed test method was assessed by testing the DNL and INL of the ADC under test by both standardized methods [1], [2], [3] – static (Fig.4 and Fig.5) as well as dynamic one (Fig.6 and Fig.7). The static testing took 30 hours and the dynamic one just a few minutes.

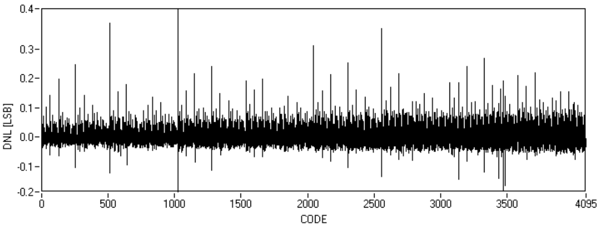


Fig.4. DNL of LAB-PC-1200- static testing method.

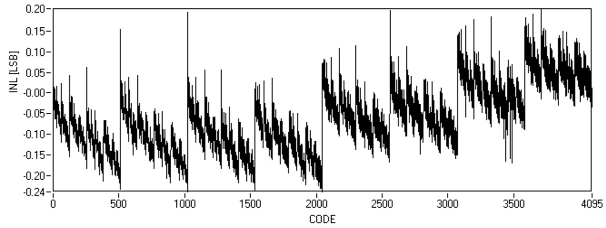


Fig.5. INL of LAB-PC-1200- static testing method.

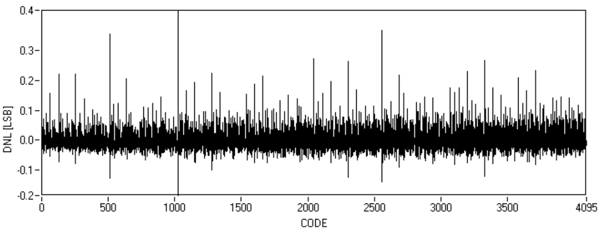


Fig.6. DNL of LAB-PC-1200 - dynamic testing method. $f_{in}$=137.777Hz, M=4Mil.

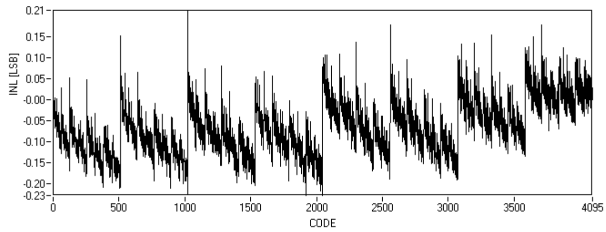


Fig.7. INL of LAB-PC-1200 - dynamic testing method. $f_{in}$=137.777Hz, M=4Mil.

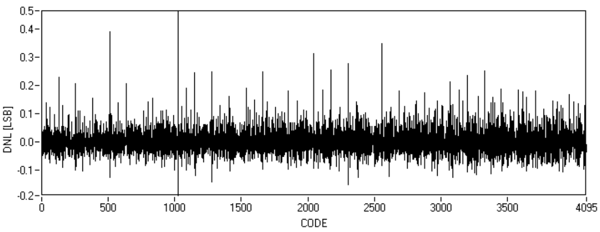


Fig.8. DNL of LAB-PC-1200 – tested by histogram of the exponential testing voltage. $U_{ST}$=11V, $U_{DC}$= -9V, M=1Mil, 1exponential.

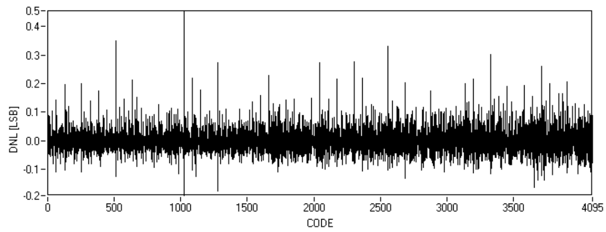


Fig.9. DNL of LAB-PC-1200 – tested by histogram of the exponential testing voltage. $U_{ST}$=15V, $U_{DC}$= -9V, M=1Mil, 1exponential.

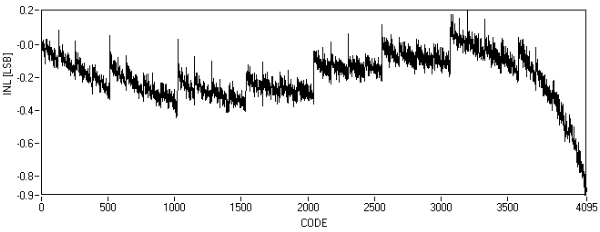


Fig.10. INL of LAB-PC-1200 – obtained from DNL in the case of one exponential component. $U_{ST}$=11V, $U_{DC}$= -9V, M=1Mil.

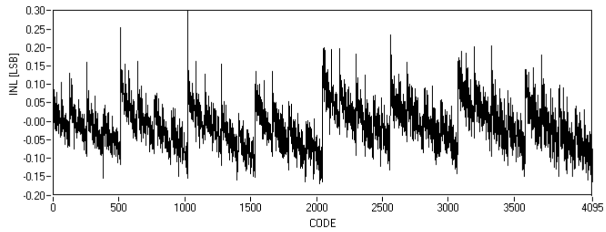


Fig.11. INL of LAB-PC-1200 – obtained from DNL in the case of one exponential component. $U_{ST}$=15V, $U_{DC}$= -9V, M=1Mil.

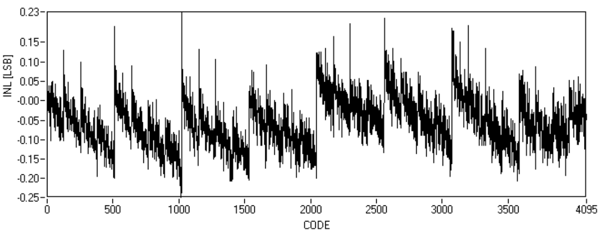


Fig.12. INL of LAB-PC-1200 – obtained from DNL in the case of two exponential components. $U_{ST}$=11V, $U_{DC}$= -9V, M=1Mil.

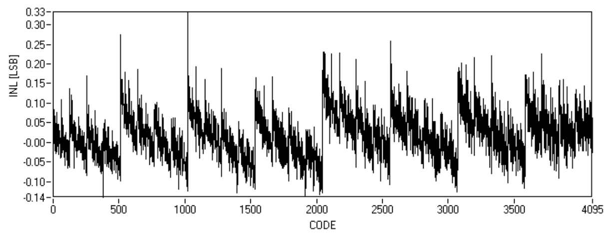


Fig.13. INL of LAB-PC-1200 – obtained from DNL in the case of two exponential components. $U_{ST}$=15V, $U_{DC}$= -9V, M=1Mil.

Fig.8 and Fig.10 show the results of the first test with the exponential stimulus signal, where $U_{ST}$=11V. The form of INL and acquired data indicate that the generated stimulus signal is not ideal, but contains at least two exponential components. This impurity is dependent on the capacitor quality. The presence of the particular exponential components is being caused by dielectric absorption of the capacitor. Increasing value of $U_{ST}$ will cause the reduction of the mentioned impurity of stimulus signal (Fig.11 where $U_{ST}$=15V). This change is not so visible in the DNL shape (Fig.9). Such a change of voltage is not commonly usable because the too high overvoltage can destroy ADC. Authors proposed another way how to avoid drawback of such shape based on fitting the acquired data by the function, which contains two exponential functions. The approximation algorithm is more complicated and time-exacting. The accuracy of calculation of DNL and INL depends on identification and separation of the exponential curves. In this case there is no analytic expression for the ideal number of histogram samples $H_{id}(k)$. After the identification of all parameters of the ideal stimulus signal, samples of the ideal signal are calculated and the ideal histogram $H_{id}(k)$ is found from them. Fig.12 and Fig.13 show INL using the approximation with two exponential curves. The similarity of obtained INL curves with the reference curves shown in Fig.5 and Fig.7 is higher. The differences in DNL are not notable.

## CONCLUSIONS

The original method was proposed. It is based on histogram method, which employs an exponential stimulus signal for ADC differential and integral nonlinearity testing. The exponential testing signal is easy to generate and allows to achieve high suppression of interfering sources. The idealized test signal is approximated from the ADC output flux by best-fitted exponential function. The main problem is in exponential purity of the generated test signal. The stimulus signal contains two and more exponential curves, which degrade the accuracy of DNL and INL determination. The necessity of large values of the capacitor and the resistance for obtaining large set of the tested samples could be avoid by repetition of exponential pulses (Fig.14) or using the operational amplifier in the generator circuit (Fig.15) for amplifying the part of the exponential shape, which has the best purity and coherence with (3).

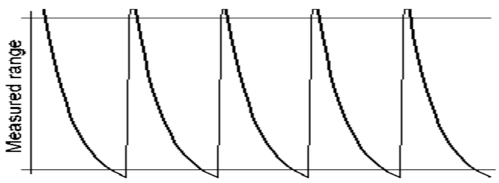

Fig.14. Periodical exponential stimulus signal.

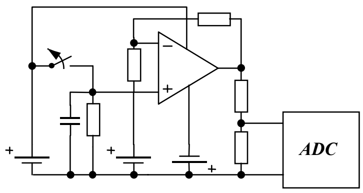

Fig.15. Generator of the exponential stimulus signal with operational amplifier.

The comparison of the proposed testing by exponential voltage with the standardized static method and the histogram method for harmonic stimulus signal showed the insufficient coherence for 12bit ADC. The uncertainty caused by not exact knowledge of exponential components prefer implementation of proposed method for testing fast ADCs with lower resolution.

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