ADC and DAC Modelling and Testing
State of the Art

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Abstract- The analog to digital front ends of measuring instruments affect crucially the interpretation of the signals acquired from the real world into the digital domain and their back presentation. The signal processing in the digital domain due to its stability meets usually the requirements on the uncertainty of the measuring instruments easily. ADCs and DACs influence dominantly the accuracy of instruments and limit the signal dynamic and their applicability. The exact error description and standardised testing methods are required by the end user. Moreover, the simplification of the error description by dominant error parameters is a permanent task for metrologist and producers. This paper is aimed at providing a metrological overview of ADC and DAC topics by referring to their: i) architectures, ii) modelling and testing, and iii) standardization.

I. INTRODUCTION

A. ADC core component of the digital instruments

Analogue-to-Digital Converters (ADCs) play a very important role in the different applications of electronic systems. In fact, at present, most part of the signal processing performed in electronic instruments is becoming digital, and the role of ADCs placed at the boundary of the digital domain acquires a particular relevance, since the signal degradation introduced by these components could be recovered by subsequent processing only if the information of its error behaviours is known.
Digital computing power has exponentially increased at ever smaller incremental costs. However, the real world still is and will always continue to be a fundamentally analogue place. To bring digital processing and its benefits to bear on real-world applications, the analogue signal of interest must be translated into a format that a digital computer can utilize.

B. Concept of modern instruments

The general block scheme of any digital instruments includes Analog-to-Digital Converters at the output of an analog conditioning block which represents the instrument's analog front end. The digital output from the ADC is usually processed in a digital signal processor according to the task to be performed by the instrument. The analog front end presents a transfer characteristic similar to the stepwise characteristic of the ADC and it can be considered as a generalised AD converter. Similarly the conversion from the digital domain into analog is manly impacted by the utilised digital to analog converter (DAC). Hereinafter modelling, testing and error correction handled for a single ADC or DAC are the same as for whole interfacing systems containing analog pre or post processing blocks. Nowadays, characterization and testing activities are a major factor of cost in integrated circuit (IC) manufacturing. In fact, testing mixed-signal circuits may cover nearly 50% of the whole production budget [1].
The main information about the ADC behaviour is contained in the vector of the transition code levels $T[k]$. For each code bin value k the performance behaviour can be described by $T[k]$, by the integral non linearity $INL[k]$ or by the differential non linearity $DNL[k]$ which are analytically linked [2, 3]. Integral parameters describe by simple numbers the global metrological features of ADCs. Effective number of bits (ENOB) or signal to noise and distortion ratio (SINAD), are examples of this group of parameters. ADCs and DACs require for their complete characterisation an extremely high number of

parameters, however end users usually take into account only some of them. Error models describe by a simple way properties of ADCs and DACs under various dynamic conditions, with a reduced set of parameters. The identified error model gives users concise information about the whole system convenient not only for their metrological description but also for the signal processing algorithms performing error reduction.

II. ADC Models

A. Quantization model

An ideal transfer characteristic is described by an ideal stair like transfer characteristic with singularities of the first order at the transition code levels T(k). Mathematically the transfer function can be described for unipolar and bipolar ADC, by Sign+Mag code through

$$T[k] = \text{round}\left[\frac{x}{Q}\right]; \ T[k] = 1.\text{sign}(x) + \text{round}\left[\frac{|x| + 0,5.Q}{Q}\right] \tag{1}$$

where x is the analog input signal, k its corresponding representation in the digital domain and Q is ideal code bin width. *Quantization models* allow the study of the effects of the ideal quantisation noise, dithering and digital post processing targeted on the quantization noise reduction.

B. ADC error models

As mentioned before ADC models are devoted dominantly to the metrological description of error behaviour. Moreover, apart from their final aims, frequently the ADC error models are influenced by the conversion mechanism and influence by inherent error sources inside the architecture. The relative strength of a particular error source depends on the utilised technology. *The architecture-dependent error models* are classified according to circuit abstraction level as *the electrical models (i) the macromodels (ii) and the signal processing models (iii).*
Electrical models details ADC metrological behaviour at the level of real electronic components utilised in the structure. Description of the ADC circuit in the PSPICE environment offers such model. However the error macromodel has weaker link to the circuit layout, its structure contain dominant error sources and the relation among them are expressed by the electrical equivalent circuits. ADC error macromodels analyse the ADC behaviour through electrical equivalent circuits, simpler then the complete electrical models (Fig.1). Electrical models or macromodels can be analysed in circuit simulating programmes (PSPICE, Cadence, etc.).
Applicability of the electrical models is limited by the lack of information about chip layout and accurate models of the utilised components and only component producers could design it and offer it to end users. On the other hand simpler macromodels requires from their designer experience in the finding a suitable equivalent topology without losing significant information on the real ADC metrological behaviours.
Signal processing models (Fig.2). describe by the signal processing blocks the signal flux during the conversion, including the dominant effects impacting the metrological properties. A model is a graphical representation of a process composed of analog input, processing blocks and the output block rounding where the continuous quantity is transformed into digital domain. The structure has a close link to the circuit architecture. Signal processing models are adaptable for transformation into icon-driven simulation software like SIMULINK.
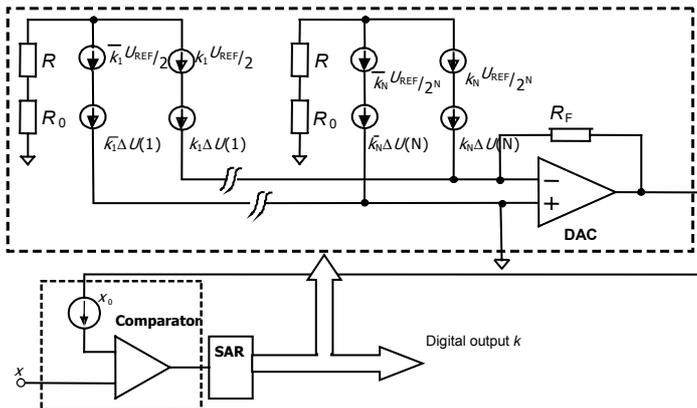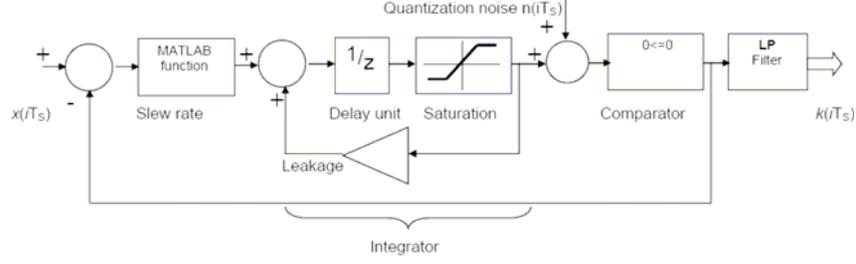

Figure 1. Macromodel of a SAR ADC.

Figure 2. Signal processing error model of ΣΔ ADC.

A behavioural model can be represented by *the memorised functional error parameters (i)* and *the mathematical model (ii)*.

The first type of the behavioural models utilises look-up table or associative memories. While the look-up table based model is represented by a vector of the measured functional error parameters $E(k)$ for any code bin k the associative memory is implemented on artificial neural network (ANN) [4]. The ANN is being programmed in the training phase to achieve for every code bin k the corresponding value of the functional error parameter $E(k)$ acquired from the real converter during the testing phase. The ANN structure and the weights of the synopsis records the metrological behaviour of the ADC. The model accuracy is in the trade of the complexity of the ANN structure. In the contrary, a look-up table is simpler but less robust against the model simplification.

Mathematical models are defined by concise analytical expression where the functional error parameter is explicitly or implicitly related with the code bin k. The number of required parameters $E(k)$ depends on the required accuracy and those parameters are identified by an appropriate testing procedure. The optimal mathematical model is being chosen on the base of the utilised testing strategy. Exampls of mathematical formulas representing ADC error model are:

- polynomial description of functional parameters of different order determined by any optimisation method [5]. Description by the first order regression line requires only two parameters from the testing phase; offset and gain error. Spline, Lagrange and LMS approximations are possibilities to estimate error model from the tested data.

- description of functional parameters by low code frequency (LCF) and high code frequency (HCF) components (Fig.3) [6]

$$INL_m^{LCF}(k) = A_0 + A_1 k + A_2 k^2 + .. + A_L k^L$$

$$INL_m(k) = INL_m^{LCF}(k) + INL_m^{HCF}(k) = INL_m^{LCF}(k) + \sum_{l=1}^{k} DNL_m^{HCF}(l) \qquad (2)$$

- Chebyshev polynomials with the weighting coefficients H_n which are acquired by the FFT (Fig.4) [7]

$$INL_m(k) = \frac{H_0}{2} + \sum_{1}^{\infty} H_n C_n \left(\frac{k.Q}{FS}.2 \right) \qquad (3)$$

where Chebyshev´s polynomials are $C_n(\zeta)=\cos(n.\arccos(\zeta))$.

A classification of error models can be carried out also according to the static or dynamic nature of functional error parameters. Static models characterise the converter for constant or slowly variable input signals whereas dynamic models are used for higher frequency input signal. The dynamic architecture based models are obtained by adding reactive components into circuits or macromodel scheme in the position where they impact dynamic behaviour of the ADC. Similarly, the single blocks in the graphical user interface must be replaced by the blocks describing both static and dynamic behaviours.
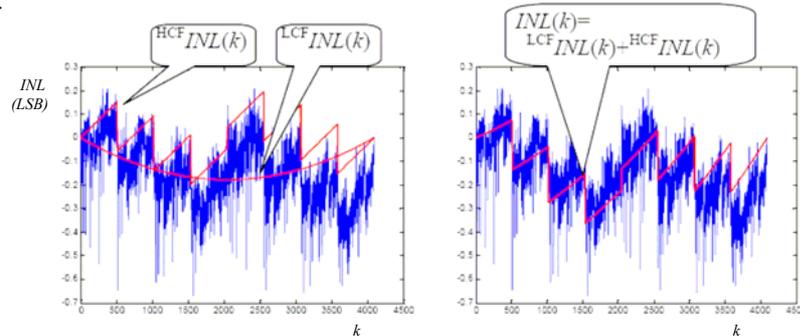

Figure 3. ADC model based on low code frequency (LCF) and high code frequency (HCF) components
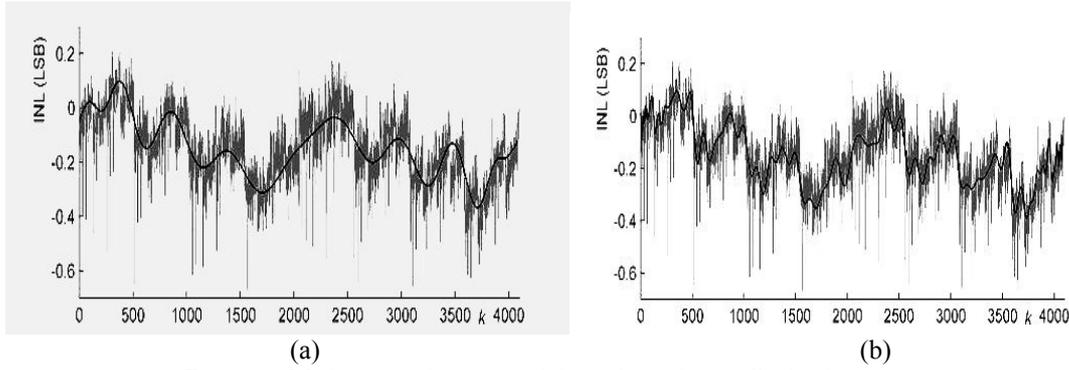
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(a)   (b)

Figure 4. Mathematical error model results utilising Chebyshev series.
Considering only the first 25 terms (a) and considering 100 terms (b).

Dynamic behavioural models represented by look-up tables are an extension of the vector of functional parameters $E(k)$ into two dimensional matrix $E(k,s)$ where s is the slope of the input signal $s = \frac{dx}{dt} = \frac{[k(i)-k(i-1)]}{T_S}$. It is called the phase plane representation and its cross section for $s=0$ is the static behavioural model. For a sinusoidal input signal $Q.k_{max}\cos(i\omega TS)$, of frequency ω the relation between slope s and code bin k is:

$$\left(\frac{s}{\omega}\right)^2 = k_{max}^2 - k^2 \tag{4}$$

Analytically expressed models cover dynamical properties enlarging the description extending the independent parameter code bin k with a second parameter: the signal slope. The polynomial static description is usually changed into Volterra series [8-10]. It models the ADC as a cascade of a linear system with memory followed by m dimensional nonlinear system as function of instant value and the *(I-1)* delayed values of the input signal. The first terms in the series can take into account the nonlinearity of the static characteristic, while the nonlinear effects which arise in the presence of dynamic signals are modelled by the non-linear purely dynamic block depending on the input signal slope $s(i)=x(i)-x(i-1)$. Taking into account the sign of the input signal slope, dynamical model covers requirement of hysteresis. Jitter effects caused by the time noise in the sampling instant are transformed into additive noise [11].

Apart from the knowledge state, the modelling approach can be "*a-priori*" or "*a-posteriori*". The first one exploits available information about architecture and/or conversion principle, whereas the second utilises only the experimental output data [12].

A generalised ADC error model is a cascade of the analog pre-processing block including all the error sources and quantisation model of the ideal ADC (Fig.5). While the analog pre-processing block expressed by structural or behavioural models describes the non-ideal ADC properties including dynamic, the ideal quantisation block describes the discontinuities in the transfer characteristic (Fig.6).
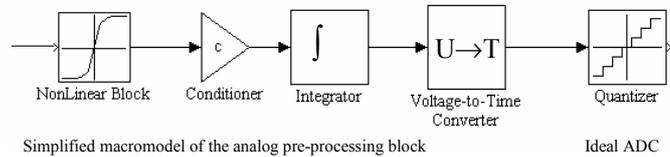

Simplified macromodel of the analog pre-processing block   Ideal ADC

Figure 5. Generalised integrating ADC model using a macromodel for the description of the analog preprocessing block.

Analog pre-processing block
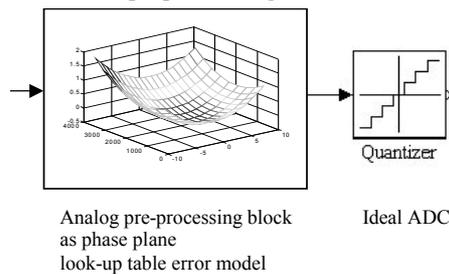as phase plane
look-up table error model   Ideal ADC

Figure 6. Generalised integrating ADC model using phase plane look-up in cascade with an ideal ADC.

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C. DAC modelling

The rapid diffusion of emerging high-performance standards for communication, measurement and entertainment purposes requires DACs with higher speed and accuracy so their design and testing become more challenging [13]. For this reason, the most recent papers concerning DAC modelling deal with simulation for the design, in particular papers proposing behavioural models for the whole device [14] or the nonlinearity only [15], have been found. Moreover architecture-dependent models have been proposed, focusing on current-steering DAC [16].

System and circuit designers, who intend to use the analog conversion components designed by other designers should understand the characteristic of these components. This can be done by using an analog circuit simulator. But due its analog nature and excessive simulation time it still cannot be used to verify the entire system or integrated circuit. So the demand for new modelling technique satisfying the cost and time-effectiveness and versatility under the various simulation environments is increasing in the SOC era.

Two DAC modelling techniques based on principles of wavelet theory are described in [14]. Macro modelling that uses passive components and adders and mathematical equations to depict the wavelet basis functions are proposed. To model the behaviour of DAC using wavelet theory, the output signal of the DAC is analysed in the time and in the frequency domain. The proposed basic block diagram for DAC modelling consists of: i) a glitch generator, ii) a damped sine wave generator, iii) an exponential function generator, and iv) an adder.

In high precision analog circuits it is important to consider the effects of nonlinearities. They can be caused for instance by temperature drift, saturation effects or mismatching between circuit elements as well as process variations. One criterion to describe the worst case nonlinearity of a converter is the INL. The effect of nonlinearities on DAC resolution is studied in [15]. Two models, an exponential and a sinusoidal approach, are proposed to estimate the drop in Signal to Noise Distortion Ratio (SNDR). These models were used to study the performance loss of a multi-bit DAC when used in a frequency synthesizer architecture.

Modern broad-band communication integrated circuits require as fundamental subcircuits DACs exhibiting both high speed and high resolution. A CMOS current-steering DAC is the usual choice for this type of application since that topology best suits these requirements. Several models have been proposed to realize current-steering DAC with better performance. In [16] is demonstrated that the segmentation of the current sources affects the statistical behaviour of the INL and DNL. In [17] a mathematical model that explains the impact of delay differences on the SFDR of a thermometric DAC is proposed. This theoretical analysis shows that the delay differences among the current sources limit the DAC SFDR even when the signal frequency is very low. In the past, dynamic element matching techniques were presented to tackle static mismatch of current-steering DACs. However, little attention was directed to dynamic errors problems. In [18] several implementations to tackle with dynamic errors while avoiding performance degradation due to static error sources are presented. Dynamic errors in current-steering DACs are analysed through a dynamic error model to show that they contribute to nonlinearity in a different way as static mismatch errors.

III. Standard and New ADC testing methods

ADCs are traditionally tested as described in IEEE 1057 [2] and 1241 [3] standards. The development of new faster, cheaper and/or more accurate ADC testing procedures, able to characterize high resolution and high frequency converters is nowadays one important task in Measurement.

The performance of the same converter under different conditions tends to vary, in some cases very strongly, fig.7. Consequently tests should be performed in conditions (input signal frequency and amplitude and sampling frequency) similar to those where they are expected to be used. Fig.7 results show that ADCs performance limit not only the accuracy but also the bandwidth of the instruments where they are included.
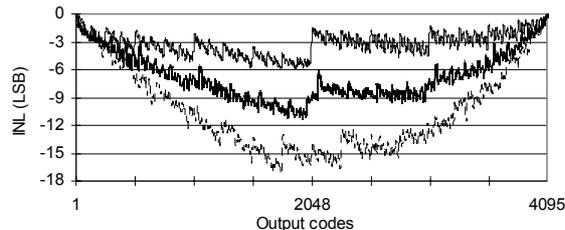

Figure 7. *INL* of a 12 bit ADC, measured by using the traditional histogram test as described in [2] with a sampling frequency of 10 MHz and input sinewaves of 1 kHz, 20 kHz and 60 kHz. |*INL*| increasing for increasing input frequency.

When the converters are to be used to acquire very low frequency signals, the static test is mandatory. In all other cases a dynamic test must be performed. Dynamic tests generally used can be divided in time domain, frequency domain and statistical domain tests. All test procedures present advantages and drawbacks. The main problem with the traditional static test procedure [2] is the unacceptable time duration of the tests for medium and high-resolution converters. The equipment required to test these converters with accuracy better than a small fraction of an LSB is also very expensive and consequently not available in many circumstances. Another problem is the inexistence of input stimulus sources to characterize state of the art very high resolution ADCs.

Regarding the traditional dynamic testing techniques, all of them are based on the use of "ideal" sinusoidal input stimulus (except in what concerns some time base tests). These ideal sources obviously do not exist and the validity of the approximation of considering them ideal will be lost when very high frequency or very high-resolution converters are under test. Other severe problem on these tests is the difficulty to assure coherent sampling in many cases.

A . THE STATIC TEST OF ADCs

Given the large number of low frequency application of ADCs, this is a very important test, both for the industry and the consumers.

Traditionally the test is performed as described in [2]. The transition levels are determined one at a time by applying a constant signal to the ADC input. The value of this stimulus signal is increased until it crosses each transition level, $T[i]$. After each stimulus signal change a set of samples is acquired. The number of acquired samples depends on the standard deviation of noise in the experimental setup (σ_n) and on the required confidence and tolerance levels for the measurement. The value of each transition level is computed from the samples values and from the known values of the applied stimulus signal before and after transition level detection. This procedure is very time consuming because a high number of samples have to be acquired and processed. Furthermore it is necessary to wait for the output of the calibrator that generates the stimulus signal to settle each time it changes. This depends on the calibrator used but can go from a few milliseconds to more than one second. The duration of the test of a 12-bit converter can take several hours. If the sampling frequency is low, or the number of bits of the converter increases, the duration of the test becomes prohibitive. The calibrator used must have an output resolution lower than ¼ of the ideal quantization width, which implies the use of medium to high cost calibrators. The higher the resolution of the converter, the costlier is the equipment necessary. The more recent IEEE 1241 standard [3], introduced a different procedure, in relation to IEEE 1057 std. it is based on the use of a feedback loop, where a DAC generates the feedback signal, applied to the ADC under test. The digital word input of the DAC, is incremented or decremented, depending on the result of the last ADC conversion. M measurements of the input signal of the ADC should be recorded in each step. M should be greater or equal to $2(\sigma_n/\varepsilon)^2$, where ε is the allowable code edge uncertainty. The number of samples to be acquired for each transition level depends on the step size, but it will be always greater than $9+M$. All these samples are acquired at a rate that will be the smaller of the values of the settling time of the DAC and of the desired sampling period. If the settling time is high, the duration of the test will be prohibitive. It can be shown that this procedure is much faster than the static test described in [2] if the settling time of the DAC is low. It is a very good solution if dedicated hardware, containing a fast DAC, is to be used. However it should be avoided if a general-purpose calibrator with a large settling time is considered for ADC input signal generation. The procedure is particularly interesting for high-resolution, low sampling rate ADCs, since in this case the duration of the test is limited by the sampling rate, and the number of acquired samples in this procedure is very low.

A new test that allows the reduction of the test duration and on the possibility of the use of low cost equipment to perform the static test was recently developed [19-21] and included in the new IEC standard 62008 [22]. It is based on the use of small amplitude triangular waves with variable DC levels as stimulus signal for the static test, see fig. 8. This procedure is based in the traditional Histogram Method [23] but uses a uniformly distributed input signal that scans the ADC input range by increasing the DC level by steps.

The procedure requires several steps (N_s). In each step, a small number of ADC codes are stimulated repetitively via small triangular waves. The shape of the stimulus signal is always the same in every step, but the DC level is changed from step to step.

As in the traditional histogram test, the ADC is overdriven in order to stimulate all the codes and to exclude the samples corrupted by noise in the extremities of the stimulus signal [2]. In the case of a triangular stimulus signal, the samples in the extremity have to be excluded also to avoid distortions due to the discontinuity in the signal derivative.
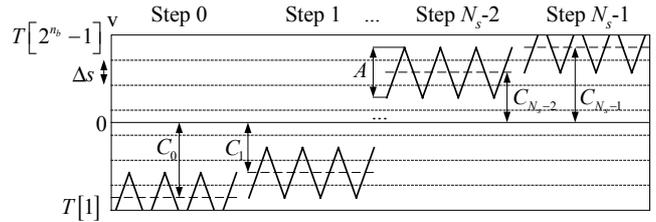
Figure 8. Stimulus signal applied to the ADC in the new IEC 62008 standardised test.

For all the codes stimulated by each of the small triangular waves, the DNL is calculated according to the histogram test procedure. The transition levels are estimated from the DNL values. Gain and the offset errors are corrected, and the final DNL and the INL vectors are computed.

This new procedure for the static test of ADCs reduces dramatically the duration of the test and allows the use of low cost equipment. The time duration of the test is reduced because the number of changes in the DC level generator is dramatically reduced, 80 to 100 changes are the maximum number of changes needed in any ADC. In many cases, good results are achieved with a much lower number of steps. This means that for instance for a 12-bit ADC the waiting time for the calibrator to settle is reduced from 4×4096 to 80-100, i.e. a reduction of about 200 to 1! Another reason for the reduction of the test duration comes from the use of all acquired samples to compute all transition levels, it must be noted that in the traditional static tests [2, 3] only a very small number of all acquired samples are actually used to determine the value of each transition level, and that after the computation of each level, all the previously acquired samples are discharged.

Figure 9 presents the results of the traditional static test, performed as described in [2] for a 12 bit data acquisition board. The rms noise level of the experimental setup was estimated to be 0.2LSB. The acquisition of records with 4096 samples assures an accuracy of 0.012LSB for the INL.
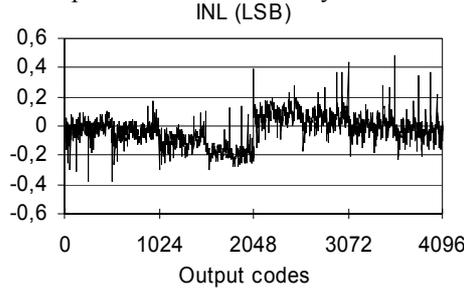

Figure 9. Results of the IEEE 1057-94 standard static test of a 12-bit data acquisition board

In [21] it was shown that a triangular generator with a poor nonlinearity was capable of performing the test if the input range is divided into a convenient number of intervals. A test was performed by acquiring a total of 20 million samples leading to an uncertainty in the INL results lower than 0.01LSB with 99.5% confidence. The difference between the results of the INL obtained with the histogram test and those obtained with the static test ($\Delta\text{INL} = \text{INL}_{\text{histogram test}} - \text{INL}_{\text{static test}}$) is shown in Fig. 10.

The error introduced in the INL by the poor nonlinearity of the generator in the case of a full-scale triangular wave had a maximum value of 3.5LSB. It was reduced to 0.0175LSB as can be seen in the central part of the INLs difference (ΔINL) in figure 10. The higher values of ΔINL, in fig. 10, for lower and higher codes are due to the decrease of accuracy of the traditional static test, due to the increase of the rms value of noise generated in the calibrator used as DC input stimulus, due to the change of its output circuitry for different output ranges. A significant reduction of the testing time in relation to the static test was achieved. The traditional static test in fig. 9 took approximately 6 hours and the test with the new method took only about 5 minutes.
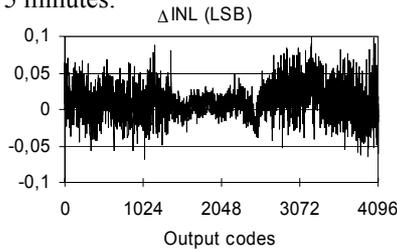

Figure 10. INL difference of the small amplitude waves test results with 200 triangular waves and the traditional the static test results of Figure 9.

The main drawback of this test arises from the acquisition of a small number of samples per period when the input signal frequency approaches the sampling frequency. This procedure is not, in its present form, suited for the dynamic test of ADCs since the small amplitude of the stimulus signal to use makes difficult the generation of a stimulus signal with sufficiently high slope to approach dynamic conditions.

B. DYNAMIC TEST OF ADCs

The histogram method [2, 23] is the test procedure usually used to extract the stationary dynamic transfer function of ADCs. It is based on the comparison of the known probability density function (*pdf*) of a repetitive dynamic input signal applied to the ADC and the distribution of codes at its output Due to the practical difficulty of achieving economically accurate ramp or triangular wave generators, which would allow working with uniform *pdf*s, the sinusoid has become the stimulus signal for this test. The output codes distribution is compared with the theoretical sinusoid *pdf,* the *DNL* is computed and therefore INL and the transfer characteristic are derived. The equation traditionally used to compute the code transition levels in a sinewave histogram test is

$$T_{j+1} = O - A\cos\left(\pi\frac{HC_j}{M}\right) \tag{5}$$

where *A* is the amplitude and *O* the offset of the input stimulus signal, HC_j the experimental cumulative histogram for code j and M the total number of acquired samples. Using (5), the accuracy on the evaluation of the code transition levels is "only" dependent of the spectral purity of the input sinewave and of the knowledge of its amplitude and offset.

Figure 11, shows experimental results of the histogram test performed in a 12 bit ADC. It represents the number of occurrences of each code as a function of the digital output codes and consequently corresponds to trend of the sinusoid pdf, plus the influence of the ADC nonlinearity (which is what we want to measure) and the unwanted, but unavoidable influence of additive and phase noise, of the finite number of acquired samples, of the incoherent sampling resulting from relative frequency errors between the input and sampling frequencies and from the lack of spectral purity in the supposedly sinusoidal input stimulus. From the results in figure 11 and the use of equation (5), one of the *INL* curves presented in figure 7 was computed and from this last the transfer function can be obtained.

In order to decrease the error induced by additive noise in transition levels determination, the input sinusoid must present an amplitude greater than the ADC end of scale limits [2, 23]. This overdrive depends on the required tolerance and confidence levels for *DNL* and *INL* determination. The tolerance level (*B*) is measured in LSBs and the confidence level (*v*) is a probabilistic value. For transition code levels measurement they are related by

$$P\{T_t - BQ \le T_m \le T_t + BQ\} \ge 1 - v \tag{6}$$

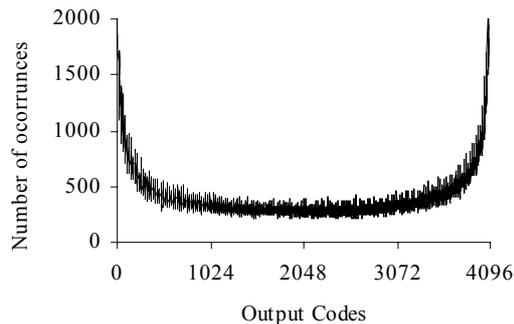where T_t and T_m stand respectively for the true and the measured values of the transition voltages.

Fig. 11. Experimental results of a histogram test of a 12-bit ADC stimulated by a sinewave as described in [2], the total number of acquired samples was 1.7×10^6 .

The total number of samples to be acquired during the histogram test depend on the noise level in the measurement system, on the required tolerance and confidence levels and is different if they are defined for *DNL* (quantization interval) or for *INL* (transition levels) determination. The number of samples depends also on the specification of tolerance for an individual transition level or code bin width, or for the worst case in all range. Expressions to compute the total number of samples and the amount of overdrive in the histogram test can be found in [2, 23].

In any dynamic test f ADCs, stimulated by a sinusoid, the input signal frequency (f_{in}) must be selected in order to assure that for the chosen sampling frequency (f_s) the M acquired samples are uniformly distributed between 0 and 2π. This will happen if

$$f_{in} = \left(\frac{J}{M}\right)f_s \qquad (7)$$

where J is an integer, prime in relation to M. This way M e J don't present any common factors and consequently exactly J periods of the input signal are contained in the M acquired samples. If M is a power of two, then any odd value for J meets the relatively-prime condition.

The accuracy required of the signal frequency depends very strongly on the frequency and depends also on whether the frequency deviation is in the positive or negative direction from the nominal value. In many practical situations the condition of equation 7 is very difficult to achieve.

The use of a statistically defined electrical stimulus signal for the histogram test, like Gaussian noise, was proposed in [37, 38]. When Gaussian noise is used as stimulus signal of the histogram test, code transition levels are computed through [37]:

$$T_{i+1} = \sqrt{2}\sigma_R \, erf^{-1}\left(2HC_i - 1\right) + \mu_R \qquad (8)$$

where σ_R and μ_R are the standard deviation and the mean of the noise stimulus and *erf* is the error function.

The standard deviation of the input noise to be used as stimulus signal in this test cannot be arbitrary for two reasons: (i) it must be such as to excite all levels of the converter; (ii) as shown in [37], an optimum value exists that minimizes the required number of samples for a given pair of tolerance/confidence (B/v) levels in the measurement of INL and DNL vectors. In [37] an expression for the number of required samples was derived.

The use of Gaussian noise as stimulus signal presents the following advantages:
(i) only the first order statistics are relevant for the characterization; (ii) a noise wave is as easy as or easier to generate than a sine wave, especially when high resolution or high frequency converters are under test; (iii) noise in the test ensemble will only add its variance to the noise of the generator, as long as both possess normal distribution; (iv) noise is not periodic, thus not requiring hard to implement sampling schemes. Apart from that, the use of Gaussian noise should be considered in those cases where the ADC is expected to acquire signal with a *pdf* similar to that of random noise. It is the case for instance of audio signals. Converters for use in digital radio or on modern digital communication systems should be tested with such a stimulus. It is well know that ADCs exhibits in many cases nonlinearities dependent of the input signal *pdf* as a consequence of localised heating effects in ADC integrated circuits, the use of a sinusoidal wave as input signal for the test, with *pdf* maximums in the input range limits will lead to different results of those obtained with waves presenting *pdf* maximums in the central part of the range

Caution must be taken in order to avoid device damage by high input signal amplitude when this stimulus signal is used. In fact, due to the nature of normal distributed noise, a high variance implies the existence of a finite probability for the occurrence of potentially damaging levels. Consequently, a limiting circuit must be included (except in the cases where noise is originated in a pseudo-random digital sequence) that does not distort the input signal normal *pdf* within all the input ADC range.

DFT and sine fitting tests are used in fast dynamic tests of ADCs. Traditionally they are used to measure noise, signal to noise and distortion ratio and ENOB [2, 3]. More recently they were proposed to obtain the INL, the DNL and the transfer function of ADCs, namely when they present a hysteric behaviour [6, 7, 39].

C. DAC Testing

Due to the exponential growth in DAC internal complexity there is a major increment in testing time and equipment cost. In order to reduce the total time necessary to carry out the static testing of a given N-bit DAC, parameters should be estimated by measuring the analog outputs corresponding only to a suitable subset of all possible 2^N input codes. However, a reduction in the number of input test vectors requires the definition of appropriate mathematical models able of describing the influence of each elementary part of a given DAC architecture on its actual output voltages [24]. Once this data is known, the static testing efficiency can be improved by selecting only the input codes that enable the estimation of the most significant errors of the DAC. Interesting methods have been proposed to minimize the number of input codes aimed at testing both specific device families [25] (Fig. 11) and basic DAC schemes [26]. A more general approach is proposed and justified in [13].

Concerning BIST schemes for testing static parameters, they follow three approaches. In the first approach, suggested in [27], tests are performed to check if any of the errors exceed the ±0.5 LSB
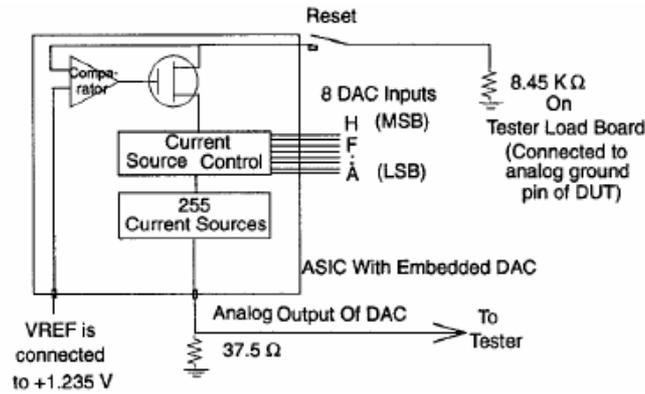
Figure 11. DAC Block diagram.

bounds. This scheme uses multiple voltage references and a precision gain amplifier. In [28] a variable gain amplifier is introduced to amplify different codes to the same level and then compare it with a single reference. The second approach is to use the DAC in a feedback loop. In the scheme proposed in [29], the input to the DAC in the feedback path of a Σ-Δ modulator is switched between two codes with opposite signs. Static errors are inferred from the average value of the output, measured using an up/down counter. In [30] a scheme is proposed whereby the output of the DAC used in a successive approximation. In the third approach, a high frequency clock is used and static parameters are measured in terms of the number of clock cycles. In the scheme proposed in [31], the time taken by a linear ramp to cross the two consecutive levels is considered as a measure of corresponding step. In [32] the DAC output voltage to control a VCO and obtain errors in terms of the frequency shift is used. In [33], a modification of the scheme, which reduces the linearity requirements of the VCO is proposed.

D. Standardisation progress with the scope of the ADC&DAC modelling and testing

Metrological characterisation of ADCs and DACs is not feasible on national or private level. In fact, metrology is a global task, and relevant organisations like IMEKO and IEEE are aware of the need to start manifold research activities in the digitising field. The International Measurement Confederation (IMEKO) is devoted to metrology and measurement with worldwide membership. On the other hand, actual research work of relevance is known from the IEEE TC-10 (Waveform Measurements and Analysis Committee). An European standardization work in ADC and DAC field was born in the IMEKO TC-4 Working Group on A/D and D/A Converter Metrology, and takes actively part in the IEEE TC-10 work for creating a unified terminology and test methods for analogue-to-digital converters. IEEE 1241 does not cover all aspects and also does not meet all needs formulated worldwide and defined by the IMEKO Working Group. Therefore, inside IMEKO TC-4 a network was formed under the name EUPAS, European Project for ADC-based devices Standardization, and which extends over about 20 institutes within 14 European countries (Czech Republic, Estonia, Finland, France, Germany, Hungary, Italy, Poland, Portugal, Russia, Slovak Republic, Spain, UK, Ukraine). The aim is to develop European standards for improving production quality of ADC-based embedded systems, making components and products interchangeable, simplifying test procedures to check conformity.

Due to their numerous features and wide range of application uses, it is very difficult to define a unique way in which DACs can be specified and tested. For this reason it is growing the need for DAC standardization. At the present time the existing main DAC standards are: (i) the IEEE Std. 746 which addresses the testing of Analog-to-Digital and Digital-to-Analog converters, used for PCM television video signal processing [35], (ii) the JEDEC Standard 99, addendum number 1, which deals with the terms and definitions used to describe Analog-to-Digital and Digital-to-Analog converters and does not include test methods [36], and (iii) the EBU Technical Information I15-1998 [37] which reports ADC and DAC performance parameters for testing in conformity with ITU-R Recommendations BT.601 and BT.656. However, it does not exist a standard intended to focus specifically on terms, definitions and test methods for DACs for a wide range of applications as exists for ADC (IEEE Std. 1241 [3]). To solve this problem the Waveform Measurement and Analysis Technical Committee (TC-10) of the IEEE Instrumentation and Measurement Society is working to realize a standard to provide common terminology and test methods for the testing and evaluation of DACs. The information in this standard will be useful both to manufacturers and users of DACs because it will provide a basis for evaluating and comparing existing devices, as well as providing a template for writing specifications for the procurement of new ones. Moreover, in some applications, the information provided by the tests described in this new standard could be used to correct DAC errors.

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