An FPGA Based Peak Detector for Magnetostrictive Current Sensors

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Abstract- The paper describes a FPGA based peak detector. The present design is aimed for signal processing coming from a magnetoresistive current sensor, but it can be used for any kind of signal. The maximum value of the signal is determined using the derivative sign change from positive to negative means positive peak and sign change from negative to positive means negative peak while the signal is positive or respectively negative. Two thresholds are used in order to separate the absolute peak from other relative peaks in the waveform. The peak detection is performed comparing the signal with a threshold and selecting sequences that exceed it for positive maximum or are located under it for negative minimum. The peak value can be directly displayed on a digital display, or transmitted via LPT interface to computer or converted to analog signal again with a D/A converter.

I. Introduction

In many applications is necessary to take over the data with different type of sensors. A wide range of sensors gives the useful information as impulse parameters: amplitude, impulse length, duty cycle, etc. The present design is aimed to process signals that carry the useful information as peak value (for example coming from a current sensor based on magnetostrictive wire, Mateucci effect, like in figure 1). The pulse amplitude, either positive or negative is proportional with the magnetic field along the wire [1]. Nowadays electronics offers few alternatives for peak detection: analog (using diodes and low pass filter) or digital using DSP [1], [2], [3]. Taking into consideration that the pulse length is around 1μs, either analog or hardware digital peak detection must be used. In order to keep the resolution of the A/D converter for the detected amplitude too (12 bits for example), fast A/D converters have to be used. Estimating that, around the peak, the derivative is

$$\frac{du}{dt} \cong 0.012 \quad V/\mu s \tag{1}$$

the sampling frequency must be

$$f_S \geq \frac{du/dt}{1LSB} \tag{2}$$

For 12 bits this leads to 12.3 MHz. For this speed, the best digital solution is the use of an FPGA.

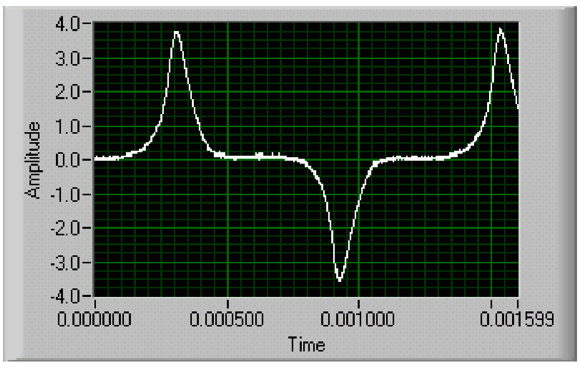

Fig.1. Mateucci voltage waveform

II. System description

In order to get good results for signals with offset, DC analog input has been chosen. The interface is designed for best performance in concordance with the input characteristics of the A/D converter. In order to obtain a good Total Harmonic Distortion (THD) and a Spurious Free Dynamic Range (SFRD) the A/D uses a differential input. The input signal is shifted to a DC point, swinging symmetrically around the supply middle voltage (figure 2) [4].

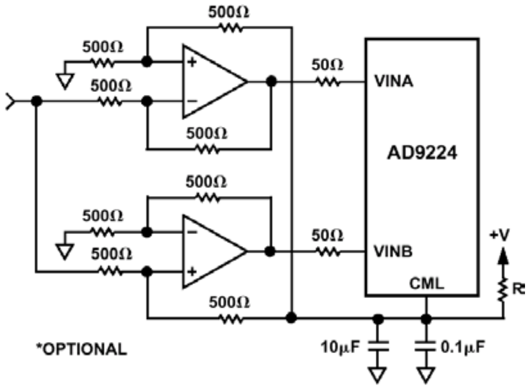

Figure 2. Schematic of the analog interface and A/DC

One, double, low noise, high speed, voltage feedback amplifier is used (AD8022 [5]) to match the A/DC input range (-2V to +2V). The noise of the amplifier, specified by manufacturer, is 2,5nV/sqrt(Hz). The useful signal is coming directly from the current sensor (figure 3) and it is converted into digital on 12 bits using a fast ADC. It works as fast as 40MHz sampling speed, but the clock signal must not exceed duty cycles between 49% and 51%.

The system's frequency is the same as for the A/D converter. The A/DC delivers the samples with three clocks periods delay, one sample per clock period, and they are sampled into the FPGA on the negative edge of the clock signal. The samples are delivered on parallel interface to the FPGA, on 12 bits bus. The FPGA hosts a hardware DSP, that filters the data stream, determines both positive and negative peak values and delivers the result to the output.

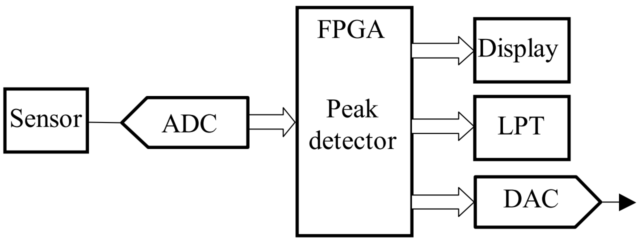

Figure. 3 Data acquisition system – block diagram

The block diagram of the hardware DSP is shown in figure 4 and it is based on a previous design [6]. First the data stream is filtered in order to reduce the high frequency and quantization noise. F is a first order digital filter with a low pass characteristic. The filter is described by the following equation:

$$Y_N=(Y_N+Y_{N-1})/2 \qquad (3)$$

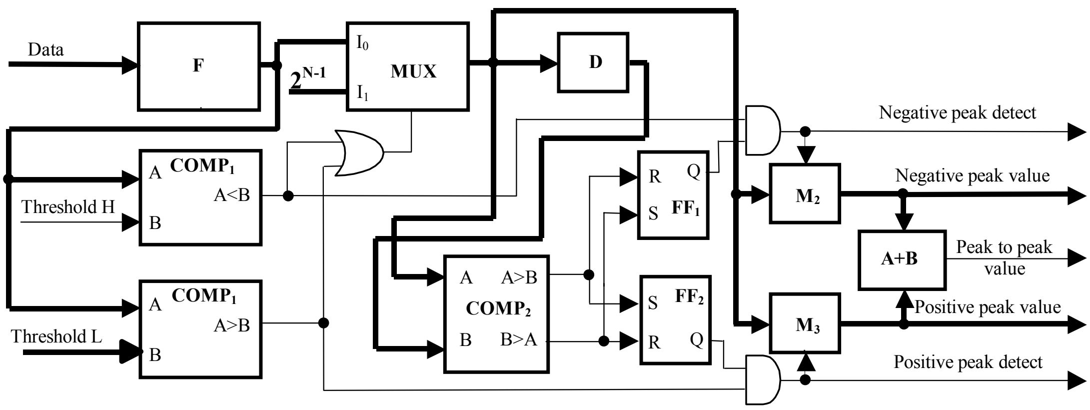

Fig. 3 Peak detector - block diagram

After filter, the "signal" is compared (COMP1) with two thresholds (Threshold H and Threshold L), usually zero for bipolar AC signals without offset, in order to separate the absolute peak from local peaks. DC 0V value is half of the A/DC scale, and for binary shifted code this means 80H. Depending on signal's value, the multiplexer (MUX) will replace the values between thresholds with 80H. Local peaks, either positive or negative will be deleted from the data stream.

The memory M_1 produces a one clock delayed replica of the signal, allowing the comparator ($COMP_2$) to compare two consecutive samples. According to the relation between them the position of the positive peak or respectively of the negative peak can be determined (FF_1 and FF_2). These must be validated by the $COMP_1$ output in order to avoid local maximums or minimums. The peak-to-peak value is also computed (A+B).

The data communication between PC and FPGA is realized through LPT port. Reading 12 bit words on LPT port imply a two-step transfer, because this is an 8 bit wide port. For the writing/reading to/from FPGA 3 control lines are also used. A debouncer is used to remove false transitions of these signals from the LPT.

The peak detector is located in a Flex10k20 programmable logic device from Altera. It uses a number of 141 logic cells from a total of 1152 (approximately 12%). Also the number of Input/Output pins used is less than 20% (33 of 183) and none of the 48 embedded cells. Due to this more processing can be located in the same circuit and other functions can be implemented.

For testing and checking the system, some known signals were acquisitioned. For this, the peak detector has been replaced with a 1024 wide FIFO memory. For 25MHz A/DC clock, a 25kHz signal has been acquired for a full period. Figure 4 presents the waveforms of a sine and sinc signal.

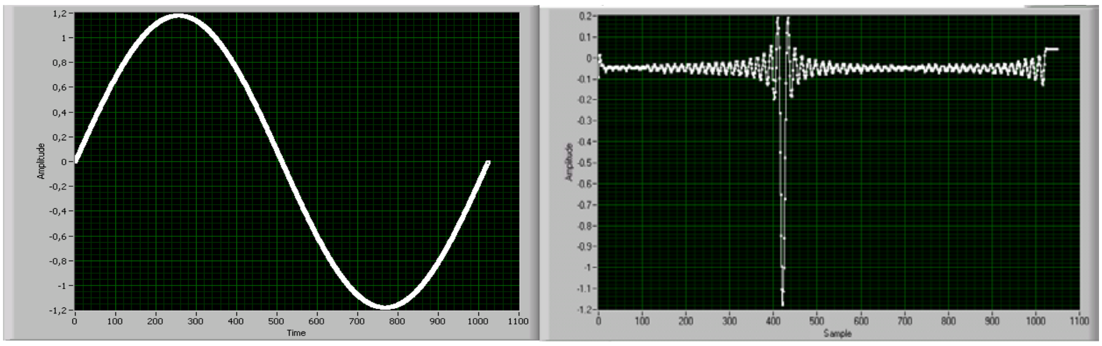

Figure 4 Waveforms acquired with the data acquisition system associated with the peak detector

III. Experimental results

Once the system is working, real verifying of the peak detector can be performed. The known test signal has been produced with a Sony-Tektronix AFG 310 arbitrary waveform generator. For sinus wave, the signal was measured with a Keithley 2000 precision multimeter. Two types of signals were used for testing: a sinc signal (very similar to the signal coming from the current sensor) and a sinusoidal one. For the sinus signal the frequency was varied from 50kHz to 250kHz, and for sinc signal the frequency has been limited to 10 kHz by the generator.

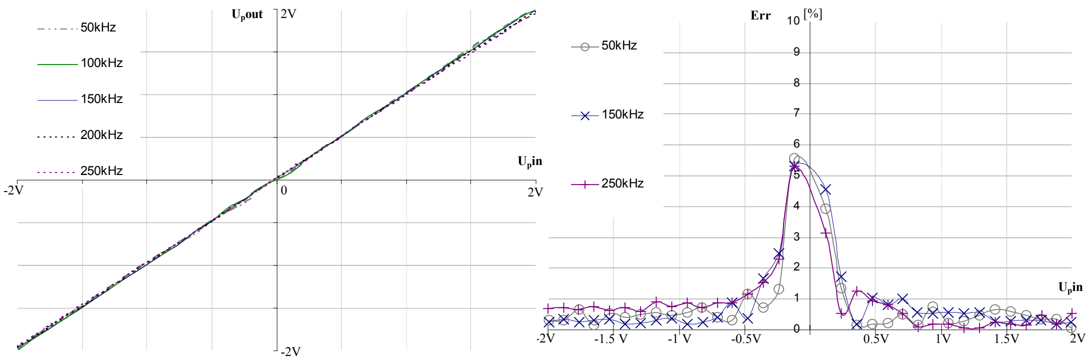

Figure 5 Response and errors for peak detector for sinus wave

For high over-sampling rates (under 100), the response is located under 0.5% (gray curve) in the range 0.5V÷2V). Once the rate is becoming lower, the error is increasing, going towards 1%. Under 0.5V the errors surpass 1%, rising up to 5% around 0V. For frequencies higher than 250kHz, the signal drops due to the amplifier bandwidth.

For sinc waveform the results are similar as it can be seen from figure 6. The errors start to increase under 0.5V. The measurements were performed at 10kHz, the maximum frequency the signal generator could deliver for arbitrary waveforms.

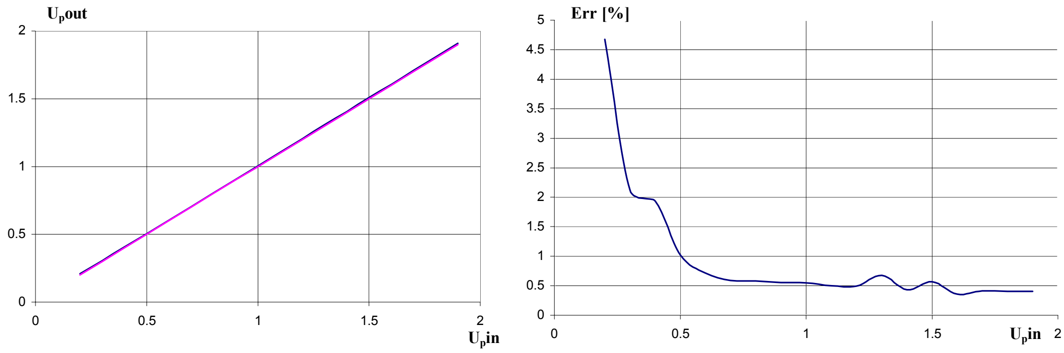

Figure 6 Response and errors for peak detector for sinc wave

IV. Conclusions

A hardware peak detector for high frequency signals has been presented. The main aim is to be used in a current sensor based on magnetostrictive wire. The signal coming from the sensor is the Mateucci voltage (figure 1), whose waveform is similar with a sinc signal. Hardware digital signal processing has been chosen in order to ensure desired resolution and noise cancelling in large bandwidth. The peak detector supplies at its outputs the positive, negative and peak-to-peak values. The available interfaces are 7 segments display, parallel port and analogue output with 12 bits resolution. The frequency range last from 1kHz up to 250KHz, limited by the amplifier and the errors are bound under 0.5% for the last ¾ of the range.

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