A New Analog-to-Digital Converters Differential Nonlinearity Testing Method

Martin Kollár[1], Peter Michalko[2]

[1] *Department of Electrical Engineering and Measurement, Technical university in Košice,Park Komenského 3, phone:* +421-55-602 2579*, fax:* +421 - 55 - 632 39 89 *,Martin.Kollar@tuke.sk*
[2] *Department of Electronics and Multimedia Communications, Technical university in Košice,Park Komenského 13, phone:*+421-55-602 2861*, fax:* +421 - 55 - 632 39 89*,Peter.Michalko@tuke.sk*

Abstract- This paper presents a new approach to static parameters testing of analog-to-digital converters (ADCs). In comparison to ordinary approaches, the measured transition levels are not related to zero potential but to the transition levels of a reference ADC, which is of the same type as a tested ADC. These differences, which can be in the extreme case in the range of a few least significant bits (LSB) of the tested ADC, were measured by a succesive approximation principle-based test system, with a digital-to-analog converter (DAC) in the feedback. A special algorithm has been proposed to control the measurement. The new approach sets no special requirements on the input saw-tooth impulse generator precision and the precision of the obtained differential non-linearity (*DNL*) characteristics mainly depends on the DAC used. Practical measurement results evaluated on data acquisition board Lab-PC-1200 with 12b ADC obtained by new method are compared with common static method results.

I. Introduction

The price of mixed-signal integrated circuits is dominated by the ever-increasing testing cost of the analog blocks and converters. In particular, the full test of an ADC implies the determination of two kinds of parameters, the static errors linked to some deviations of the converter transfer function, and the dynamic features expressing the distortion and noise of the converted signal introduced by the converter. Static errors are generally deduced from a histogram-based test [1] lying on a statistical analysis of the occurrence frequency for each output code, while dynamic parameters are usually evaluated from the spectral distribution of the converted signal, computed using a Fast Fourier Transformation (FFT) [2].

Although the principles of both the static and dynamic tests have been well elaborated [1-3] more work remains to be done on its feasibility issues. The test methods have been originally proposed under the assumption that the input source of reference signal is without uncertainties.

Let us consider the full scale (FS) of a tested 12 bit ADC is in the range of a few V. Then the LSB will be in the range of a few mV. Since, the precision of a signal generator should be at least two orders higher than LSB of the tested ADC [3], in this case the generator absolute error should be in the range of a few hundredths of mV. A serious problem arises when 16 bit ADC is tested, because the generator absolute error should be in the range of a few thousandths of mV.

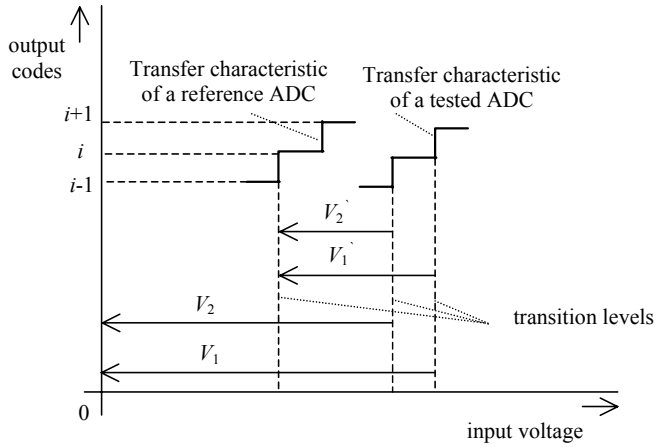


Figure 1 Principle of a new approach in testing ADCs.

To avoid such requirements on high precision of the input generator a new approach will be presented in the following part of this paper. Its originality consists in measuring the decision levels of the tested ADC not to zero potential but to decision levels of a reference ADC. Thus, if the reference ADC is of

the same type as the one to be tested, the maximal measured values will be in the range of a few LSB of the tested ADC.
To be more detailed, let us consider a tested and reference ADCs with an element of transfer characteristic according to Fig.1. By using an ordinary approach, the voltages V_1, V_2 are measured in relation to zero potential, while using a new approach the voltages $V_1^{`}, V_2^{`}$ are measured in relation to a decision level output code i of the reference ADC. In both approaches the voltages can be generated with the same relative error. However, using the new approach leads to the absolute error much smaller than that obtained by the ordinary approach [4].
The principle of this new method including also a possible hardware realization is described in the following sections.

II. New approach in testing ADCs

Fig. 2 shows a complete scheme of the test system. As it can be seen the output codes of a reference and tested ADC are processed in a microprocessor (μP). Also DAC, of which output voltage is added to input of tested ADC through a precise resistive divider R_2/R_1, is controlled by μP. According to Fig.1, by increasing input voltage from saw-tooth impulse generator, because of given transfer characteristics, the output code i at first will be generated by the reference ADC and then, with a time delay, by the tested ADC. However, by adding a voltage from resistive divider R_2/R_1 which is smoothly greater than $V_2^{`}$ the output code i at first will be generated by the tested ADC and then with a time delay by the reference ADC.

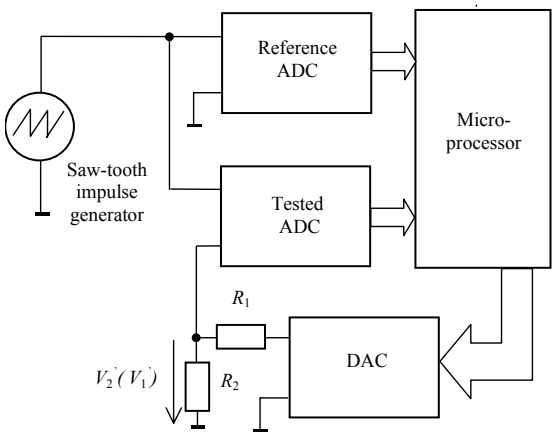


Figure 2. Block diagram of new test method.

To achieve a very short time of measurement of voltage difference $V_2^{`}$, the principle of successive approximation can be used. For example, by using 8 bit DAC the saw-tooth impulse must be generated 8 times by the input generator. During the first impulse, only a decision whether difference voltage is positive or negative is done. In the case of a positive value, which means that output code i at first will be generated by the reference ADC and then with a time delay by the tested ADC, the voltage at resistive divider output will be set to FS/2, where FS is a full scale of the DAC relating to resistive divider output. During the second impulse it is tested by μP whether the reference or tested ADC generates output code i at first. In case that again at first the reference ADC generates output code i, the output voltage of the resistive divider will be set to FS/2+FS/4. In the opposite case this voltage will be set to FS/2-FS/4. Thus, the output voltage of the resistive divider is successively set during the following six cycles. The principle of successive approximation is well known [5] therefore only its summary is made here.
In the same manner difference voltage $V_1^{`}$ is measured. Since, in this case the measurement is related to the decision level of the output code i from the reference ADC and to the decision level of the output code i+1 from the tested ADC, μP tests during each cycle, which one from these output codes is generated as first. From the measured $V_1^{`}, V_2^{`}$, DNL of output code i is calculated using formula [5]

$$DNL(i) = \frac{\left(V_1^{`} - V_2^{`} - LSB\right)}{LSB} \tag{1}$$

where LSB is a value of an ideal least significant bit of the tested (reference) ADC.
From (1) it is clear that the precision of calculated DNL is determined by precision of measured $V_1^{`}$, $V_2^{`}$. Fig.3a shows an example when the difference between actual decision levels of the output code i of the tested and reference ADC is smoothly lower than kT_s, where k is slope of saw-tooth impulse and T_s sampling period. In the moment t_1, output code i-1 is at the output of the reference and tested ADC, while in the moment t_2 there will be the output code i.

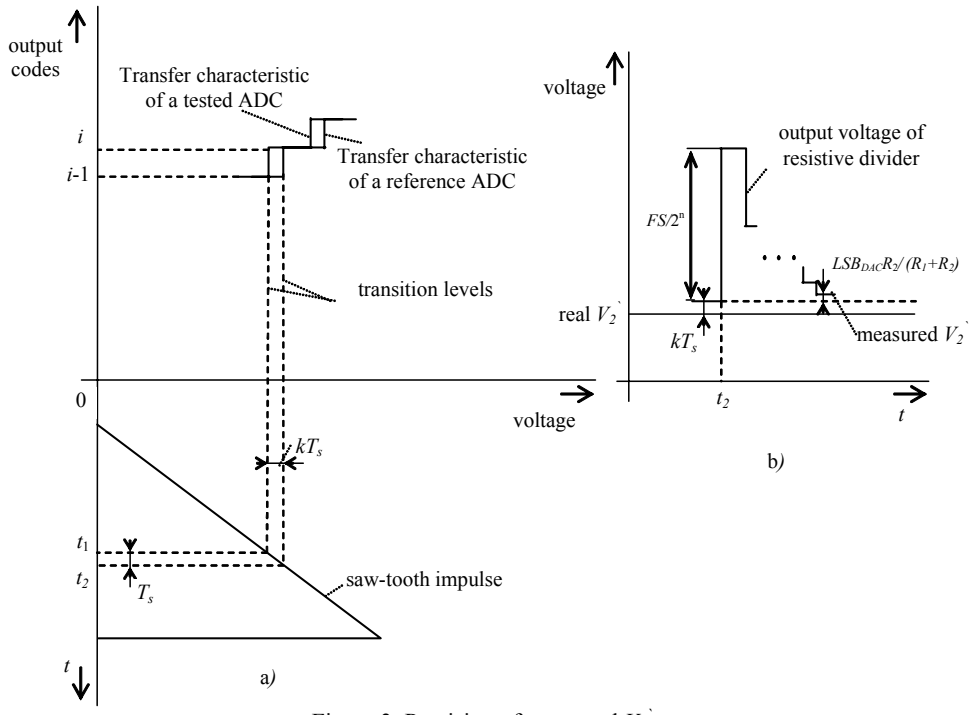


Figure 3. Precision of measured V_2`.

In this case, it is not possible to decide whether the tested code *i* was generated by tested or reference ADC at first. Thus, instead to be decreased, the output voltage of DAC will be increased by value $FS/2^n$, where *n* is an actual step of approximating conversion. In the remaining conversion steps this voltage will be increased with the resolution $LSB_{DAC}.R_2/(R_1+R_2)$, where LSB_{DAC} is the least significant bit of DAC, as shown in Fig. 3b. Therefore the maximal error of measured V_2` is given by formula [4]

$$\Delta_{V_2`} = \left|kT_s\right| + \left|\frac{R_2}{(R_1+R_2)} LSB_{DAC}\right| + \left|\frac{R_2}{(R_1+R_2)} INL_{DAC}\right| \tag{2}$$

In addition, maximal integral non-linearity of DAC was assumed in (2). Since the same error is for measured V_1`, the maximal error of measured DNL is given by formula [4]

$$\Delta = 2\left(\left|kT_s\right| + \left|\frac{R_2}{(R_1+R_2)} LSB_{DAC}\right| + \left|\frac{R_2}{(R_1+R_2)} INL_{DAC}\right|\right) \tag{3}$$

If nominal parameters are such that kT_s is about hundredths of LSB, then an extreme change of slope about 100 % reflects an error $2kT_s$ and thus does not influence markedly the resultant precision.

III. Algorithm for measuring DNL characteristic

As described in the previous section, the difference voltages $V_1`, V_2`$ have to be measured to obtain DNL in the given output code *i.* In this section, an algorithm is described by using of which the complete DNL characteristic is obtained by passing the full scale of the tested and additional ADC *s* times, where *s* is the number of bits of used DAC. By assuming that

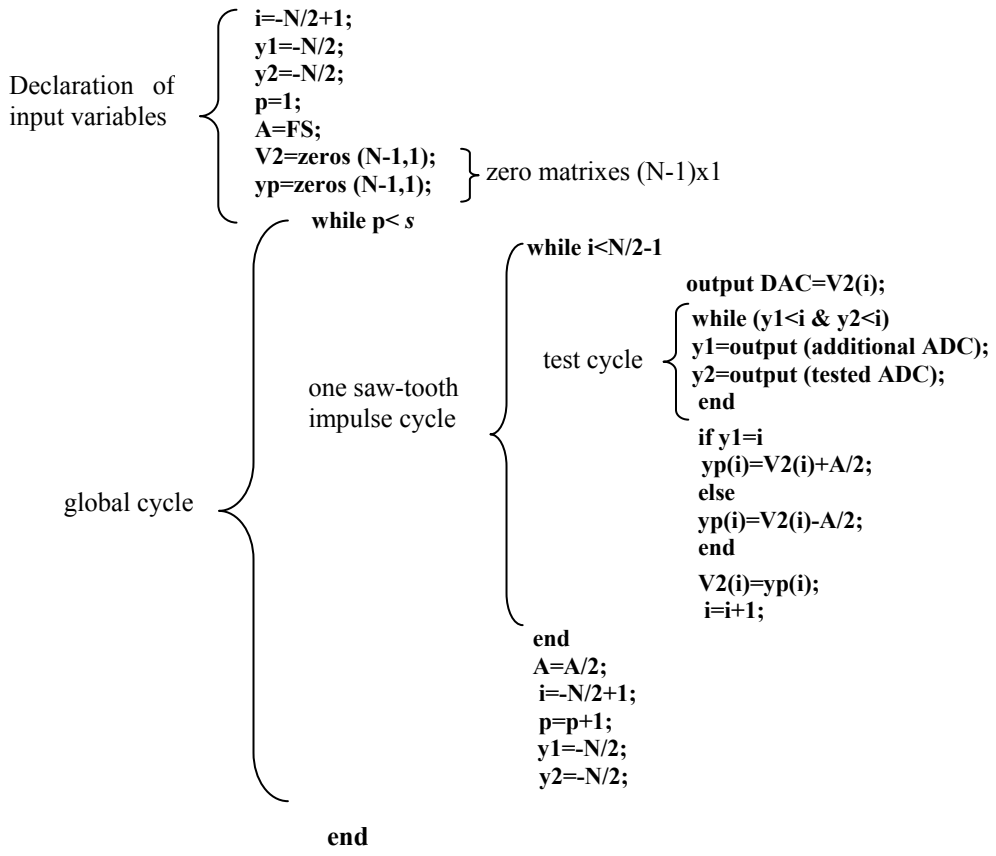
$$\overline{DNL} = \begin{pmatrix} DNL\left(-\frac{N}{2}\right) \\ . \\ . \\ . \\ DNL\left(\frac{N}{2}-1\right) \end{pmatrix}, \tag{4}$$

where *N* is the number of output codes of the tested (reference) ADC, we can write that

$$\overline{DNL} = \left(\overline{V}_1` - \overline{V}_2`\right) / LSB - \overline{E}, \tag{5}$$

where $\overline{V}_1^{`} = \begin{pmatrix} V_1^{`}\left(-\frac{N}{2}\right) \\ . \\ . \\ . \\ V_1^{`}\left(\frac{N}{2}-1\right) \end{pmatrix}$, $\overline{V}_2^{`} = \begin{pmatrix} V_2^{`}\left(-\frac{N}{2}\right) \\ . \\ . \\ . \\ V_2^{`}\left(\frac{N}{2}-1\right) \end{pmatrix}$ and $\overline{E} = \begin{pmatrix} 1 \\ . \\ . \\ . \\ 1 \end{pmatrix}_{(N-1)x1}$.

To measure the vector $\overline{V}_2^{`}$ the following algorithm is to be implemented to μP.



At the beginning, the variables are declared. Into variable **A,** the full scale **FS** of DAC is placed and zero column matrixes **V2**, **yp** are defined. The algorithm contains a global cycle with two embedded cycles. During the test cycle is tested if the output code **i** is at first generated by tested or reference ADC. If, for example, the output code **i** is generated at first by the reference ADC, the output of DAC will be increased by *A*/2 (at the beginning *A=FS*) and this value will be placed into **V2(i).** Then, **i** is incremented and this procedure will be repeated. Thus, from one saw-tooth impulse cycle after 1st step of conversion a vector $\overline{V}_2^{`}$ will be obtained. Then, the variable **A** will be decreased by half and **i** will be set to –N/2+1. The whole procedure will be repeated. The result will be vector $\overline{V}_2^{`}$ after 2nd step of conversion. Like that, after *s* steps of conversion the vector $\overline{V}_2^{`}$ entering the equation (5) will be obtained. To measure the vector $\overline{V}_1^{`}$, the above algorithm has to be implemented in μP, however with the difference that it is tested whether the output code **i** will be generated by the reference ADC or output code **(i+1)** by the tested ADC at first. By means of (5), the complete DNL characteristic is obtained.

IV. Total uncertainty in the estimation of measured DNL

The equation (3) estimates the maximal error in measuring DNL of ADC under test. Since, in practice, the sampling frequency $1/T_s$ is much greater than that of saw tooth impulse, the sampling is never done in the same points during each period of saw tooth impulse. Therefore, the error resulting from non-zero sampling period is random. Let us consider that this error has rectangular probability of

distribution and zero mean. Furthermore, ADCs have their own noise. Its maximal value, covering the probability of about 99.95 %, on data acquisition board Lab-PC-1200 was near to 0.9 LSB, which is two orders higher than quantization error of DAC and an error resulting from non-zero sampling period. Influence of this noise complicates the measurement because the result cannot be obtained form one realization. On the second hand, it can be used for stochastic dithering, where by averaging a set of conversion the quantization error of DAC can be decreased [6]. For stochastic dithering the total uncertainty must be calculated assuming that each original conversion has an independent uncertainty. Using these facts we receive the total uncertainty

$$u = \sqrt{\frac{U_n^2}{K} + \left(\frac{R_2 INL_{DAC}}{(R_1 + R_2)\sqrt{3}} \right)^2} , \tag{6}$$

where U_n is the RMS of the noise and K is the number of averaging. Other source of uncertainty that could be taken into account is the resistive divider. However, because, nowadays the resistive dividers with relative error 0.01 % are standardly produced, this source of uncertainty can be omitted.

V. Experimental results

In order to verify the proposed DNL testing method a testing setup (Fig.4) consisting of two Data Acquisition (DAQ) cards, a saw-tooth impulse generator and two resistors was realized. ADC under test was a 12 bits ADC on LAB-PC-1200 card. DAQ PCI-6014 was utilized for reference ADC, DAC and synchronization generator. The synchronization generator was necessary to determine sampling instant and sampling rate because both ADCs are supposed to sample at the same time moment. A control algorithm and DNL calculation were realized in LabVIEW environment. Maximum achievable sampling rate was only 10kS/s due to sampling frequency of the used DAC. This has increased testing time of one realization to 55 minutes. By increasing the sampling frequency to ones of MHz the testing time of one realization should take less than a minute.

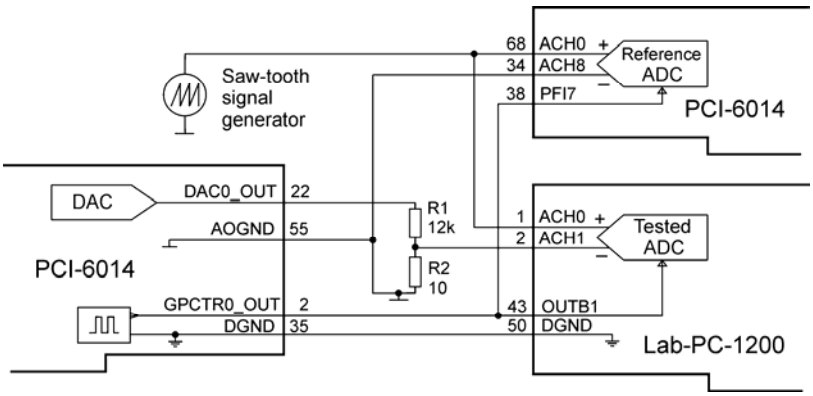


Figure 4. Testing setup for DNL measurement by the proposed method.

As mentioned before, the maximal error is related to the slope k of saw-tooth testing impulse and sampling period T_s. Testing parameters were calculated using equation (3) to achieve Δ=0.01LSB of the tested ADC. The test was performed with the following parameters: f_s=10kHz, s=12, R_1=12kΩ, R_2=10Ω, the parameters of saw-tooth signal were amplitude equal to 10.1V and period 137s.

Testing results are shown in Fig.5. In Fig. 5a, a DNL characteristic obtained by static method is shown. Fig. 5b and 5c present DNL characteristics obtained by using the proposed method for one realization and averaging 10 realizations, respectively. Observed distortions between DNL characteristics in Fig. 5a and 5b are caused by system noise of DAQ card, of which RMS value is 0.3 LSB according to user manual. The DNL characteristic for K=100 is shown in Fig.6a and corresponding absolute error related to static DNL characteristic (Fig. 5a) in Fig. 6c. Fig. 6e shows absolute error histogram. The resultant uncertainty given by equation (6) expresses the metrological reliability of DNL characteristics measurement. In this case equation (6) predicts uncertainty 0.03 LSB while the uncertainty obtained from experimental results was 0.0266 LSB. It should be noted that experimental uncertainty was obtained as standard deviation of characteristic in Fig. 6c.

Equation (6) also shows that in case when the maximal error according to (2) is at least two orders smaller than the RMS of the noise, the error of input saw-tooth signal generator does not markedly influence the resultant uncertainty. To verify it the slope of saw-tooth signal was changed two times, which reflects 100% error in amplitude and measurement results for K=100 are shown in Fig. 6b, 6d, 6f. In this case, the uncertainty obtained from measured data was 0.0271 LSB.

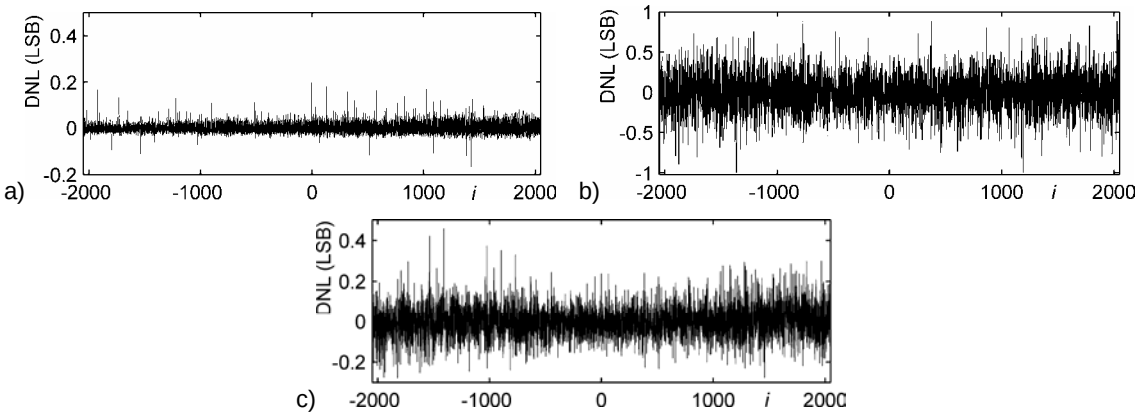


Figure 5. Testing results obtained by a) static method b) proposed method (one realization) c) proposed method (average of 10 realizations).

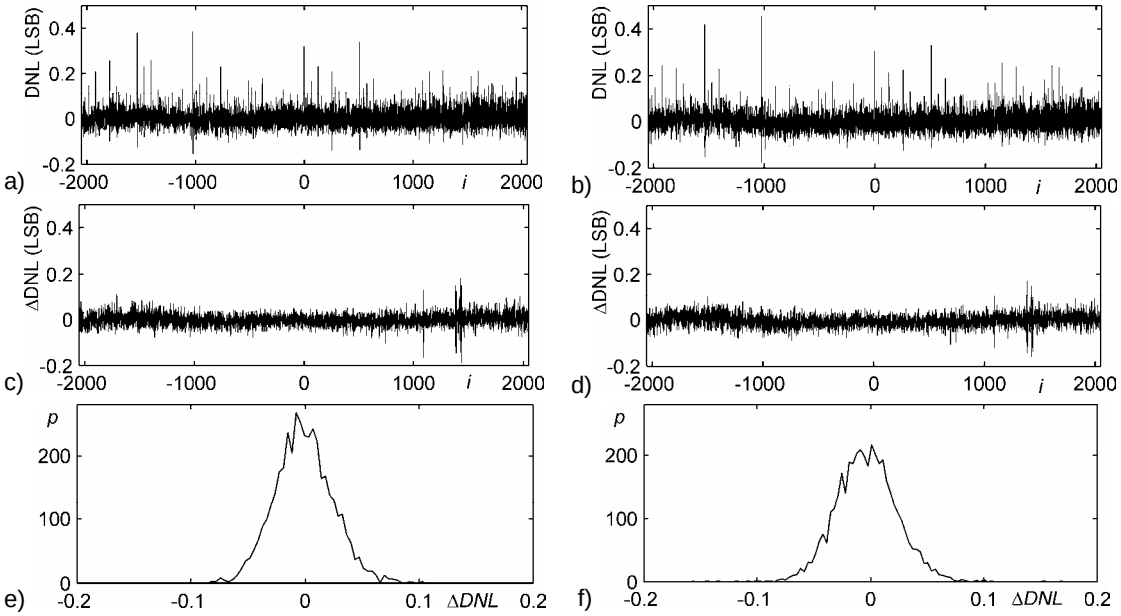


Figure 6. Measured DNL characteristics for a) K=100, k=73.7mV/s b) K=100, k=147.4mV/s, c) corresponding absolute error of a), d) corresponding absolute error of b), e) absolute error histogram of c), f) absolute error histogram of d).

VI. Conclusions

A new DNL testing method has been presented. In comparison with the standard ones, transition levels of tested ADC are not related to zero potential but to the transition levels of a reference ADC. Thus, there are no special requirements on precision of input saw-tooth signal generator. It has been shown that uncertainty of measured DNL is in the range of a few hundredths of LSB. Theoretical considerations were verified by experiments.

Acknowledgements

This work has been supported by the Grant Agency of the Slovak Republic VEGA grant. No. 1/2180/05.

References

[1] Kuyel, T.: "Linearity Testing Issues of Analog to Digital Converters". *IEEE International Test Conf.,* pp. 747-756, 1999.

[2] European project DYNAD.: "*Methods and Draft Standards for the Dynamic Characterization and Testing of Analog-to-Digital Converters"*, published on web at: htpp://www.fe.up.pt/~hsm/dynad

[3] IEEE Std. 1057-1994. "*IEEE Standard for digitizing waveform recorders"*. The institute of electrical and electronics engineers, Inc. New York, USA, 1994, p.80.

[4] Kollár, M.: "A New Approach in Testing Analog-to-digital Converters". Informacije MIDEM - Journal of Microelectronics Electronics Components and Materials, Vol.34. No.4, pp. 135-140, 2004.

[5] Michaeli, L.: Modeling of Analog-to-Digital Interfaces. Mercury-Smékal Press, Košice, p.160, 2001, (In Slovak).

[6] Aumala, O., Holub, J.: „Practical aspects of dithered quantizers". Proc. Intl. On-line Workshop on Dithering in Measurement, Prague, pp. 11-18, 1998.