Analysis and Application of Modified Sub-Optimal Algorithms to ICADC Design

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Abstract **–** The approach presented in the paper shows possibility of increasing performance of cyclic analog digital converters (CADC) [1]. In the paper, the intelligent version of CADC (ICADC) is considered. The main particularities is ICADC computes the binary codes of input signal samples using the model based on the adaptive algorithms developed in [2-5]. In the paper there are presented the results of real design and analysis of the laboratory prototype of sub-optimal ICADC.

I. Introduction

Each microsystem (measurement, control, audio, video and others) require the fast, high-resolution, low energy and cheap ADC. These criterions are the best satisfied by CADC [1]. In the paper intelligent CADC (ICADC) are discussed. Their specific feature is computing the codes of input samples using the long word arithmetic and application for the conversion of the optimal adaptive signal processing algorithms. This permits to remove typical for CADC limitations on the possible values of the the gain coefficients in amplifiers in their analogue part and to make them greater that results in improvement of resolution and speed of conversion [2-7]. The removal of this limitations allows to optimize the wotk of ICADC and improve the their performance taking into account possible overloading of the converter.

In the paper, there is analysed the performance of the laboratory prototype of ICADC in comparison with the results of similar experiments with its simulation model. The second task considered in the paper is the analysis of ICADC with modified sub-optimal conversion algorithm on ICADC performance, and demonstration of its improving influence of on ICADC performance. There are compared the results of simulations carried out for sub-optimal ICADC and its modified version. The results confirm a possibility to improve the performance at the initial cycles of conversion and methods of its achievement.

II. Sub-optimal conversion algorithm

The hardware prototype of ICADC was designed and realized according to the schema presented in Fig.1 on the basis of general relationships obtained in analytical stage of researches (see also [2-7]). The main recursion determining the work of ICADC digital part has the form:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k \tag{1}$$

where $\hat{V}_k$ are the current codes (digital estimates) of the input sample and

$$\tilde{y}_k = C_k e_k + \xi_k \tag{2}$$

are the observations at the analog part output (ADC_{in}). Values

$$e_k = V^{(m)} - \hat{V}_{k-1} + \nu_k \tag{3}$$

are the residuals at the amplifier (A) input. Value $V^{(m)}$ describes the m-th sample at the sample and hold unit (S&H) output (index $m=1,2,\dots,M$ represents a current number of the converted sample, further omitted). Index k is the current number of the conversion cycle ($k=1\dots n$), and ξ_k is the quantization noise at ADC_{in} output, see Fig.1. The analog gain coefficients C_k and the gains L_k in recursion (1) are set, at each cycle of conversion , according to the formula :

$$C_k = \frac{D}{\alpha\sqrt{\sigma_v^2 + P_{k-1}}} \;\; ; \;\; L_k = \frac{C_k P_k}{\sigma_\xi^2 + C_k^2 \sigma_v^2} \tag{4}$$

where $P_k = E[(V - \hat{V}_k)^2]$ presents the mean square error (MSE) of estimate at *k*-th cycle of conversion ($k = 1,...,n$) and is given by formula:

$$P_k = P_{k-1}\left\{1 + \frac{C_k^2 P_{k-1}}{\sigma_\xi^2 + C_k^2 \sigma_v^2}\right\}^{-1} \tag{5}$$

Initial conditions for recursions (1),(5) are: $\hat{V}_0 = V_0$ (mean value of converted signal); $P_0 = \sigma_0^2$ (variance of converted signal). Parameter D determines the saturation level (input range [- D , D]) of the internal ADC_{in}. Value σ_v^2 describes the power of the analog internal noise. Value σ_ξ^2 describes the power of the noise determined by quantization and evaluated by known formula: $\sigma_\xi^2 = \Delta^2/12 = D^2 2^{-2N_{ADC}}/3$, where N_{ADC} is the internal ADC_{in} resolution.

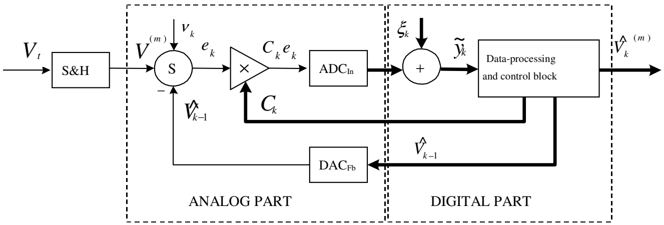

Fig.1. General structure of ICADC.

Parameter α is a saturation factor and determines a probability of ICADC saturation given by formula:

$$\Pr\{| y_k - \hat{V}_{k-1} | > D / C_k \mid \tilde{y}_1^{k-1}\} < \mu \tag{6}$$

Parameter α in (6) satisfies the equation: $\Phi(\alpha) = (1-\mu)/2$, where $\Phi(\alpha)$ is Gaussian error function. If, for each $k = 1,...,n$, the gains C_k and L_k are switched according to (4), resolution N_k of ICADC increases with maximal rate. Relationships (1)-(5) determine the structure and parameters of sub-optimal algorithm of conversion, which enables close to optimal estimates computing and adaptive adjusting the analogue part.

III. Implementation

The prototype of ICADC converter consists of the analog part which is responsible for sampling, adding and amplifying of input signal and the digital part which adjusts analog part and calculates current estimate. The one input sample $V^{(m)}$ performs during *n=7* internal conversion cycles.

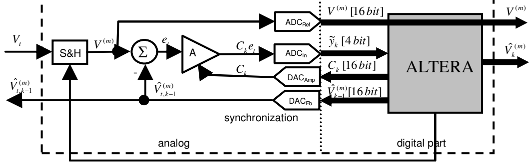

Fig.2. Structure of the laboratory ICADC

In each cycle of conversion of one input signal sample held on S&H output the following sequences of operations perform according to formula (1):

i) Calculating of current estimation error e_k in analog adder block A as a sum of currently converted sample $V^{(m)}$ routed from S&H output and its current estimate $\hat{V}_k^{(m)}$ with opposite sign calculated in previous cycle according to formula (3). For the first cycle of each converted sample $V^{(m)}$ the value of estimate $\hat{V}_0^{(m)} = 0$.

ii) Amplifying of the current estimation error e_k (calculated in sequence i) and present on analog adder block output) by the Voltage Control Amplifier A, with the coefficient gain set by the microcontroler ALTERA conformable to formula (4).

iii) Conversion of amplified estimation error $C_k e_k$ (taken form amplifier A output, performed in sequence ii)) by internal fast, 4-bits converter ADC_{in} with the conversion range $\pm D$.

iiii) Calculating the new more accurate estimate. The digital observation $\tilde{y}_k = C_k e_k + \xi_k$ (from internal converter ADC_{in} output) is transmitted to the microcontroler based on ALTERA and then according to formula (1) new estimate $\hat{V}_k^{(m)}$ is calculated. This estimate, with opposite sign, is routed via 16-bits converter DAC_{Fb} with the conversion range $\pm D^{DAC}$ to the analog adder block input. The new gain C_{k+1} for Voltage Control Amplifier is set simultaneously. After that next conversion cycle starts with sequence i). The coefficients C_k and L_k are written into the ALTERA program table. They are calculated once for an experiment, according to the formula (4) under condition of determined measured signal statistical parameters, and then sent to ALTERA.

The main difference between ICADC and CADC is using long-word arithmetic instead of combination of few-bits partial calculations [4,5,6]. For that reason the C_k coefficients (see formula (4)) don't have to be a power of two. Removal of this limitation allows to optimal selection of the analog coefficients and improve the ICADC performance. In order to realize a such construction (ICADC) using of PLD devices was needed.

IV. Analysis of the prototype functioning

The prototype performance was analysed using specially developed laboratory stand. As a basic characteristic of quality, empirical effective number of bits (ENOB) [3-7] was used computed as follows:

$$\hat{N}_k = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{\hat{P}_k}\right);\ \hat{P}_k = \frac{1}{M}\sum_{m=1}^{M}\left[\ V^{(m)} - \hat{V}_k^{(m)}\right]^2;\ (k = 1,...,n); \tag{7}$$

Typical runs of trajectories ENOB N_k as the function of the cycles number is shown in a Fig.3. Continuous line corresponds to trajectories obtained in the experiment with the laboratory prototype and dashed line - for the computer simulations. Real and simulations experiments are carried out for the same input signals and parameters of elements and algorithms. As an input signal was used a full-scale sin wave with the frequency $f_0 = 200Hz$. The resolution of ADC_{int} was $N_{ADC} = 4$ bit, and DAC_{fb} - $N_{DAC} = 16$ bit. Power of internal analog noise $\sigma_v^2 = 10^{-5}$ Wt was evaluated experimentally and used for calculation of the coefficients C_k and L_k. The samples $V_k^{(m)}$ of the input signal converted by the laboratory prototype of ICADC were routed from the S&H output, through 16-bits ADC, to the computer. Their digital codes were used as the reference signal for the computing the ENOB both of real converter and in its model used simulations to ensure identical conditions of experiment.

Main task solved in experiments was comparison of performance of the laboratory ICADC prototype and its simulation model. Trajectories of ENOB obtained in real experiments and in simulations are almost identical (see Fig.3). The second task was the analysis of changes of ENOB for different values of saturation factor α. As it was described in Sect. II, parameter α defines the probability of ICADC overloading. For less α, the speed of conversion is higher but the probability of overloading grows.

It is worth to notice that in ICADC prototype the implementation of different α parameter values does not need the hardware construction change. The only needed think was reprogramming ALTERA with other set of the coefficients C_k and L_k calculated using variable values of parameter α. It means, this construction allows, in a vary simple and cheap way, to form ICADC performance characteristics for the different experiment (or measurement) conditions.

a) $\alpha = 5$ b) $\alpha = 4$ c) $\alpha = 3$

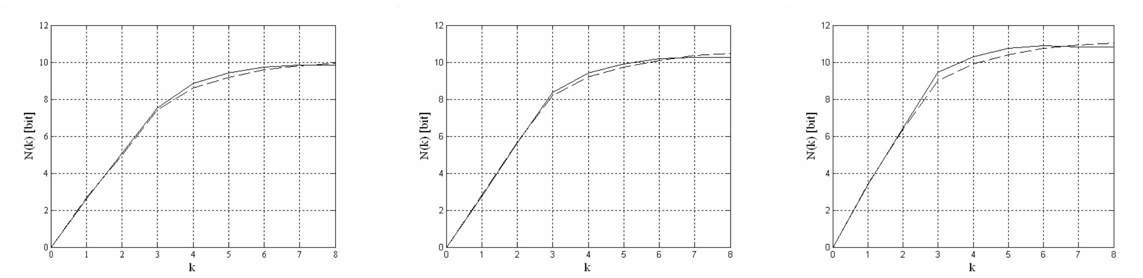

Fig.3. The trajectory of ENOB dependence on the number of cycles for different values of α parameter. (results of laboratory experiments are presented by continuous line, computer simulation dashed lines).

The approach presented in works [1-7] employs general model which has many possibilities of applications in sensors, measurement systems and others. Algorithms (1-6) are optimal for presumption of the linear processing characteristic with saturation level (e.g. $N_{ADC} \to \infty$) and Gaussian distribution of the compensation error e_k (Fig.4a). In this case the optimal coefficient gain C_k for each cycle of conversion is given by formula (4) (taking into account formula (6)). In practice it means the analog compensation error e_k is observed in a range $[-\alpha \cdot \sigma_{e_k}, \alpha \cdot \sigma_{e_k}]$, where $\sigma_{e_k} = \sqrt{P_k + \sigma_v^2}$ is a standard deviation of the compensation error e_k.

a) b)

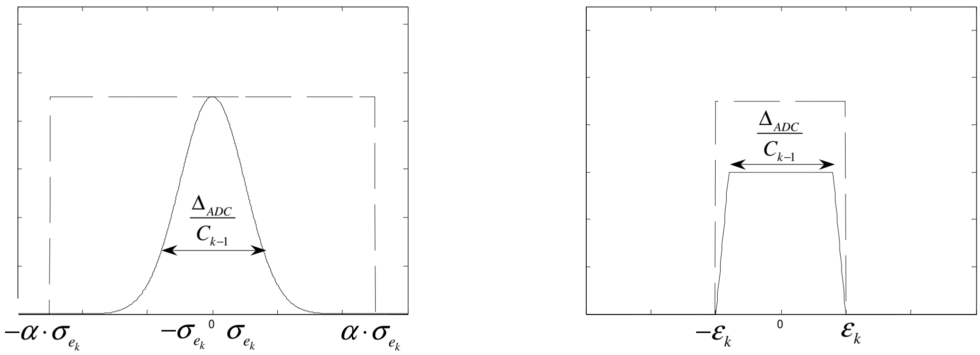

Fig.4. Distribution of compensation error e_k (continuous line) and the observation window of analog part (dashed line): a) for optimal ICADC, b) for sub-optimal ICADC (for number of cycles k>1).

Below, there are considered the effects appearing under the assumption of limited boundaries of ADC_{in} quantisation error $-\Delta_{ADC}/2 \le \xi \le \Delta_{ADC}/2$, where Δ_{ADC} is a quant of ADC_{in}. Simplifying the formula (4) $L_k = 1/C_k$ and substituting (4),(3),(2) into (1) one can obtain following expression for optimal estimates:

$$\hat{V}_k = \left[C_k \left(V^{(m)} - \hat{V}_{k-1} + v_k \right) + \xi_k \right] \cdot \frac{1}{C_k} + \hat{V}_{k-1} + \varsigma_k \qquad (8)$$

where: C_k is the gain coefficient of amplifier (A) at k-th cycle of conversion; $V^{(m)}$ is the m-th input signal sample on S&H output and $\hat{V}_k$ is the estimate of current input sample at k-th cycle of conversion. Variable v_k describes the analog noise at k-th cycle of conversion, ξ_k is the quantization noise at k-th cycle of conversion, ς_k is the numerical processing error. Similar transformation of residual signal (3) gives the expression:

$$e_k = -\left(v_{k-1} + \frac{\xi_{k-1}}{C_{k-1}} + \varsigma_{k-1} \right) + v_k = v_k - v_{k-1} - \frac{\xi_{k-1}}{C_{k-1}} - \varsigma_{k-1} \quad (9)$$

Using well-known assumption [9], we assume further that quantisaion noise of ADCin ξ_k and feedback DAC ς_k are distributed uniformly in corresponding quantization intervals $[-\Delta_{ADC}/2 \cdot C_{k-1},\ \Delta_{ADC}/2 \cdot C_{k-1}]$ and $\left[-\Delta_{DAC}/2, \Delta_{DAC}/2\right]$ (Δ_{ADC} -quant of ADCin , Δ_{DAC} -quant of DAC). Then, probability of ICAD saturation given by formula (6) takes the form:

$$\Pr\left\{\left|e_k\right| > \Delta_{ADC}/2 \cdot C_{k-1} + \Delta_{DAC}/2 + \sqrt{2} \cdot \alpha \cdot \sigma_v \right\} < \mu \quad (10)$$

The probability of ICADC saturation could be interpreted as a field under the probability density function of the residual signal beyond the observation window which is determined by formula (6). The observation window could be interpreted as the interval, where each value of the input signal may appear with the probability not less than 1- μ . Fig. 4a shows the relation between the distribution of residual signal (continuous line) and observation window (dash line) in the conditions considered in derivation of algorithm (1-5) (linear in observation range model (1) and Gaussian signal and noise ξ_k and v_k [10]). Observation window which corresponds to the ICADC can be determined from formula (10). Fig.4b presents similar to Fig. 4a relation between the distribution of residual signal values and observation window which refers to formula (10) where $\varepsilon_k = \Delta_{ADC}/2 \cdot C_{k-1} + \sqrt{2} \cdot \alpha \cdot \sigma_v + \Delta_{DAC}/2$. This distribution is computed as a result of a convolution of distributions of the noises v_k , ξ_k , ς_k . Formula (10) permits to obtain following equation for the gain coefficient C_k . ($k = 2,3,..$):

$$C_k = \frac{D}{\dfrac{\Delta_{ADC}}{2 \cdot C_{k-1}} + \sqrt{2} \cdot \alpha \cdot \sigma_v + \dfrac{\Delta_{DAC}}{2}} \quad (11)$$

The gain coefficient C_1 for the first cycle of each conversion is given by formula (4).

Fig.5 presents the trajectory of ENOB N_k dependence on the number of cycles for different values of α parameter obtained in computer simulations. Each if Fig.5.a-c present two plots corresponding the ENOB of ICADC working on the basis of origin sub-optimal algorithms (continuous lines) and its modified version (dashed line). As an input signal, samples $V^{(m)}$, ($m = 1,...,512$) of Gaussian random signal were used (with zero mean and variance $P_0 = 0.25$). Other parameters had the values: $N_{ADC} = 4$, $N_{DAC} = 16$, $\sigma_v^2 = 10^{-10}$. Value of the noise power σ_v^2 is taken smaller than in first series of experiments in order to show more clearly the effects which appear in modified ICADC. According to Fig. 5, ENOB of ICADC with modified version of sub-optimal algorithm (dashed line) is greater then ENOB of origin ICADC (continuous line). The obtained results show a possibility to improve significantly the resolution ICADC if the modified algorithm of conversion is used. This effect is due to the change of the compensation error e_k distribution (see Fig.4). This modification permits to increase the gain coefficient C_k (*k=2..N*) according to formula (11). Because the α parameter, in the modified ICADC model, concerns the noise v_k only (see formula (11)), the α parameter has a transient influence on the ENOB N_k trajectory during the first few cycles. The α parameter in the ICADC model based on the sub-optimal algorithm (1)-(6) concerns all of the compensation error e_k (see formula (4)) therefore it has a significant influence on the speed of ICADC conversion.

The increment of ENOB N_k of conventional CADC [1] in each cycle is not greater then $\Delta N \le N_{ADC_{in}} - 1$, where $\Delta N = \Delta N_k = N_k - N_{k-1}$. Then the ENOB N_k is given by formula $N_k \le k \cdot \Delta N$. The CADC with the internal ADC converter $N_{ADC_{in}} = 4$ obtains after *k=4* cycles the ENOB $N_4 \le 12$ bits. The construction of ICADC specially while introducing the long arithmetic word permits to set up the gain C_k and L_k coefficients to the optimal value (not only power of two as in a CDAC converters). This is the direct reason of the increment of ENOB N_k of ICADC in each cycle could be described by formula $N_{ADC_{in}} - 1 < \Delta N < N_{ADC_{in}}$. On the Fig.5. ENOB N_k of the modified version of ICADC (dashed line) after *k=4* cycles reaches $N_4 = 14$.

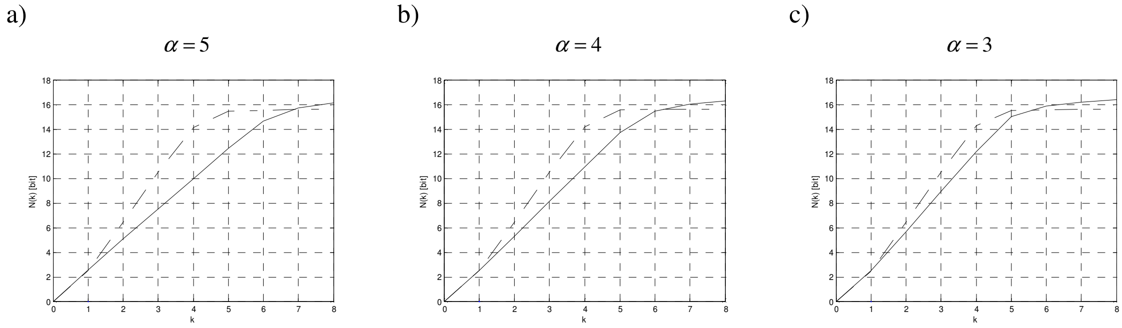

Fig. 5. The trajectories of ENOB depending on the number of cycles under different values of saturation factor α obtained in computer simulations (continuous lines correspond to the plots obtained for ICADC with sub-optimal algorithms [3-7], dashed lines – for its modified version.

V. Conclusions

Adapting into the sub-optimal algorithm (1)-(6) the ICADC processing model gives a possibility to increase the C_k coefficient and to improve the ICADC performance without overloading. The results show a possibility to improve the performance at the initial cycles of conversion and methods of its achievement. The results will be used for improvement of the conventional ICADC performance.
Presented approach gives a possibility to determine easily the parameters of the analog and digital parts of ICADC with additionally improved conversion. This permits to design the “flexible” reprogrammable converters with possibility to reset the parameters, depending on applications. Obtained empirical results are close to theoretically expected. General questions of modified sub-optimal algorithms implementation were discussed. The results of the work can be utilized in further development and design of the advanced pre-industrial prototypes of ICADC.

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