Aperture Jitter and Timing Skew Analyses in ADC Structure

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Abstract- Time interleaved ADCs are generally very sensitive to any sampling time errors. In order to study its influence in term of performance decreasing, there is introduced an ADC jitter model developed in Simulink. Simulation results of this model correspond with the formulas described in literature[1] and [2]. Timing skew errors of the time interleaved structure are discussed and compared to those of a single ADC.

I. INTRODUCTION

As the demand of high accuracy sampling of input frequencies continues to increase, the ADC aperture uncertainty (jitter) is becoming the limiting factor of the achievable SNR of the whole signal acquisition chain. The clock jitter affects the signal accuracy only during the conversion process of analog to digital and digital to analog converters.
ADC clock jitter can cause a degraded performance (noise and distortion) with even small amount of jitter. Improper routing can induce noise to the clock line as a result of coupling from the analog signal chain. The clock jitter can be also the result of a poor clock source, layout or grounding.
In this paper, we will introduce the ADC model developed using Simulink toolbox of Matlab software. In this part we will mention different ADC errors. The timing error will be described in detail in the next part. We will show the model of aperture jitter, the influence of the jitter on ADC dynamic parameters and our model will be validated by simulations as well. The last part deals with timing skew error in the time interleaved ADC. Here, we will depict the differences between clock timing error in a single and a dual interleaved ADC structure.

II. ADC MODEL

Figure 1 represents a simplified ADC model considering only the basic imperfections of the analog-to-digital converter which are placed just after the input sine wave (linearity, gain and offset errors) and the clock signal(jitter and timing skew errors).

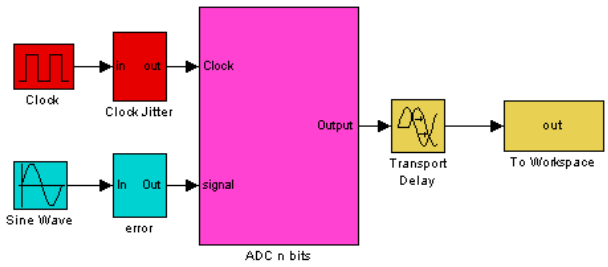

Figure 1. The ADC model

Now let us introduce the description of ADC, Error and Clock jitter blocks as follows:
The **ADC block** represents an ideal ADC with the sample and hold, quantizer and saturation block. All of these blocks are provided by Simulink library.

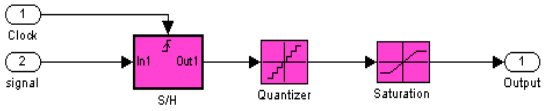

Figure 2. The ideal ADC

As shown in figure 3, the **Error block** represents all kinds of errors which can modify the input sine wave parameters before the conversion process. These errors are the result of imperfection of the manufacturing process. The offset error is usually a constant near zero. The gain one is a multiplicative error which is commonly a constant assumed to be near one. The non-linearity block is modeled by a polynomial function. The last modeled error is the thermal noise given by: $noise_{thermal}(t) = \sqrt{k * T} * n(t)$, where k is Boltzman constant, T is temperature in Kelvin and $n(t)$ is a random Gaussian noise.

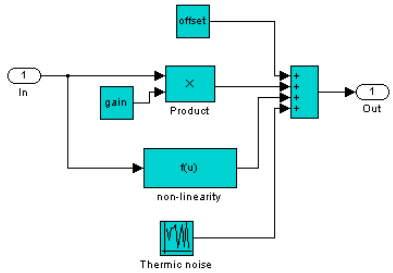

Figure 3. The error block

The last block of the ADC model shown in Figure 1 is the **Jitter error**. This error, which is the main work presented in this paper, will be described in the next section.

III. THE JITTER

A. The principle

As shown in Figure 4, the aperture jitter is an imperfection in the sampling instant, which gives an output with the worst spectral parameter.

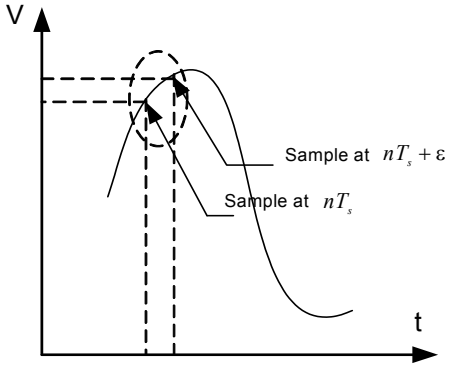

Fig.4. The jitter principle

Consider a sinusoidal input signal $V_{in}(t) = A\cos(2\pi f_{in} t)$. This sine wave is sampled at a time $t = nT_s + \varepsilon$ where T_s is the sampling clock periode and ε is the jitter noise with a Gaussian distribution of $N(0, \sigma_j^2)$ [1]. So, when neglecting the quantization, the ADC output reach the values $V_{out}(nT_s) = V_{in}(nT_s + \varepsilon)$. The difference between the ADC output and input is the jitter error which can be expressed as:

$$V_{out}(nT_s) - V_{in}(nT_s) \approx \varepsilon \left(\frac{dV_{in}(t)}{dt} \right)_{t=nT_S} \qquad (1)$$

with the assumption that

$$2\pi f_{in} \sigma_j << 1 \qquad (2)$$

The error is proportional to the slew rate $\frac{dV_{in}(t)}{dt}$ as well as the jitter ε. Hario Kobayashi showed in [1] and [2] that with the assumption of (2) the noise power due to the jitter is given by

$$P_j = 2\pi^2 f_{in}^2 A^2 \sigma_j^2 \qquad (3)$$

So, the SNR due to the aperture jitter is given by

$$SNR = 10\log\frac{A^2/2}{2\Pi^2 f_{in}^2 A^2 \sigma_j^2} = -20\log(2\Pi f_{in}\sigma_j) \quad [dB] \qquad (4)$$

Without the assumption of (2), S. S. Awad has demonstrated in [4] that the SNR can be expressed by

$$SNR = -10\log\left[2\left(1-\exp\left(-2\pi^2 f_{in}^2 \sigma_j^2\right)\right)\right] \qquad (5)$$

B. The model

The jitter block is modeled in detail in Figure 5. Note, this model consist only of digital Simulink blocks.

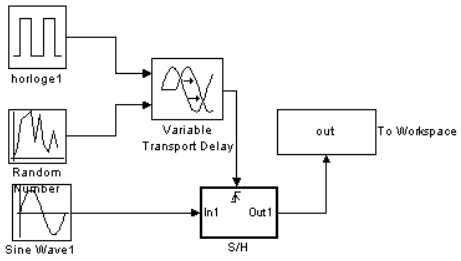

Figure 5. Jitter model Figure

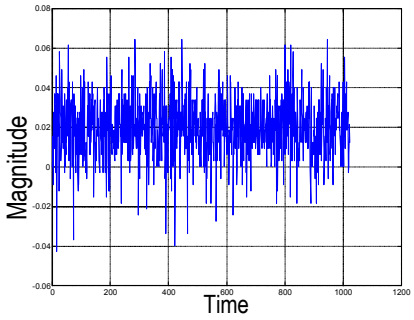

Figure 6. Sampling system response in time domain

The Random Number block generates normally distributed random numbers. Contrary to the theory, this Gaussian noise is used with nonzero mean to be coherent with the delay transport bloc. These sequences of random number are considered as a time delay in the variable transport delay. To emphasize the jitter effects, we will sample the input signal at the clock frequency. This means that, if the clock is without jitter, we take always the same sample. If a jitter is added as a delay to the clock by the random Gaussian number, the sampling system output is presented by noise proportional to the value of jitter and to the variation of the input signal.

Using a finite sampled input signal the number of states in the sinusoidal input is also finite. That's why there are a difference between the histogram of input noise and output sampling system. Figures 7 and 8 show respectively the two histograms of input jitter error and the sampling system output.

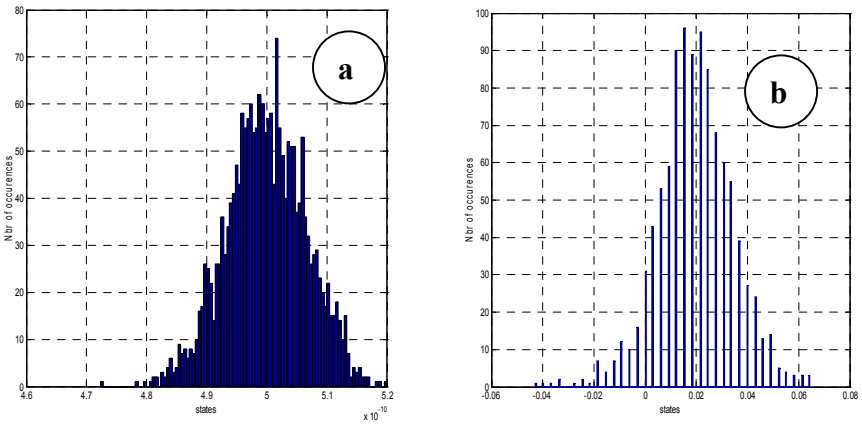

Figure 7. Histogram: (a) input jitter, (b) sampling system output.

The maximum of jitter inserted in ADC is given by this equation :

$$Maxjitter = 1/2^{(resolution+1)} * \pi * F_{in} \qquad (6)$$

We simulate the jitter model with the same input frequency and sampling clock frequency equal to 500MHz. The jitter inserted in the model is of 40ps. The value of jitter of the this system is about 46.7ps.

C. Model validation

This section is dedicated to the validation of our model using the whole ADC model shown in figure 1. During this simulation we consider that gain, offset and nonlinearity errors do not exist and only the jitter error is changed. Figure 8 shown the ADC simulation results with two different jitter: the first at 20ps , the second at 40ps. As it was expected, the noise level increase with the jitter value.

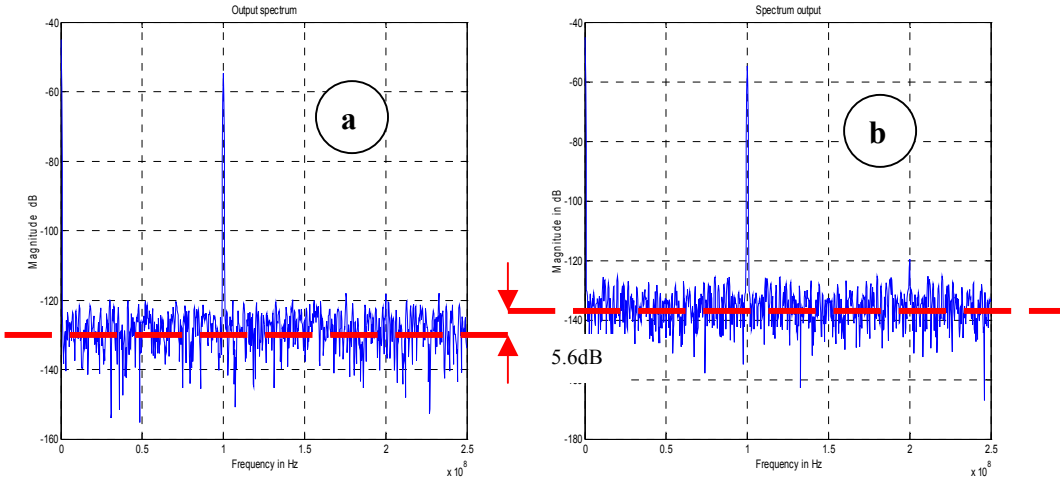

Figure 8. ADC response: (a) 40ps of jitter, (b) 20ps of jitter.

The first approach is based on a qualitative validation, now we propose a quantitative validation of the jitter model is based in spectral parameters evaluation with a fixed jitter. We make the magnitude input signal changed until the full scale. The input signal frequency is near to the half of sampling frequency. We work at coherent input frequency. Figure 9 show that SNR increases differently according to the presence of the jitter. With 10ps of jitter and beyond fifth of the full scale, the SNR is stabilized. In the simulation conditions, the theoretical SNR detailed by the equation (4) is of 39.6dB and we simulate an SNR of 42dB. The model works well.

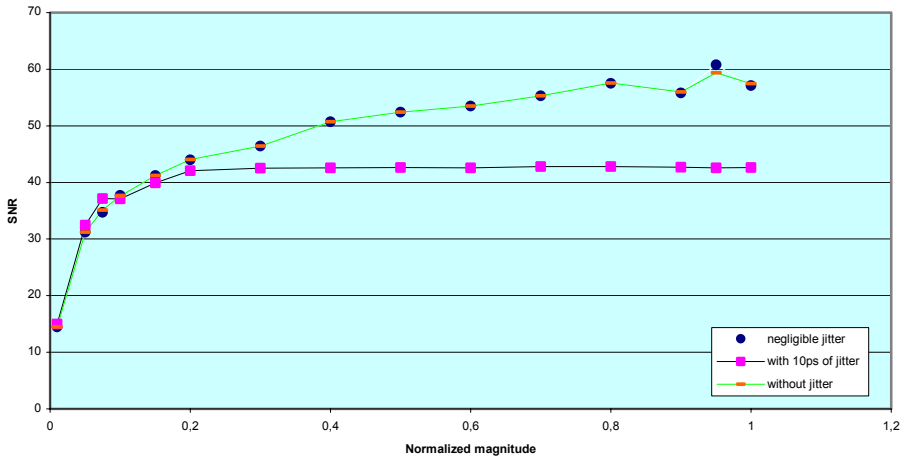

Figure 9. SNR variation vs. jitter.

III. THE TIMING SKEW

The timing skew is the error of timing in time interleaved ADC. In this part we will show the difference in timing error in a single and a dual ADC structure. In fact, if we interleave two ADCs with two different timing error, the output timing error is higher than the sum of two error.

A. Time interleaved ADC structure

The technique of time-interleaving ADCs [3] consists in placing M ADCs with duty cycle interleaved between them. The ADCs are mounted to convert the same signal. After the conversion, all the outputs signals are multiplexed. This architecture presents a fast conversion flux, having the conversion rate determined by the number of parallel ADCs in the circuit.

At high conversion rate applications, such as satellite receiver and dual channel digital oscilloscope applications, time-interleaving ADCs technique is an attractive choice. This technique is used in two situations: when an application requires a high conversion rate, not achieved by a single ADC; or when the manufacturing cost is reduced using lower cost parallel ADCs than one single high conversion ADC.

The time interleaved ADC model developed in Simulink is shown in next figure. The ADC n bit, errors and clock jitter subsystems are identical to those which were quoted in the first part.

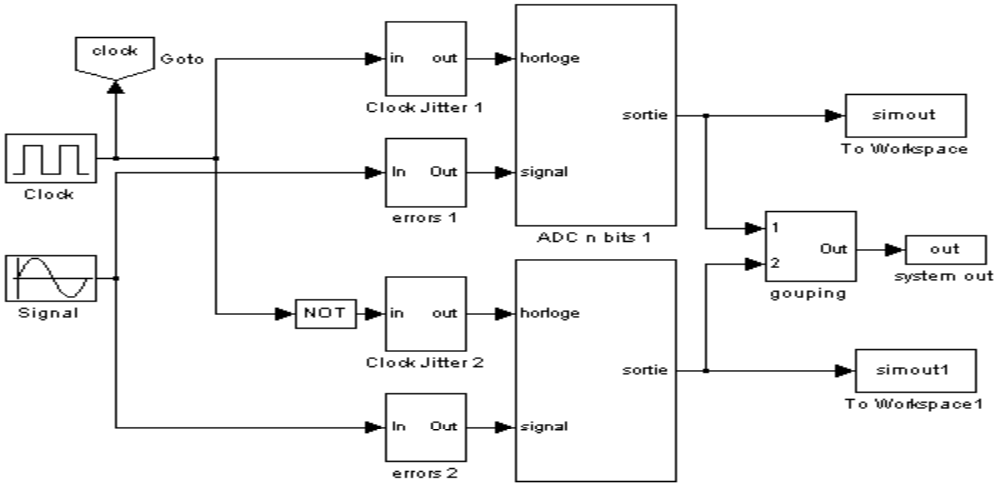

Figure 10. Time interleave ADC model

Offset and gain error are largely quoted in literature, so in this paper we focuses on the timing skew and compare the influence of timing errors for the single and the dual ADC.

B. Timing skew effects vs. aperture jitter

According to [1], and for a sinusoidal input, the noise power Ps due to the timing skews is equivalent to this given in (3) where $\sigma_j^2 = \frac{1}{M}\sum_{p=1}^{M}\left(dt_p\right)^2$, dt_p is aperture jitter for every ADC. However, in frequency domain, there are a big difference : the basic error occurs with a period of M / fs and the magnitude of the error is modulated by the input frequency f_{in} . The noise spectrum peaks are at

$$f(noise) = \pm f_0 + k * f_s / 2\,,\ k = 1,2,3... \qquad (7)$$

Note, that *SNR* degrades as f_{in} increases what is also different compared to the jitter.

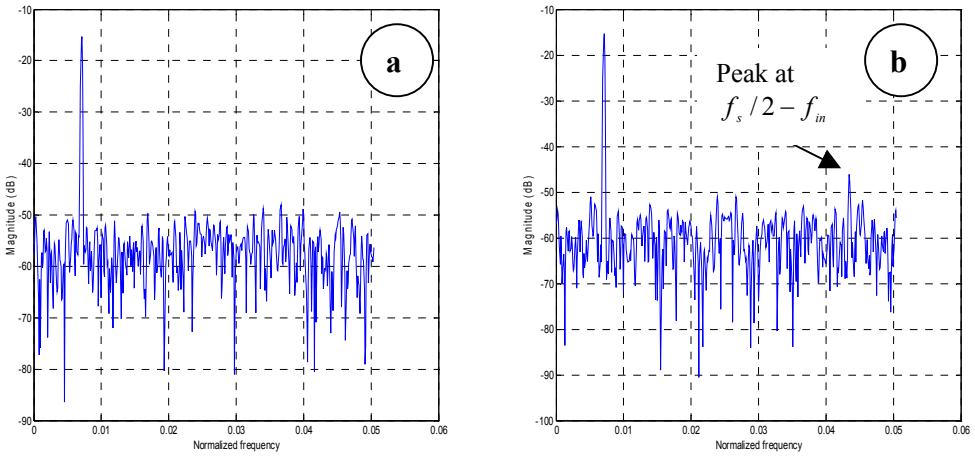

Figure 11**.** Simulation result of a two-channel time-interleaved ADC system with timing error channel. 1024-point FFT was performed with f_s = 2*500e06Hz, f_0 = 70e06Hz.(a) : jitter1 = 20ps, jitter2 = 20ps; (b):jitter1 = 20ps, jitter2 = 40ps.

II. Conclusion

Many are those which treated the ADC modeling such as in [5] and [6]. Contrary to what was made we showed in this paper a complete model of analog to digital converter and we have oriented our study on the jitter model. Digital simulations made on Matlab validated the mathematics formulas already quoted in literature. The same model was injected around a time interleaved ADC structure. A comparison was made between the jitter and the timing skew. This has showed differences in the indices of peaks in the output spectrum but it also showed similitude in the value of jitter and timing skew. This is true only under some initialization conditions.

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