Continuous-Time Delta-Sigma Modulator Model for A/D Conversion

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***Abstract*-**In this paper we present a study of a Continuous-Time Delta-Sigma Modulator (CT ΔΣM) to be applied in radio communication systems, including a high-level modelization for simulation purposes. The conventional sample-and-hold and comparator blocks, very popular in CT ΔΣM models, are replaced by an analog-to-digital converter (ADC), in order to allow the ADC modelization. In this way, we propose a model able to improve the performances of ADCs. This model is a useful tool to characterize data conversion systems.

I. Introduction

The rapid development of radio communications systems has led to a great effort to design high resolution and high-speed analog-to-digital (A/D) converters. Delta-Sigma (ΔΣ) modulators are popular nowadays for A/D conversion applications. A ΔΣ Modulator can be implemented by designing the loop integrator / resonator either in the discrete-time (DT) domain such as switched-capacitor filters or in the continuous-time (CT) such as with RC, transconductors-C and LC filters [1]. There is an increasing interest in designing ΔΣ modulators using continuous-time circuitry for the loop filter, because it is generally possible to clock CT ΔΣ modulators at much high frequency than DT ΔΣ modulators. Consequently, for a given oversampling ratio (OSR), the conversion bandwidth is greatly increased. It is known, however, that the continuous-time ΔΣ modulators suffer from performance degradation due to nonidealities such as excess loop delay and clock jitter in the ΔΣ modulator loop [2]. The aim of this paper is to model a ΔΣ modulator for conversion of wider bandwidths, in order to meet the high dynamic range (DR) requirements of radio applications. Architecture was developed in order to allow the insertion of an ADC inside the ΔΣ conversion chain. In this way, from a known ADC, it is possible to make its modelization and improve its performances.

II. Radio Receiver Application for ΔΣ ADC

There are two types of ΔΣ modulators: the low-pass (LP) converters and the band-pass (BP) converters. ΔΣ Modulators where the quantization noise has high pass shape are built with low pass loop filters and hence are denoted LP converters. If we were to build a transfer function out of resonators, the noise would tend to be shaped away from the resonance frequency. The quantization noise then has a band stop shape because the loop filter is band pass, and the resulting ΔΣ modulators are called BP converters. A common type of band pass converter is built starting with a low pass transfer function and performing the substitution $z^{-1} \rightarrow -z^{-2}$. This produces a converter with noise shaped away from $f_s/4$ with identical stability properties and performance as the low pass prototype, thought the order is doubled [3].

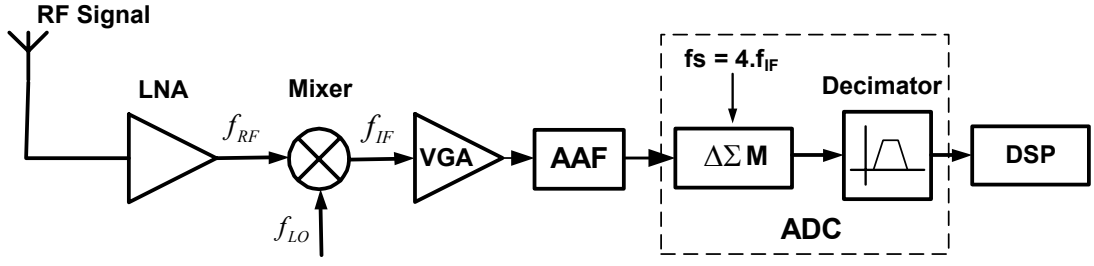

Figure 1. Classic radio receiver application for ΔΣ Modulator

A typical application of such a converter is the conversion of an RF or IF signal to digital for processing and heterodyning in the digital domain. The quantization noise is large everywhere except in a narrow band near the frequency carrier. Mixing to baseband digitally for I and Q channel recovery becomes particularly easy when the sampling frequency is chosen to be four times the input signal frequency ($f_o = f_s/4$). This because sine and cosine are sequences involving only ± 1 and 0, so simple digital logic can replace a complicated multiplier circuit. In general, the ability of a ΔΣ modulator to perform narrowband conversion at a frequency other than dc makes them particularly attractive for radio applications. Furthermore continuous-time ΔΣ modulators can be made fast enough to allow conversion of signals into the hundreds of MHz and beyond [3]. A straightforward implementation of the receiver back end as depicted in Figure 1 is feasible, but suffers from the drawback of requiring several high-dynamic-range (and thus high-power) blocks, namely the variable-gain amplifier (VGA), the mixer, the anti-alias filter (AAF) and the ADC. Since the VGA can be eliminated if the ADC has sufficient dynamic range, and since the AAF can be eliminated if the ADC is of the continuous-time variety, the system can be simplified greatly by using a power-efficient and high-dynamic-range continuous-time ΔΣ ADC. Note in the Figure 1 that after a stage of analogue amplification and mixing, the IF band is digitised and mixed down to baseband. After that the spectrum is filtered and the signal details sorted out using DSP.

III. CT ΔΣ ADC Model

One of the main problems of the ΔΣ modulator is the difficulty to predict the converter resolution by analytical means, thus relying on transient simulations for obtaining its performance. However, the large oversampling ratio used in the modulator and the requested accuracy demands a lot of time with SPICE-like simulators to perform the transient simulation, which makes it unfeasible. This is why the use of high-level description models like MATLAB and SIMULINK is necessary [4]. The Matlab environment is ideal for the behavioural simulation of ΔΣ converters because signals can be treated as vectors (matrices with only one row or column) and the modulator itself can be described simply as a set of difference equations. A few recent papers [5], [6] have investigated the use of CT ΔΣ modulators BP converters for digitisation of an analogue signal at an intermediate frequency (IF) in a radio receiver. These systems are still limited in bandwidth reason why it is not possible nowadays to meet the standards requirements radio applications.

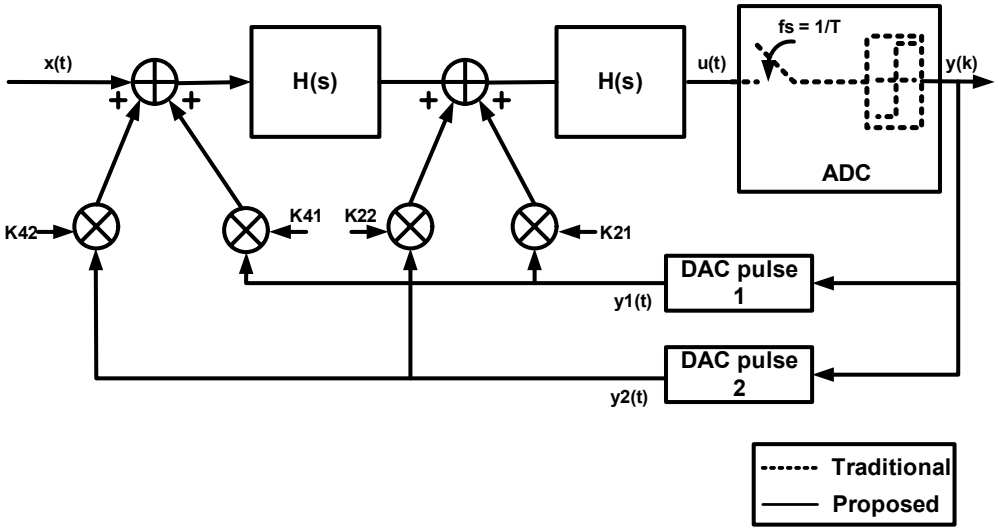

Figure 2. High-level model of a general ΔΣ ADC

In this paper, the authors propose a model using SIMULINK able to characterize the systems conversion and to increase its performances (for example, the conversion bandwidth). The traditional sample-and-hold and comparator circuits, very popular in the CT ΔΣ structures, are replaced by an ADC [7], in order to model and analyse its behaviour. The goal is to use the advantages of CT ΔΣ architecture to improve the performances of the conversion system. The high-level model of a general

ΔΣ ADC is shown in Figure 2. The aim is to find a reasonable tuning of the conversion system before facing the circuit implementation.
The architecture used in this paper is based in an association of resonators ($As/s^2+\omega^2$) with two different types of feedback DAC (Digital-to-Analog Converter), leading to the so-called *multifeedback architecture* in Figure 2. This kind of architecture allows to achieve higher order noise-shaping maintaining the modulator stability. There, the DAC's are return-to-zero (RZ) and half- return-to-zero (HRZ). Both are easy to fabricate in an ECL-style latched comparator by diode-connecting the final differential pair rather than cross-coupling them [6]. We could have used any two of NRZ (non-return-to-zero), RZ, and HRZ, or for that matter any other two different pluses, but these three types are easiest to build in a practical circuit.
The NTF (Noise-Transfer-Function) of this modulator is a band-pass NTF one, with a noise notch at one quarter of the sampling frequency ($f_s/4$). We used the fourth order band-pass function:

$$H(z) = \frac{z^{-2}(2+z^{-2})}{(1+z^{-2})^2} \tag{1}$$

This has its counterpart in continuous-time:

$$H_{BP}(s) = \frac{\left(\frac{\pi}{2}-\frac{1}{4}\right)\frac{s^3}{T}+\left(\frac{3\pi^2}{16}+\frac{\pi}{4}\right)\frac{s^2}{T^2}+\left(\frac{\pi^3}{8}+\frac{\pi^2}{16}\right)\frac{s}{T^3}+\frac{3}{4}\left(\frac{\pi}{2T}\right)^4}{\left(s^2+\left(\frac{\pi}{2}\right)^2\right)^2} \tag{2}$$

The NTF $H_{BP}(s)$ implemented in Figure 2 can be set by altering the K coefficients. We wish to find how to set K's in order to realize the band-pass NTF; this is done by converting $H_{BP}(s)$ to the z-domain for each DAC separately, then linearly combining the results and solving K's.

IV. The ADC Modelled

The ADC used in this model was developed by the Design Team of IXL Laboratory [7], in a BiCMOS 0.25µm SiGe process from STMicroelectronics. It was designed to meet the requirements of radio astronomy applications. The chip integrates an input adapter amplifier, seven comparators (one per comparison level) with associated latches, an encoder matrix and three output buffers. The main features of the ADC are a 3 bits resolution (8 quantization levels), an input bandwidth from 2 to 4 GHz with 4 GHz sample rate. The design architecture of this digitizer is based on a conventional flash analog-to-digital converter structure. The comparator outputs are coded by a FDL encoder with a 3-bits Gray code. The measurement results show that the converter is operational for clock rates up to 5.5 GHz. The overall chip dissipates 1.4 W under 2.5 V and the die area is 9 mm² (Figure 3).
Figure 4 shows outputs for a 4 GHz 0 dBm clock and a 3 GHz 0 dBm sinusoidal input. This result verifies the good functionality of the encoder.

The original chip was designed for radio astronomy applications, where the dynamic tests like SNR and SINAD are not significant, because the input signal is a Gaussian statistics weak noise buried in another noise signal dominated by the front-end system noise. Only a digital auto-correlator system can estimate the conversion efficiency of an input weak noise signal after a long integration. Nevertheless, the model presented in this paper is able to evaluate several ADC's characteristics, including SNR and SINAD. This allows us to model the chip to different applications and requirements.

In order to respect the condition $f_o = f_s/4$, the behavioural model has sampling frequency at 4GHz and input signal at 1GHz.

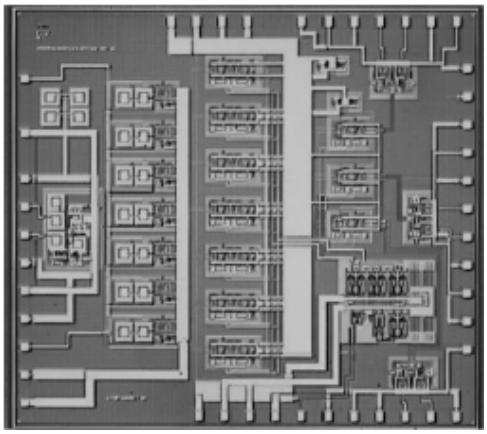

Figure 3. Microphotograph of the chip

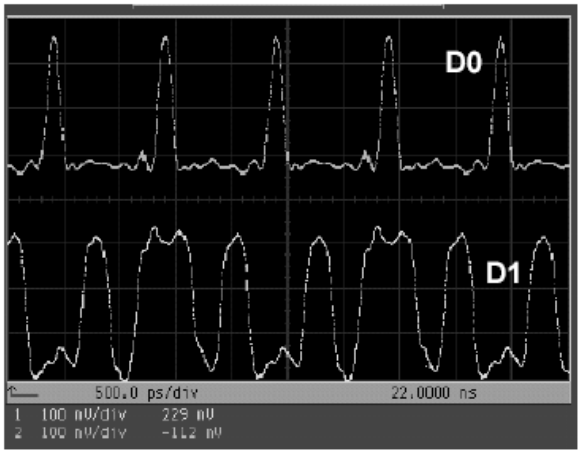

Figure 4. Measured output waveforms (3 GHz input signal and 4 GHz clock)

V. Conclusion

A Continuous-Time Delta-Sigma Modulator Model has been developed using SIMULINK. Architecture based in an association of resonators with two different types of feedback DAC was used in order to achieve higher order noise-shaping maintaining the modulator stability. This model is able to characterize ADCs and improve its performances. The conversion system has been tuned in order to meet the high dynamic range and bandwidth requirements of radio applications. The ADC modelled can be used in a receiver radio, applied in the first intermediate frequency (IF).

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