Direct and Indirect Methods of ENOB Evaluation and Analysis

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Abstract. The paper presents the backgrounds of analytically grounded approach enabling strict theoretic and experimental analysis of the cyclic analogue-to-digital converters (CADC) [1,2] performance. Methods of assessment of the effective number of bits (ENOB [3,4]) and effective resolution (EFR, [5]) of these converters are considered. The analysis is based on results of works [6-8] and develops the direct approach to real ENOB values evaluation proposed in [9]. There is shown the specific for CADC and important for design and applications effect of normalisation of the output quantization noise with the growth of the number of cycles.

I. Introduction

Recently, all the greater attention is paid to development of cyclic and cascade (pipe-line) converters, which is conditioned by their high performance, as well as technical, technological and marketing characteristics [2,10]. Growing requirements to ADC (to their sizes, energy consumption, production cost, speed and accuracy of conversion) impose full utilisation of the resources of analogue and digital elements of converters. In the paper, this and related task of reliable and accurate evaluation of conversion quality are discussed. The analysis is performed for intelligent cyclic A/D converters (IC ADC [6-9]), but the approach can be also applied to analysis and design of other cyclic or cascade ADC.

In [6-9] it is shown that a necessary condition of full utilisation of the resources of CADC is transition to computing the codes of input samples as long binary words of fixed length using sub-optimal conversion algorithm [6-9, 11] (see also Sect 2). Computation can be performed using simple long-word arithmetic unit integrated with CADC's analogue part or directly in the microprocessor, which employs CADC as the analogue input. The term "intelligent" CADC reflects their capability to adaptively restore the model of the input signal and apply it to the analogue part adjusting.

Performance of sub-optimal IC ADC approaches the theoretically achievable boundaries. In order to design and manufacture these converters, adequate and reliable methods of their performance assessment and testing have to be developed. Nowadays, CADC are analysed as "black boxes" using procedures developed for flash, parallel ADC and based on sine-wave testing signal and assumption about uniformity of the distribution of quantization errors. This approach has a number of serious shortcomings. Firstly, it does not permit to analyse the influence of non-ideality of CADC analogue elements (gain errors, offsets, differential and integral non-linearities of internal quantizer, etc.) on the results of measurements. The second drawback is the assumption that quantization errors have uniform distribution, which is not valid for CADC. The latter makes it impossible to accurately evaluate the reference ideal IC ADC ENOB and to assess the actual ENOB values. Furthermore, sine-wave is not an adequate signal for CADC testing as the residual signal at their input is, beginning with the second cycle of conversion, a random process independently of the form and characteristics of the input signal.

In the paper, approach permitting to remove these shortcomings is discussed. Main attention is paid to analysis of conversion errors in IC ADC. Investigation is carried out on the basis of approach [6-8] developed for optimisation and design of cyclic ADC with long-word codes computing. Apart from sub-optimal conversion algorithm, works [6-8] present the relationships for upper boundary of ENOB of sub-optimal IC ADC versus number of cycles and parameters of the input signals, noises, analogue elements and conversion algorithm. In [9], in turn, equivalence of the expressions for ENOB introduced in [6-8] and in Standard [3] is shown (see also Sect. 3). It permits to develop unified mathematically grounded approach to analysis, optimal design and practical realisation of IC ADC and other classes of cyclic and cascade ADCs, as well as to evaluation and measurement of their performance characteristics.

2. Principles of CADC and IC ADC functioning. Conversion errors diminution

General scheme of cyclic ADC is presented in Fig. 1 [1,2]. Input signal V_t is sampled in the sample-and-hold (S&H) block. Each sample $V^{(m)}$ ($m = 1,2...$) is converted in the same way in $n = T / \Delta t_0$ cycles ($T = 1/2F$ is the sampling interval, $\Delta t_0 = 1/F_0$ is duration of a single conversion cycle). During each interval $T = n\Delta t_0$ S&H block keeps the voltage $V_k^{(n)} = V$ constant at the first input of the summer Σ (further, index m in $V_k^{(n)}$ is omitted). At each cycle $k = 1,...,n$, summer Σ forms the residual signal $e_k = V - \hat{V}_{k-1} + \nu_k$ next routed to the input of amplifier A with controlled gain C_k.

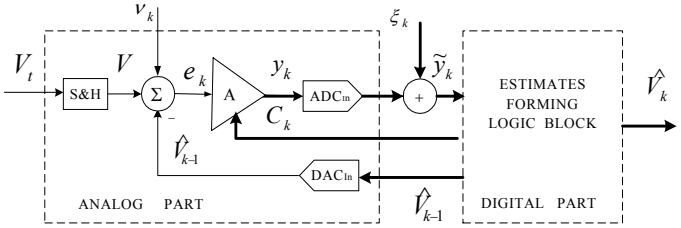

Figure 1. General structure of cyclic CADC

Amplified signal $y_k = C_k e_k$ is routed to the input of internal fast low-bit ($N_{ADC} = 1 \div 8$ bit) A/D converter $\mathrm{ADC_{In}}$. Formed by $\mathrm{ADC_{In}}$, code (observation) $\tilde{y}_k$ is routed to the digital block, which computes new estimate $\hat{V}_k$ according to the recursive equation valid for all classes of CADCs:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k ; \quad (k = 1,...,n) . \tag{1}$$

In each cycle, new estimate $\hat{V}_k$ is written into the storing unit instead of the previous estimate $\hat{V}_{k-1}$. Simultaneously, value $\hat{V}_{k-1}$ is routed to the input of high quality feedback digit-to-analog converter $\mathrm{DAC_{In}}$. The analogue equivalent of digital estimate $\hat{V}_{k-1}$ is routed (with inverted sign) to the second input of the summer Σ, and the new, (k+1)-th cycle of conversion begins. Noise ν_k in Fig. 1 is the summary noise of the feedback chain, S&H block and the summer Σ. Below we assume that ν_k is a white zero-mean gaussian noise with the variance σ_ν^2. Value ξ_k describes the zero-mean $\mathrm{ADC_{In}}$ quantization noise. Variance σ_ξ^2 of quantization noise is evaluated according to the commonly used formula: $\sigma_\xi^2 = \Delta^2/12 = D^2 2^{-2N_{ADC}}/3$, where N_{ADC} is the $\mathrm{ADC_{In}}$ resolution.

Differences between various types of CADC are taken into account in the values of the gains L_k in (1) and parameters of the model of the analogue part. This model should reflect both particularities of the ideal IC ADC work and dependence of observations $(\tilde{y}_1,...,\tilde{y}_n) \equiv \tilde{y}_1^n$ on nonlinearities, parameters setting errors and noises in the analogue part. In [6-8], it was shown that the simplest non-linear model satisfying these requirements and permitting to solve the task of IC ADC optimisation has the form:

$$\tilde{y}_k = \begin{cases} C_k e_k + \xi_k & \text{for } C_k \mid e_k \mid \le D ; \\ D\,sign(e_k) + \xi_k & \text{for } C_k \mid e_k \mid > D , \end{cases} \tag{2}$$

where $e_k = V - \hat{V}_{k-1} + \nu_k$ and $y_k = C_k e_k$ is the signal at the $\mathrm{ADC_{In}}$ input. Parameter D determines the boundaries $[-D, D]$ of the full-scale range (FSR) of $\mathrm{ADC_{In}}$. Particularity of model (2) is that apart of quantization noise, also the always-limited FSR of $\mathrm{ADC_{In}}$ is taken into account, which permits to consider overloading of the converters. The model is "ideal" in sense of [3-5], that is the offsets, gains C_k setting errors, differential and integral non-linearity of actual $\mathrm{ADC_{In}}$, are not (but can be) considered.

To explain the benefits of IC ADC over conventional CADC, let us consider their work in detail. In conventional CADC [1,10], short (N_{ADC}-bit) binary word $L_k \tilde{y}_k$ is, at each cycle of conversion, written into the memory unit where previous estimate $\hat{V}_{k-1}$ is stored. This is realised by shifting and adding the code $\tilde{y}_k$ to less significant bits of the estimate $\hat{V}_{k-1}$ so that m_k most significant bits of the code $\tilde{y}_k$ overlap m_k less significant bits of the code $\hat{V}_{k-1}$ (see Fig. 2). Such overlapping removes possible errors in final codes of estimates $\hat{V}_n$ due to possible errors in LSB of intermediate estimates $\hat{V}_k$.

Shifting observations $\tilde{y}_k$ by an integer number of bits, restricts the set of permissible values of both the digital and analogue gains to the values [8,9]:

$$L_k = C_k^{-1} = L_{k-1} 2^{-(N_{ADC} - m_{k-1})} = L_1 2^{-\Sigma_{i=1}^{k-1}(N_{ADC} - m_i)} ; \quad C_k = C_{k-1} 2^{(N_{ADC} - m_{k-1})} = C_1 2^{\Sigma_{i=1}^{k-1}(N_{ADC} - m_i)} , \tag{3}$$

where initial values C_1 and L_1 are determined by the ratio of input FSR of $\mathrm{ADC_{In}}$ and CADC, and also have the form of integer power of two. Setting the gains to other values will cause errors in the least significant bits of the codes $\hat{V}_k$. Resolution of CADC after n cycles is equal to $N_n = \Sigma_{i=1}^{n}(N_{ADC} - m_i)$.

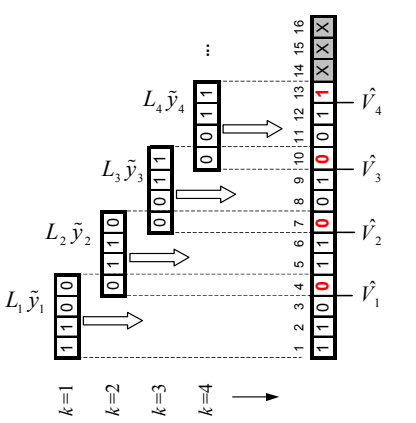

Figure 2. Code forming in conventional CADC.

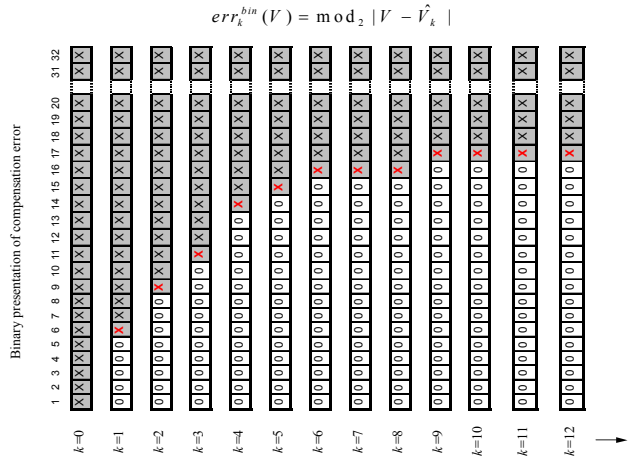

Figure 3. Code forming in IC ADC

In IC ADC, binary logic elements which realise shifting, adding and storing operations are replaced by a long-word computing unit (N_{comp} = 16; 24 or 32 -bit arithmetic depending on required accuracy of conversion). This permits to compute codes of estimates according to recursion (1) in the form of N_{comp} -bit words of the same length at each cycle of conversion instead of forming the estimates $\hat{V}_k$ by sequential "gluing together" N_{ADC} -bit words $L_k\tilde{y}_k$, as in conventional CADC (Fig. 2). Each new estimate $\hat{V}_k$ is the result of adding the N_{comp} -bit code word $L_k\tilde{y}_k$ to the previous N_{comp} -bit estimate $\hat{V}_{k-1}$. This process is illustrated in Fig. 3, where the changes of binary code of estimation error $err_k^{bin}(V) = \mathrm{mod}_2 |V - \hat{V}_k|$ in subsequent cycles $k = 1,...,n$ are shown. Positions of zeros correspond to the bits without errors. The latter one creates the basis for development of direct procedures of ENOB assessment [9] as alternate to indirect ones [3-5],[6-9] based on measurements of the root mean square errors (*rms* in notations used in [3]) of the codes $\hat{V}_k$ (see also Sect. 3).

Transition to long-word estimates computations removes the constraint (3) on the set of permissible gains L_k and C_k. For this reason, gains C_k can be set to values some greater than in conventional CADC. This increases, for each $k = 1,...,n$, the signal to quantization noise ratio SNR_k^{ac} at the internal $\mathrm{ADC_{In}}$ output. The latter diminishes its influence on the quality of estimates $\hat{V}_k$ and increases, at each cycle of conversion, the number of correct bits in these estimates. Enlargement of the gains C_k is limited, however, by the requirement that the probability of overloading P^{sat} be not greater than a given acceptable value μ at each cycle of conversion. One should notice, that for this reason the gains C_k in conventional CADC have the values always smaller than the maximal acceptable ones which practically never belong to the set (3). This, in turn, diminishes CADC resolution in comparison with potentially available. Role of this effect increases for CADC with low-resolution $\mathrm{ADC_{In}}$.

According to the said above, in IC ADC, gains C_k can be set to the optimal values (maximal under given permissible probability of saturation). These values as well as corresponding values L_k can be found using analytical approach described in [11] (see also [6-8]). For each $k = 1,...,n$, minimisation of MSE of estimates $P_k = E[(V - \hat{V}_k)^2]$ over gains C_k, L_k under probability of overloading not greater than μ gives following relationships for the optimal gains values:

$$C_k = \frac{D}{\alpha\sqrt{\sigma_v^2 + P_{k-1}}}, \qquad L_k = \frac{C_k P_k}{\sigma_\xi^2 + C_k^2\sigma_v^2} = C_k^{-1}\left(1 - \frac{P_k}{P_{k-1}}\right), \tag{4}$$

$$P_k = \left(1 + \frac{C_k^2 P_{k-1}}{\sigma_\xi^2 + C_k^2\sigma_v^2}\right)^{-1} P_{k-1} = (1+Q^2)^{-1}\left(1 + \frac{\sigma_v^2 Q^2}{\sigma_v^2 + P_{k-1}}\right)P_{k-1}, \tag{5}$$

$$Q^2 = \frac{C_k^2 E(e_k^2)}{\sigma_\xi^2} = \frac{W_{sign}}{W_{noise}} = \left(\frac{D}{\alpha\sigma_\xi}\right)^2 = \frac{3}{\alpha^2}2^{2N_{ADC}}. \tag{6}$$

Optimal number of cycles of each sample conversion can be found from the equation $P_k = \sigma_v^2$ and has the value:

$$n^* \approx \frac{1}{\log\,(1+Q^2)}\log\left(\frac{\sigma_0^2}{\sigma_v^2}\right). \tag{7}$$

Relationships (1), (2), (4)-(7) determine the structure and parameters of converters whose performance can approach theoretically achievable boundaries (sub-optimal converters). Formulas (5),(7) represent, respectively, the dependence of low boundary of MSE of estimates and optimal number of cycles (time of conversion or frequency band) on parameters of the analogue part, data-processing algorithm, input signals and noises.

Initial values for recursions (1), (5) are determined by the mean value and permissible power of the input signal: $\hat{V}_0 = V_0$, $P_0 = \sigma_0^2$, respectively. Parameter α in (4),(6) is the saturation factor connected with the given value of probability μ of IC ADC overloading [6-9,11] by the relationship: $\Phi(\alpha) = (1-\mu)/2$ where $\Phi(\alpha)$ is gaussian error function. Value Q^2 is the SNR at ADC_{In} output.

In these conditions, input FSR of the converters can be determined as the interval $[-V_0^{\max}, V_0^{\max}]$, which guarantees that each sample V of the input signal falls within it with the probability μ. For gaussian input signals with zero mean value and variance σ_0^2, boundaries of FSR have the values $[-V_0^{\max}, V_0^{\max}] = [-\alpha\sigma_0, \alpha\sigma_0]$. Choice of $\alpha = 3$ refers to the probability of overloading $\mu \sim 10^{-3}$, and corresponding FSR is the "three sigma" range. Nowadays, a more prevalent value of saturation factor $\alpha = 4$ is used that corresponds to $\mu \sim 10^{-5}$. Being the probability of ADC_{In} overloading, value μ determines the probability $\gamma = 1-(1-\mu)^n$ of receiving an erroneous code of the sample. According to [3], p. 4.13, value $\gamma = \mu n$ describes the *word error rate* or the probability of spurious codes appearance.

3. CADC and IC ADC performance analysis

As it was stated above (see also [6-9,11]), beginning with the second cycle of conversion, the residual signals at the CADC input have random values. The real input signal is, in general case, also a random process. Therefore, in order to obtain adequate results, signals for cyclic ADC testing should be of the same class, i.e. should be random processes, and conversion quality measures ought to be averaged characteristics of random conversion errors. Such measures are known and used for analysis of the flash ADC performance (rms *error*, ENOB, EFR) [3-5]:

$$ENOB = N - \log_2 \frac{\sigma_{err}}{\sigma_{id}} = \log_2 \frac{FSR}{\sigma_{err}\sqrt{12}} \; ; \qquad EFR = R \; \frac{\sigma_{id}}{\sigma_{err}} \; . \tag{8}$$

Values σ_{id} and $R = 2^N$ in (8) denote the *ideal rms quantization error* (term from [3, p.5.5.2]) and reference effective resolution, respectively, of the ideal *N*-bit converter. Variable σ_{err} describes the *rms noise* in its actual non-ideal version being analysed. ENOB and ERF are equivalent measures of conversion quality and depend on the form and distribution of testing signal not directly but through *rms* σ_{err}. For this reason, they are much more universal than the quality measures based on the fitted sine-wave tests (total harmonic distortion THD, spurious free dynamic range SFDR and others [3]).

In works [6-8], particularities of IC ADC work were investigated on the basis of the following analytical expression for ENOB of cyclic converters:

$$ENOB_k = N_k = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{P_k}\right); \qquad k = 1,...,n \, , \tag{9}$$

where MSE $P_k = E[(V - \hat{V}_k)^2]$ determines the *ideal rms quantization noise* $\sigma_{k,id} = \sqrt{P_k}$ [3, p. 4.5.2] at the IC ADC output. Both computer analysis and laboratory experiments with IC ADC prototype, were carried out on the basis of (9) were theoretical MSE P_k was replaced by their empirical analogues:

$$\hat{P}_k = \frac{1}{M}\sum_{m=1}^{M}\left[V^{(m)} - \hat{V}_k^{(m)}\right]^2 ; \quad rms\ noise = \sqrt{\hat{P}_k} = \hat{\sigma}_{k,err} \, . \tag{10}$$

Results of computer analysis of ENOB (9) using MSE of estimates (10) have shown [6-8] high accordance of theoretic N_k and empirical $\hat{N}_k$ assessments of ENOB for ideal IC ADCs built using internal ADC_{In} with resolution $N_{ADC} \geq 4$ bits . For $N_{ADC} \leq 3$ bits , empirical MSE values are smaller than theoretic assessments for each $k = 1,...,n$, that is, these estimates are not optimal and can be improved. Plots in Fig. 4 illustrate the changes of theoretic (dash lines) and empirical (continuous lines) values of ENOB depending on the number of cycles for different ADC_{In} resolution $N_{ADC} = 1 \div 8$ bits . Experiments performed using random (see Fig. 5) and sine-wave testing signals gave also numerically close results under $N_{ADC} \geq 4$ bits, and noticeably different under $N_{ADC} \leq 3$ bits .

Another result significantly extending possibilities of CADC analysis and design is the established in [9] equivalence of the ENOB definition (9) (see also [6-8]) and expression (8) included in IEEE Standard [3]. This means that one may combine known methods of ENOB experimental assessment and results of theoretic consideration using approach [6-9]. More detailed analysis of the task has

shown that only the first form of ENOB (8) can be used for CADC performance assessment. The second form (ENOB as function of FSR / σ_{err}) is valid only for the flash ADC, and uniform distribution of quantization errors. Direct computer analysis of histograms of quantization errors at the IC ADC output has shown that it is weekly related with the initial distribution and form of input signals (see Fig. 6). Typical plots presented in Fig. 6 show that after the second cycle of conversion, distribution of quantization errors takes the form close to uniform. In the next cycles, this distribution quickly transforms into gaussian distribution with zero mean value and variance close to $\sigma_{k,id} = \sqrt{P_k}$. For this reason, for CADC, analogue of the second term in (8) should have the form: $ENOB = \log_2(FSR / 2\alpha\sqrt{P_k})$. This relationship and formulas (8), (4)-(7) can be used for accurate theoretic assessment of the reference values of ENOB N_k or EFR R_k of the ideal IC ADC (with ideal $\mathrm{ADC}_{\mathrm{In}}$). This value is necessary for actual ENOB (9) and EFR measurements using methods recommended in [3].

According to definition, ENOB represents directly the mean number of significant bits in codes of the samples. For this reason, ENOB is the most convenient for the analysis and adequate measure of conversion quality. However, formulas (8), (9) define ENOB as function of MSE P_k (or *rms noise* $\sigma_{k,err}$), which has to be measured first.

As it was shown in [9] (see also Sect. 1), there exists a possibility to evaluate actual and theoretic values of ENOB *directly*, omitting *rms noise error* measurements. This can be done by processing the binary codes of conversion error $err_k^{bin}(V) = \mathrm{mod}_2 \mid V - \hat{V}_k \mid$. Number of zeros before the first non-zero bit in $err_k^{bin}(V)$ determines position of the first erroneous bit in the code $\hat{V}_k$ of the sample V, that is, position $n_k^{LSB}(V)$ of its least significant bit. For random input signals, values $n_k^{LSB}(V)$ are also random. Fig. 7 presents the evolution of histogram of $n_k^{LSB}(V)$ values distribution versus number of cycles (intensity of white colour is proportional to the frequency of first unity appearance in corresponding positions, see also Fig. 4). The plot was built for 10000 random samples processed using computer model of the ideal IC ADC. Sharp low boundary of $n_k^{LSB}(V)$ values can be used for direct assessment of ENOB. Evaluations made in this way will be more accurate than those made on the basis of (8), (9).

Conclusions

Results of the work show that the origin of benefits of sub-optimal IC ADC over known cyclic ADC is the transition to the codes computing using long-word arithmetic and realisation of converters according to analytic results (1), (2), (4)-(7). The presented approach employs the measures of quality (ENOB and EFR) equivalent to those recommended in [3] and permits to develop precise and adequate methods of analysis and assessment of converters performance including direct measurement of ENOB.

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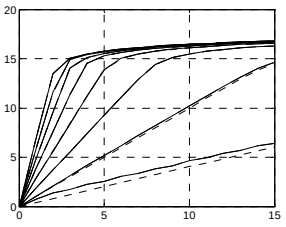

Figure 4. Theoretic and empiric ENOB vs number of cycles under $N_{ADC} = 1 \div 8$

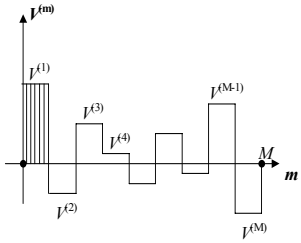

Figure 5. Random input signal used for IC ADC testing

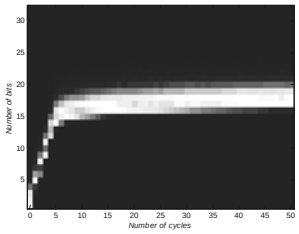

Figure 7. Distribution of $n_k^{LSB}(V)$ values vs number of cycles, used for direct assessment of ENOB

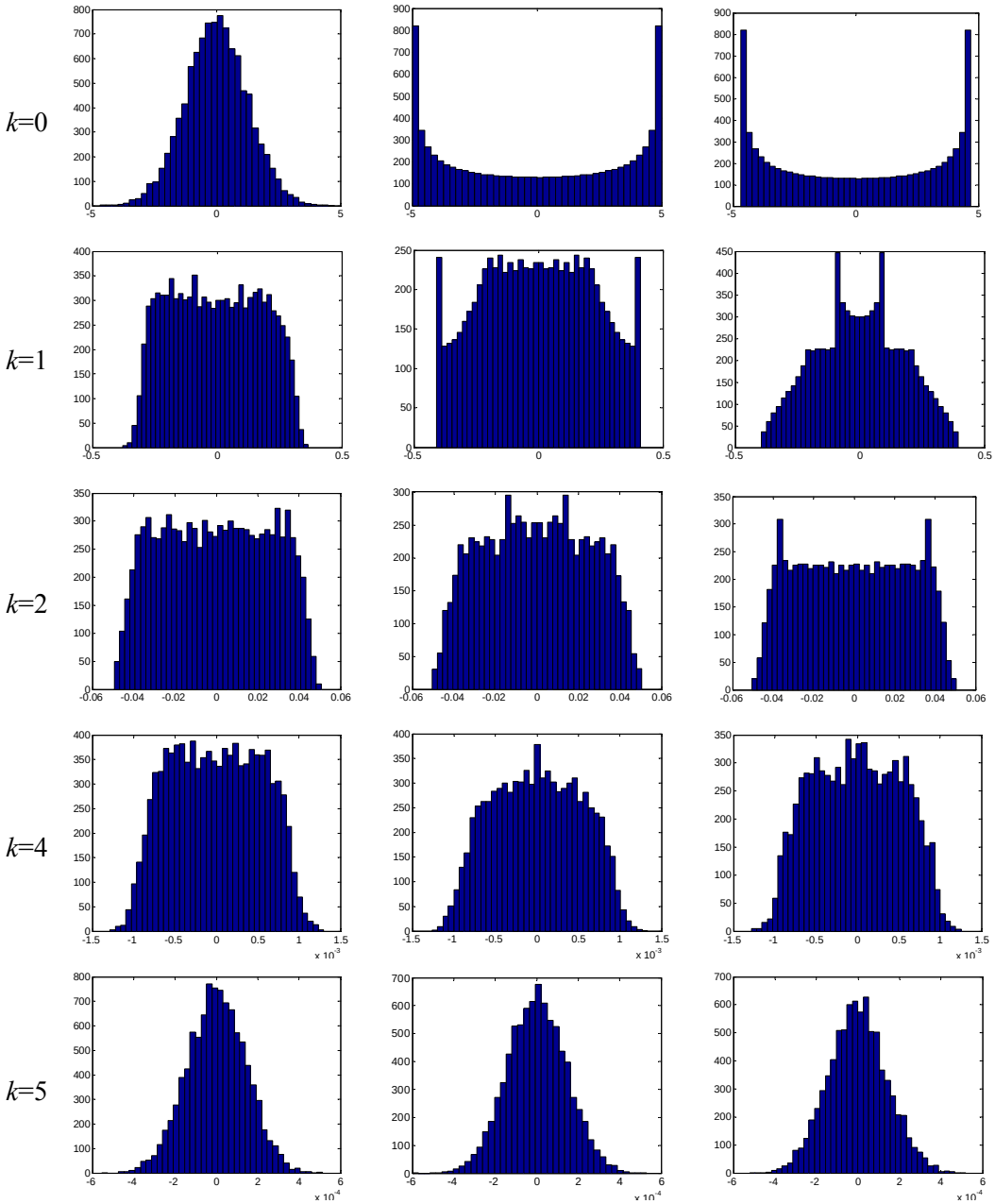

Figure 6. Histograms of testing signal (k=0) and histograms of conversion errors: $\hat{V}_k^{(m)} - V^{(m)}$ after k = 1,2,4,5 cycles of conversion (FSR=10, $\alpha = 4$, $\sigma_v^2 = 10^{-8}(FSR/\alpha)^2$, $N_{ADC} = 4$ bits, $M = 10000$). Plots in first column refer to the gaussian testing signal; in second column - to the full-scale sine-wave signal; in third column - to the sine-wave with amplitude $A = FSR/2 - LSB(ADC_{In})/2$.