High Dynamic Range Test-Bed for Characterization of Analog-to-Digital Converters up to 500 MSPS

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Abstract – A measurement set-up of for the characterization of analog-to-digital converters (ADCs) is described. The measurement set-up characterizes ADCs up to 16 bits at 350 MHz (option for >500 MHz). Testing dynamic performance of high-speed ADCs is regarded as difficult and expensive. By using existing state-of-the-art instruments in combination with specially designed amplifiers and filters, a high performance, cost efficient test-bed has been built-up. Practical performance corresponds to ADC datasheet and exceeds the performance obtained if using commercial instruments only. Consequently, the measurement results represent the true performance of the ADC without impact from the test-bed.

1. Introduction

There is a rapid development of the performance of state-of-the-art ADCs. Resolution and sampling rate are increasing continuously. Sampling rates in the high intermediate frequency (IF) range with sufficient dynamic range for communication applications were introduced about the turn of the millennium. Accordingly, there is an increased demand for high-performance measurement test-beds that are flexible to adapt to the evolution of the ADC performance.

Testing ADCs is complicated, time consuming and demands high-performance instrumentation [1]. There are no instruments to be found on the market that can accurately depict the true performance of today's state-of-the art ADCs. And still we may run into several pitfalls in high-speed ADC testing such as; coupling between digital outputs and analogue input in the $100\mu V$ range, getting good enough test signals and getting it to the ADC input, finding the appropriate test signals scenario and generate it, and avoid artifact noise injections to appear as false spuriouses; specially 2nd order distortion can be very hard to battle in the generated test signal.

2. Test-bed

The ADC test-bed is composed of commercial state-of-the-art instruments and components designed for this test-bed. Although it is designed to accomplish the general test set-ups described in IEEE standard 1241-2000 [2], it also can be used for general purpose. An overview of the test set-up is shown in Figure 1.

The clock signal is generated with a high quality signal generator. The clock signal can be adjusted via variable delays and filters to different requirements and applications. A recently developed vector signal generator (VSG) (R&S SMU200A) is the foundation to generate input signals. Specially made, ultra low distortion and low noise IF amplifiers and several custom-designed SAW filters and delay lines are used for signal conditioning. A frame grabber (FG) acquires data from the ADC at real time. In addition to this equipment a second signal generator and a signal analyser is part of the test set-up. The signal analyser is used to examine and verify input signals. All instruments are connected to a computer via GPIB or local area network (LAN).

A high-performance signal generator is a key component for successful ADC characterisation. Although it led to a larger investment, the signal generator can be used in various kinds of applications and is thereby standard equipment in most laboratories. The VSG combines up to two independent RF signal sources in one box, it also offers unrivalled RF and base band characteristics; such as -160dBc/Hz phase noise at offsets >1MHz, I/Q modulator with 200 MHz RF bandwidth and frequency from 100 kHz to 3GHz. Arbitrary signals are generated in a PC-program (e.g. Matlab) and thereafter transferred to the VSG, via LAN.
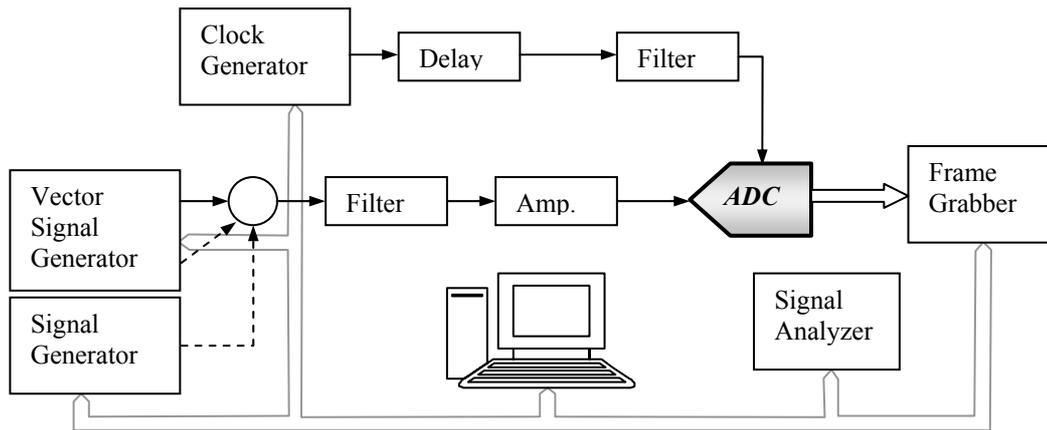
Figure 1: Schematic diagram of experimental set-up.

Even with a state-of–the–art signal generator, additional signal conditioning is required. Filters are used to clean-up spuriouses and noise from the test signal. However, the filters attenuate the signals, therefore it has to be amplified to obtain sufficient drive level to FS-0.5db, which can be as high as +16dBm on some newer ADC:s [3]. For that purpose ultra low distortion ADC driver has been designed with a frequency range of 20 - 300 MHz and 14dB gain. The amplifier ensures spectral purity even at high output levels by >80dBm output 2nd order intercept point (IP2), >49dBm IP3 and a noise level below −169dBm/Hz.

The FG acquires data from the ADC. A commercial state-of-the art logic analyzer can be a solution, but that imply a large investment for a narrow field of applications. The logic analyser solution have also been experiencing practical problems with false low level spuriouses by coupling from long parallel interconnection cables to the ADC under test. A design based on FPGA and high-speed memories is a cost efficient alternative. The FG interface to the ADC under test and in real-time record the binary represented samples at a maximum speed of 350 MHz (option for >500 MHz), width 16 bits, and depth 2 MSample (4 MByte). Samples are delivered from the ADC synchronously in binary format on low voltage differential signalling (LVDS) busses. After the acquisition process is completed the acquired data is uploaded to the PC over LAN for analyses.

3.   Results

The device under test is a 12-bit pipelined analog-to-digital converter intended for direct IF sampling that operates up to a 210 MSPS conversion rate. The digital outputs are LVDS to provide for lowest possible internal device and printed circuit board (PCB) coupling. Two different signals are presented as examples, both sampled at 210 MSPS. The first test signal is a <-100dB pure 10.3 MHz single tone, which is shown in Figure 2. The spurious free dynamic range (SFDR, [2]) is measured to 78.6 dB. This is the same figure as given in the data sheet for the ADC, which verifies that the measured results represent true device under test performance, and not any residuals from the test equipment and set-up.

Another interesting signal to study is a WCDMA signal; it is commonly used signals in telecommunication systems and thereby a possible application for high-speed ADCs. This signal is tricky from an ADC dynamic range perspective because it has simultaneously both a high excitation bandwidth and a high amplitude excursion (Cf in 7 – 9 dB range). In this measurement we chose a standard signal (3GPP FDD test model 4). The results are presented in Figure 3. The adjacent channel leakage ratio (ACLR, [4]) is an important and relevant parameter to evaluate the results because it is in direct proportional to the capacity achievable in a WCDMA cellular communication system. Moreover, ACLR (as well as noise power ratio) describes the dynamic performance of an ADC. As can be seen in Figure 3 the ACLR is 67.8 dB. A comparative measurement with a spectrum analyzer (sampled) gives 67 dB.
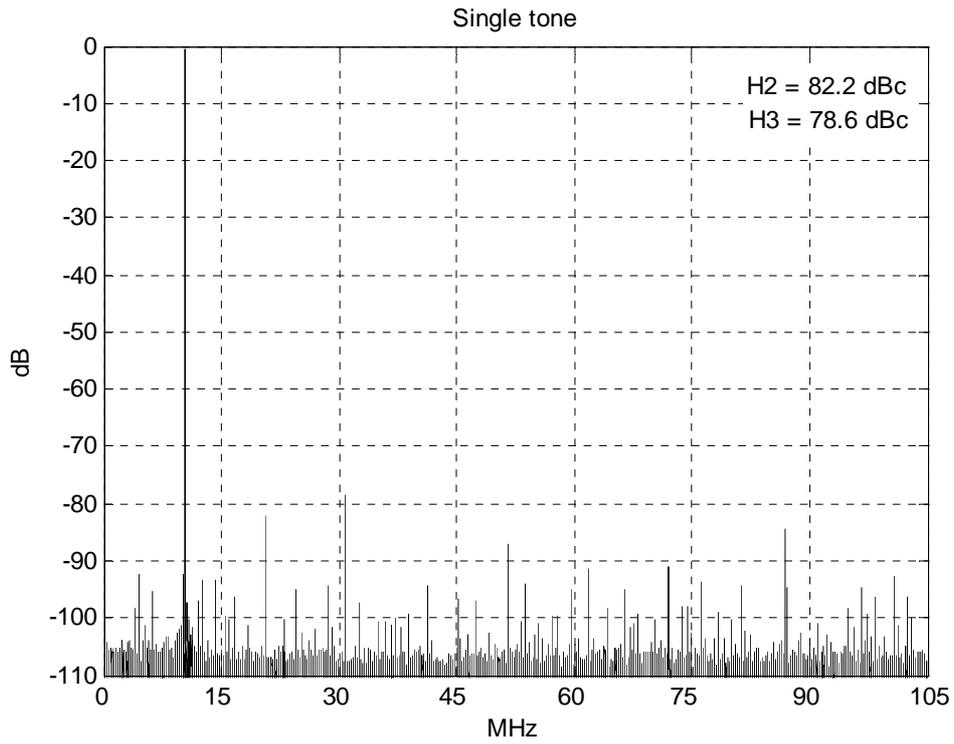
Single tone

H2 = 82.2 dBc
H3 = 78.6 dBc

Figure 2: Single tone 10.3 MHz.

W-CDMA

ACLR = 67.8 dB

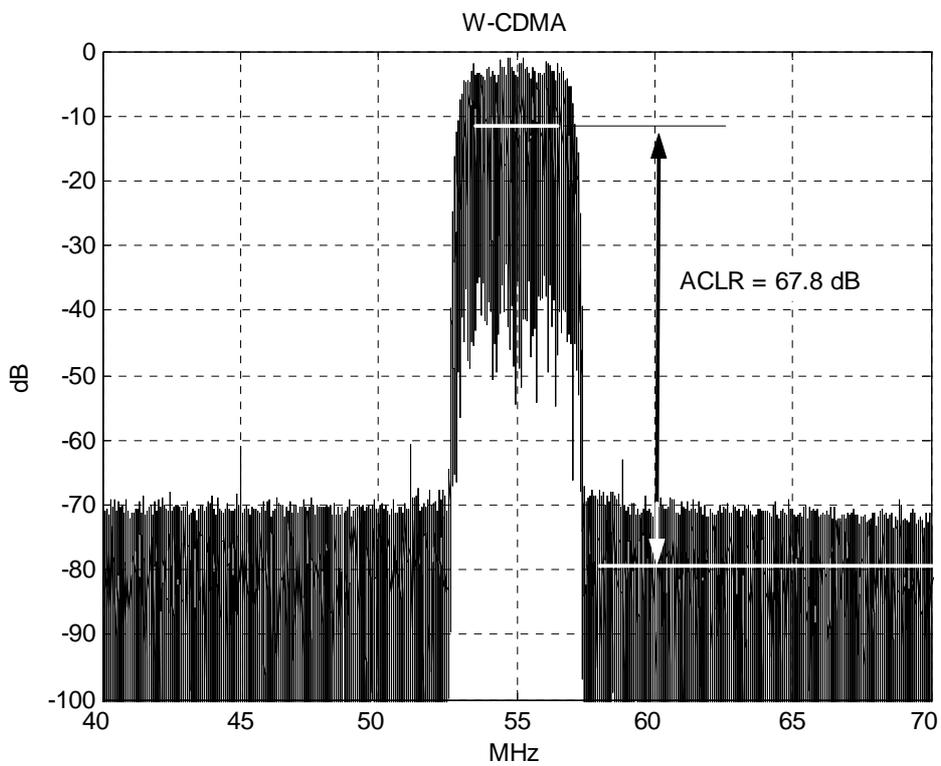Figure 3: WCDMA signal centred around 55 MHz.

4. Conclusions and contributions

An ADC measurement setup is described able to handle up to 16 bits and 350 MHz. To minimize the investment cost for the test-bed, a specially developed frame grabber is used to collect data from the ADC under test. Input signals to the ADC are of great importance. State-of-the-art signal generator together with specially designed signal conditioners ensure that appropriate test signals are generated and distributed to the ADC input.

One conclusion from Travis [1] experience is that it is difficult but not impossible to duplicate manufacturers test set-ups and results. The results presented in this paper shows that the suggested test-bed measure the merit figures of the ADC and not the test-bed, even though the sampling rate has increased more than 20 times since Travis article.

Acknowledgements

References

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