Modelling and Analysis of Influence of Internal Converters Nonlinearity in Adaptive Cyclic A/D Converters

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Abstract **-** The paper focuses on modelling and analysis of influence of internal converters nonlinearities in sub-optimal intelligent cyclic A/D converters (IC ADC) whose backgrounds and architecture were presented and analysed in works [1-5] and others. The knowledge of influence of internal A/D converter nonlinearities errors on IC ADC conversion performance enables determining requirements for $\mathrm{ADC_{In}}$ which are of crucial importance for design and practical implementation of IC ADC.

I. Introduction

Cyclic A/D converters (among other algorithmic, multi-pass, multi-fold, sub-ranging, etc.) belong to one of the most widely developing classes of A/D converters [6-8]. In works [1-5] and others, the new analytic approach to sub-optimal intelligent cyclic A/D converters (IC ADCs) design and optimization was proposed. The approach is based on mathematical models of analogue and digital parts of converter.

The main goal of this paper is working out effective tools enabling simulation analysis of IC ADC working in conditions of occurring nonlinearities of its internal A/D converter ($\mathrm{ADC_{In}}$) as well as quantitative (on the basis of measures proposed in [9]) preliminary assessment of the influence of these nonlinearities on IC ADC performance. Derivation of exact quantitative analytical evaluation of the influence of the $\mathrm{ADC_{In}}$ nonlinearities on global IC ADC performance is in almost all cases impossible due to both models of ideal $\mathrm{ADC_{In}}$ nonlinearity errors and additional nonlinear errors caused by its non-ideality. For these reasons, simulation analysis methods, which become more and more frequently used in A/D converters functioning and performance analysis [10], were applied in this paper. Finally, the paper presents simulation results obtained for typical examples of IC ADC components parameters.

II. IC ADC Functioning Principles

General block diagram of the sub-optimal IC ADC [1-5] is presented in Fig. 1.

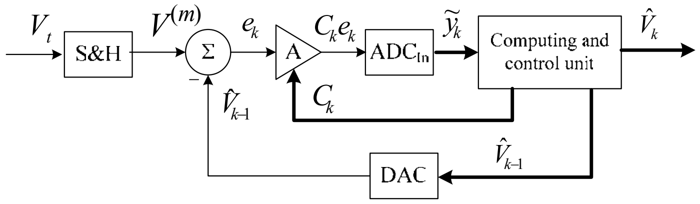

Figure 1. General architecture of the intelligent cyclic A/D converter

Each sample $V^{(m)}$ of the input signal is held at the output of the sample and hold block (S&H) during the time *T* necessary to complete *n* cycles of conversion. In each *k*-th cycle ($k=1,...,n$) of input sample V conversion (index *m* is further omitted), the computing unit calculates a new estimate (code) $\hat{V}_k$ of the input sample *V* using the estimate $\hat{V}_{k-1}$ calculated in the previous cycle and the current observation $\tilde{y}_k$ at the output of the internal fast low-bit (N_{ADC}-bit) A/D converter ($\mathrm{ADC_{In}}$) according to the common for all CADCs relationship:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k \,, \quad (k=1,...,n)\,. \tag{1}$$

Observations $\tilde{y}_k = C_k e_k + \xi_k$ are formed from residual signal $e_k = V - \hat{V}_{k-1} + v_k$. The residual signal e_k is amplified and converted by the internal $\mathrm{ADC_{In}}$. The ideal transfer characteristic of $\mathrm{ADC_{In}}$ is presented in Fig. 2. Noise ξ_k is the quantization noise of $\mathrm{ADC_{In}}$, whose variance is evaluated according to the formula $\sigma_\xi^2 = \Delta^2/12 = D^2 \cdot 2^{-2N_{ADC}}/3$, where D describes the boundaries of the $\mathrm{ADC_{In}}$ input range, N_{ADC} is its resolution (in bits), Δ is the $\mathrm{ADC_{In}}$ quantization interval (the least significant bit - LSB). Parameter C_k describes the gain of the amplifier (A) which increases with the number of conversion cycle. Noise v_k is a summary noise of the feedback D/A converter (DAC), the subtracting block (Σ) and other noises of the analogue part of IC ADC.

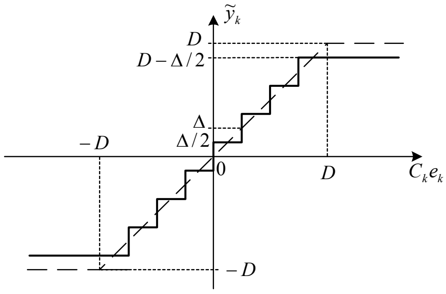

Figure 2. Ideal transfer function of the internal A/D converter - $\mathrm{ADC_{In}}$

The particularity of IC ADCs, which differs them from other cyclic ADCs (CADCs), is replacement of binary logic elements used for forming of input samples codes in conventional CADCs by a long-word computing unit (N_{comp} = 16, 24 or 32-bit arithmetic), which computes the codes of estimates in the form of fixed length (N_{comp} -bit) binary words. Each new estimate $\hat{V}_k$ is the result of adding the N_{comp} -bit code word $L_k \tilde{y}_k$ to the N_{comp} -bit estimate $\hat{V}_{k-1}$ calculated in the previous cycle of conversion. The algorithm of sub-optimal conversion includes (1) and relationships for the L_k coefficient and for the gain C_k of the residue amplifier (A):

$$L_k = \frac{C_k P_k}{\sigma_\xi^2 + C_k^2 \sigma_v^2}, \qquad C_k = \frac{D}{\alpha\sqrt{\sigma_v^2 + P_{k-1}}}, \tag{2}$$

where $P_k = E[(\hat{V}_k - V)^2]$ is the mean square error (MSE) of conversion and, in sub-optimal case, is calculated according to the formula:

$$P_k = \frac{\sigma_\xi^2 + C_k^2 \sigma_v^2}{\sigma_\xi^2 + C_k^2(\sigma_v^2 + P_{k-1})} P_{k-1}. \tag{3}$$

Initial conditions of the algorithm (1)-(3): $\hat{V}_0 = V_0$ and $P_0 = \sigma_0^2$, are determined by the mean value and maximal power of the input signal. Parameter α in (2) is determined by the assumed probability μ of CADC saturation and satisfies the equation: $\Phi(\alpha) = (1-\mu)/2$, where $\Phi(\alpha)$ is the Gaussian error function. For IC ADC employing the algorithm (1)-(3), converter performance attains maximal theoretically achievable (boundary) values [1-4]. Such converters utilize completely hardware and software resources to improve the quality and speed of conversion to maximal achievable values. Converters of this type can be integrated as peripheral function blocks in microprocessors or in other mixed analogue/digital systems.

III. Modelling and Analysis of Nonlinearities Influence on IC ADC Performance

The $\mathrm{ADC_{In}}$ nonlinearities were modelled taking into account a step-wise form of $\mathrm{ADC_{In}}$ transfer function under its distortions both in case of differential nonlinearity errors and in case of integral nonlinearity errors, which models are described below. Contrary to previous works [1-5], to evaluate the IC ADC performance, test methods and measures based on [9] were used. Test signals had sine-wave form: $V^{(m)} = V_{\max}\sin(2\pi f_i m)$, $(m = 1,\ldots,M)$, where $V_{\max}$ is a half of full-scale range of IC ADC and f_i is normalized frequency of the test signal – in experiments presented below: $M = 1024$ and $f_i = 53/1024$. Apart from simulations with sinusoidal test signal, many computer experiments with Gaussian and uniformly distributed random test signals were performed (see for example [1-5]). Other values of parameters assumed in presented below computer simulations were as follows: $V_{\max} = 5$, $V_0 = 0$, $\sigma_0 = 1.25$, $\alpha = 4$, $D = 1.25$, $N_{DAC} = 16$. It was also assumed that noise v_k is conditioned only by quantization noise of the feedback internal D/A converter (DAC). Then, its variance $\sigma_v^2 = \Delta_{DAC}^2/12 = D_{DAC}^2 \cdot 2^{-2N_{DAC}}/3$, where N_{DAC} is DAC resolution and DAC output range

$[-D_{DAC}, D_{DAC}]$ is equal to the input range of IC ADC $D_{DAC} = V_{\max}$.

In the experiments, the following measures [9]: signal to noise and distortion ratio (SINAD), effective number of bits (ENOB) and total harmonic distortion (THD) were used to compare actual IC ADC (working in conditions of occurring nonlinearities of its internal A/D converter) performance to the ideal IC ADC performance. To estimate SINAD and ENOB values both results in time and frequency domain were used and compared.

Values of ENOB were also directly estimated on the basis of the difference between the long-word reference binary code of the input sample V and the code of its estimate $\hat{V}_k$ obtained using IC ADC [11]. The sequence of first identical bits in the estimate $\hat{V}_k$ and in the reference code determines direct evaluation of ENOB. In this paper, the minimal number of first identical bits obtained for M samples of test signal was assumed as a direct measure of ENOB. To estimate such a number, the code word $err_k^{bit} = \mathrm{mod}_2 |V - \hat{V}_k|$ proposed in [11] (see also [12]) was used.

Apart from the measures mentioned above, direct FFTs of converted signal were also analysed in order to assess the IC ADC conversion quality changes under $\mathrm{ADC_{In}}$ nonlinearities.

A. Differential nonlinearity

DNL nonlinearity errors were modelled as independent random displacements of each $\mathrm{ADC_{In}}$ quantization threshold (a similar model was used in [13]). The displacements were uniformly distributed around nominal values of thresholds as in Fig. 3. The interval $\varepsilon \cdot [-\Delta/2, \Delta/2]$ of displacements distribution is determined by ε. For large DNL ($\varepsilon > 1$), overlapping of the quantization levels can occur and then missing code errors appear.

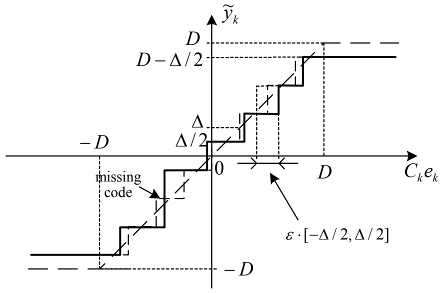

Figure 3. DNL errors model of $\mathrm{ADC_{In}}$ transfer function

The upper row of Fig. 4 shows ENOB of IC ADC as a function of cycle number (k) obtained for different values of DNL errors coefficient ε (changing from 0 to 2) and different values of $\mathrm{ADC_{In}}$ resolution $N_{ADC} = 2, 4, 8$. The respective plots of ENOB obtained in its direct evaluation described above are presented in lower row.

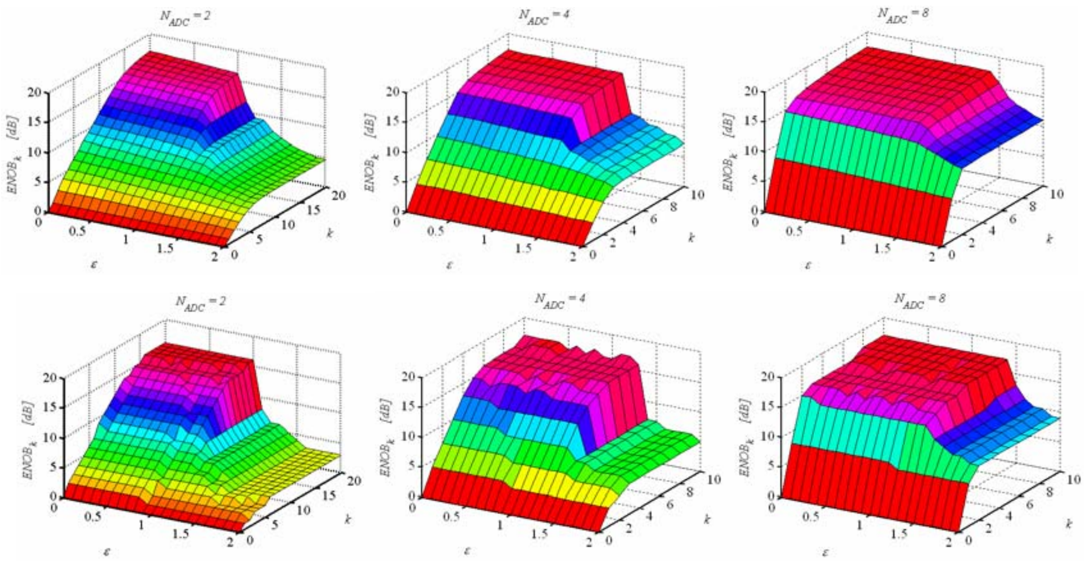

Figure 4. ENOB of IC ADC as a function of cycle number (k) and DNL errors coefficient (ε) for different values of $\mathrm{ADC_{In}}$ resolution N_{ADC}: indirect evaluation – upper row, direct evaluation – lower row

The presented plots show a wide range of tolerance of IC ADC performance for DNL errors of $\mathrm{ADC_{In}}$. The tolerance range increases for the greater values of $\mathrm{ADC_{In}}$ resolution. For assumed parameters of converter the admissible values of ε coefficient, for which IC ADC preserve its conversion performance, are as follows: for $N_{ADC} = 2$: $\varepsilon \in [0,\ 1]$, for $N_{ADC} = 4$: $\varepsilon \in [0,\ 1.3]$ and for $N_{ADC} = 8$: $\varepsilon \in [0,\ 1.4]$. In Fig. 5 plots of THD obtained in the same simulations are presented. Taking into account that the considered resolutions of $\mathrm{ADC_{In}}$ are quite low, the results of simulations show that the used in IC ADC internal A/D converters have not too excessive requirements for their DNL.

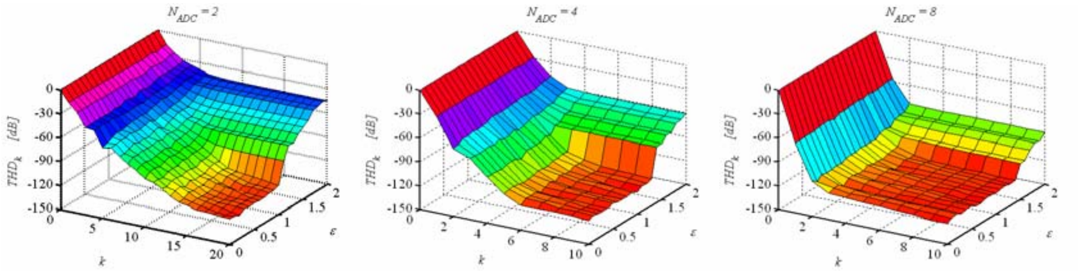

Figure 5. THD of IC ADC as a function of cycle number (k) and DNL errors coefficient (ε) for different values of $\mathrm{ADC_{In}}$ resolution N_{ADC}

Subsidiary to results from Fig. 4 and 5, the FFT plots of converted by ICADC signal as a function of cycle number (k) for different values of DNL errors coefficient (ε) and $\mathrm{ADC_{In}}$ resolution $N_{ADC} = 4$ are presented in Fig. 6. The exemplary FFT plots show that the increase of DNL errors of $\mathrm{ADC_{In}}$ causes the raising of the noise floor in FFTs, but does not influence the appearance of other harmonic components in the converted signal spectrum.

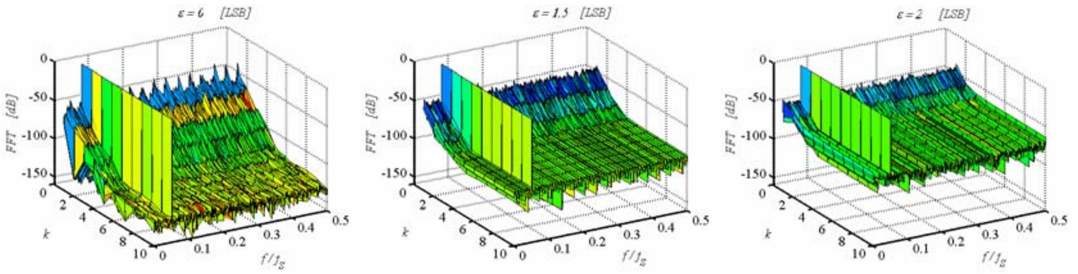

Figure 6. FFT of signal converted by IC ADC as a function of cycle number (k) for different values of DNL errors coefficient (ε) and $\mathrm{ADC_{In}}$ resolution $N_{ADC} = 4$

B. Integral nonlinearity

The assumed model of integral nonlinearity (INL) errors of internal A/D converter ($\mathrm{ADC_{In}}$) is shown in Fig. 8. The nonlinearity was modelled by the power function of $x^{1+\lambda}$ type, where λ determines the nonlinearity level, similarly as in [14].

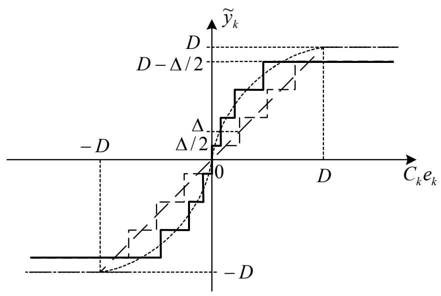

Figure 7. INL errors model of $\mathrm{ADC_{In}}$ transfer function

The results of simulation in ENOB form are presented in Fig. 8. As seen in Fig. 8, the admissible values of λ coefficient, for which IC ADC preserve its conversion performance, are as follows: for $N_{ADC} = 2$: $\lambda < 2.25$ [LSB], for $N_{ADC} = 4$ and $N_{ADC} = 8$: $\lambda \in [-1.5,\ 1.5]$ [LSB]. Fig. 9 shows corresponding THD plots. Similarly to analysis of influence of DNL distortions on changes in IC ADC performance, the presented results confirm that requirements for the ADC_{In} INL characteristics, especially for low bit A/D converters $N_{ADC} \leq 8$, are not too excessive. Not too excessive requirements allow to use as ADC_{In} fast and cheap converters with quite large nonlinearity errors, of course in range of admissible nonlinearity deviations, whose maximal values can be estimate using the elaborated simulation tools.

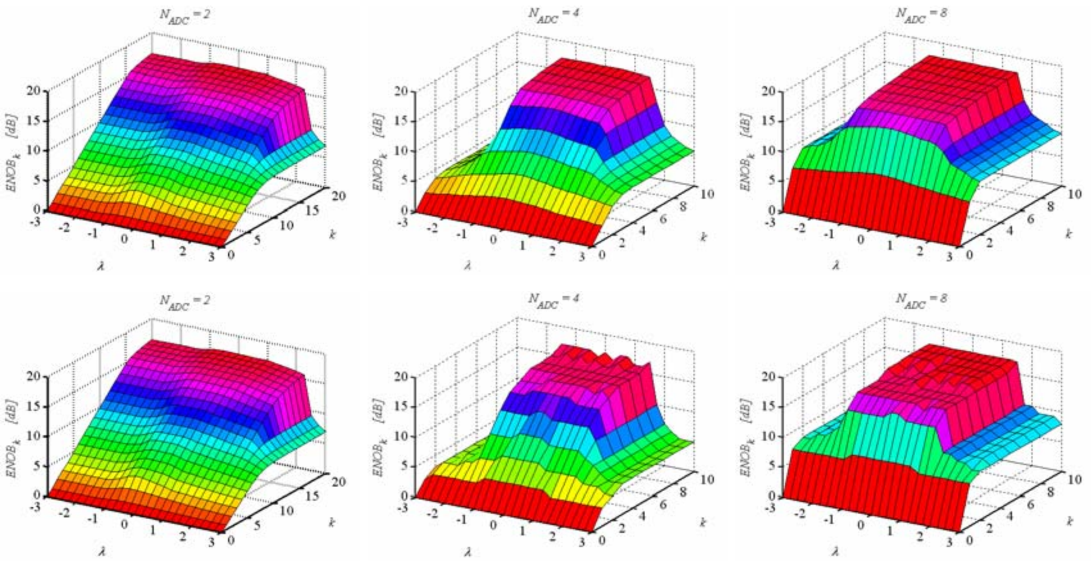

Figure 8. ENOB of IC ADC as a function of cycle number (k) and INL errors coefficient (λ) for different values of ADC_{In} resolution N_{ADC}: indirect evaluation – upper row, direct evaluation – lower row

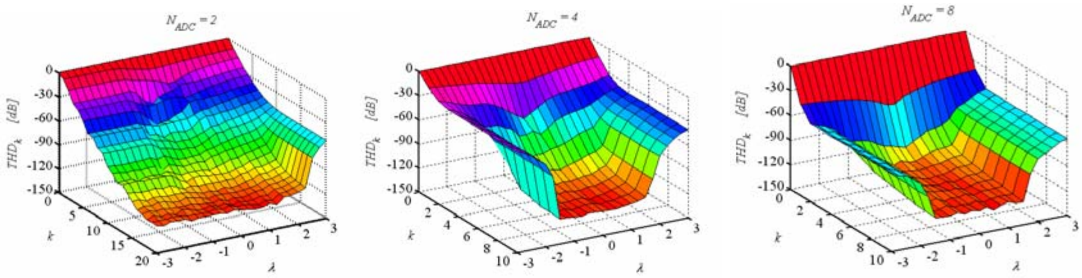

Figure 9. THD of IC ADC as a function of cycle number (k) and INL errors coefficient (λ) for different values of ADC_{In} resolution N_{ADC}

Similarly as in DNL type distortions, the FFT plots of converted by ICADC signal as a function of cycle number for different values of DNL errors coefficient λ and ADC_{In} resolution $N_{ADC} = 4$ are presented in Fig. 10. Contrary to DNL, the exemplary FFT plots show that the increase of INL errors of ADC_{In} results, from determined values of λ, in the appearance of the other harmonic components in the converted signal spectrum.

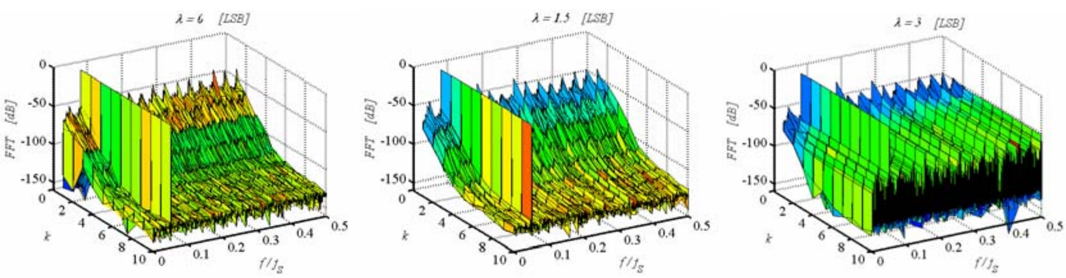

Figure 10. FFT of signal converted by IC ADC as a function of cycle number (k) for different values of INL errors coefficient (λ) and ADC_{In} resolution $N_{ADC} = 4$

IV. Conclusions

The results presented in the paper extend results of works [3-5] and give the new arguments to the claim that sub-optimal IC ADCs performance depends weakly on the non-idealities of the transfer function of their internal converters ADC_{In}. The experiments confirmed the closeness of the assessed in simulation experiments values of ENOB to their theoretical boundaries even for significantly large deviations, determined for the assumed IC ADC parameters values, of real characteristics of ADC_{In} from the ideal ones. This effect is a result of usage of the adaptive algorithm for estimate computation. The elaborated simulation tools enable assessment of technical requirements for the internal A/D converters quality, i.e. admissible boundaries of their non-linearity, for which IC ADCs do not lose crucially their performance.

References

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