Performance analysis of the PXI-based bus communication of a fast digital integrator for magnetic measurements

P.Arpaia[1,2], G. Spiezia[2,3]

[1] *Department of Engineering, University of Sannio, Corso Garibaldi 107, 82100 Benevento, Italy. Ph : +39 0824 305804-17, Fax: +39 0824 305840, E-mail: arpaia@unisannio.it*
[2] *CERN, Dept. of Accelerator Technology, Magnet Electrical Systems & Instruments, CH 1211, Genève 23, Switzerland.Ph : +41 22 76 79775.*
[3] *Department of Engineering, University of Naples - Federico II, Via Claudio 21, 80125 Napoli, Italy; E-mail:Giovanni.Spiezia@cern.ch*

Abstract- A procedure for bottlenecks analysis of the PXI bus communications of an automatic measurement station is proposed. The experimental case study of the Fast Digital Integrator (FDI), a general purpose data acquisition and processing card developed at the European Organization for Nuclear Research (CERN), is illustrated.

I. Introduction

PXI (PCI eXtensions for Instrumentation) is a rugged PC-based platform, combining PCI electrical-bus features with the modular, eurocard packaging of CompactPCI, by further adding specialized synchronization buses and key software features [1]. Such features allow PXI bus to be widely used for PC-based measurement and automation systems for industrial applications, as well as for scientific experiments [2]-[5].
The theoretical maximum throughput of the PXI bus corresponds to the PCI performance: 132 MB/s for a 32-bit bus operating at 33 MHz [1], [6]. In reality, the actual throughput of a PXI-based system depends on many factors: (i) the system hardware architecture, i.e. the presence of an extender, the position of the controller inside the rack, and so on, (ii) the number of PCI devices present in the host PC, (iii) the PC main board, (iv) the reading/writing technique, i.e. Direct Access Memory (DMA), burst mode or single access; (v) the software to address the device, and (vi) the device local bus.
The above factors are not always well specified. In addition, the usual evaluation of the maximum throughput rate does not take into account the addressing cycles and is referred only to the best case of write operations in DMA mode. Conversely, read operations are made slower by a further turn-around cycle after the addressing aimed at data retrieving [6].
The major issues in PCI performance reading are described in [7]. Advanced readout controllers for PCI-based systems are capable of reaching a throughput rate up to 30 MB/s without DMA [8]. PCI performance with DMA, at varying the buffer size, is analyzed in [9].
In synthesis, the recognition of state of art shows that the bus performance varies mainly according to the hardware architecture of the PCI-based system and to the retrieving-data technique (DMA, burst mode, or single operation).
In this paper, a procedure for analyzing the bus performance and pointing out possible bottlenecks in a PXI-based architecture of an automatic measurement system is proposed. Such a procedure is highlighted through the experimental application to the Fast Digital Integrator (FDI), a general-purpose 6 U PXI-based board for data acquisition and digital signal processing developed at the European Organization for Nuclear Research (CERN) in order to face up the new challenging requirements of magnetic measurements [10]. In the following, (i) the *procedure* of PXI communication analysis, and (ii) the *FDI case study* are highlighted.

II. PXI communication analysis

A. Procedure

The analysis of the PXI communication bus is based on the identification of the PXI chain of initiators-targets. Such a chain may be quite different depending on the system architecture. The PXI/CPci cards, usually allocated in an external rack, are the final target of the communication chain controlled by a host unit. The host unit can be:

- a CPci controller plugged in the rack;

- a standard PC. In this case an extender kit is needed to link the PCI bus to the PXI bus and the final target (the PXI card) is not reached directly by the first initiator (PC).

The final target uses a local bus manager to interface the PXI bus. Such a role can be implemented into an FPGA with a custom design or can be demanded to a dedicated integrated chip.
Once the architecture is defined, the PXI bus timing is studied by checking the signals *FRAME* and *TRDY* (Target Ready) pointing out the beginning and the end of the transaction *Initiator-Target*, respectively.
Such an analysis allows the main bottlenecks related to the architecture to be identified.

B. A case study: the FDI at CERN

The proposed procedure is highlighted by considering, as a case study, a measurement station with several FDIs, other PXI/CPCI boards, such as DAC cards, actuator controller cards, and interface cards for RS232 or GPIB bus [11]. The cards are mounted in a PXI rack acting as an extension of the host PCI bus.
The architecture of the experimental set up is shown in Fig. 1. In this case, a kit (PCI 8570 and PXI 8570) is used to extend the host PCI bus. The FDI interface with the PCI bus is handled via a PCI bridge (PLX 9030), which allows the transactions on the local bus to be programmed by the user in a very simple way. The bridge between PCI and local bus decouples the problems of FPGA design development from PCI interfacing, leading to a design more reliable and easier to maintain.
In the above architecture, initiator and target are not coupled directly on the communication bus (Fig. 1). The PCI bridge is configured as a direct slave, thus the final target is the PCI9030 chip on the FDI board and its initiator is represented by the extension kit (PCI/PXI 8570). On the other side, the extension kit behaves as the target of the bus master of the host pc which represents the actual initiator.
The procedure of the performance analysis of the overall system has to consider all the series of transactions shown in Fig. 2: (i) the function call is transferred to the CPU that initiates the bus transfer; (ii) once ready, the PCI extension initiates the transfer on the bus extension; and (iii) finally, the PCI bridge is addressed to handle the local bus transactions.
The transaction time analysis of the communication chain allows the most critical steps for further improvements to be detected. The assertion of the digital signals *FRAME* and *TRDY* (Target Ready) indicates the beginning and the end of the transaction *Initiator-Target* respectively, such as shown in Fig. 3 for a read operation [6].

III. Experimental results

The above-described architecture was analyzed by measuring the transactions through a state logic analyzer. First, the transaction between the PXI extension card (PXI8570) and the PCI bridge card (PCI 9030) was analyzed. In Fig. 4a, the local bus signals (*ADS*, *RD*, *WR*) and the PCI signals of the PXI extension card (*FRAME*, *CB[0:3]*, and *TRDY*) are reported for a reading operation. The function call, based upon the commercial API provided by the PCI bridge manufacturer, operates the reading of two

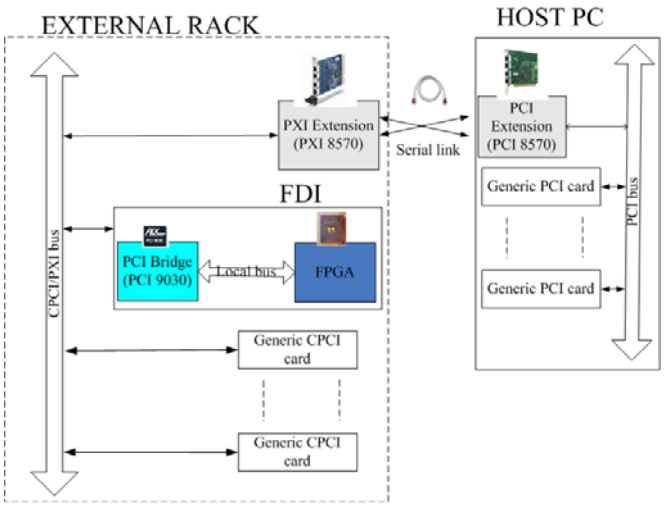


Figure 1. Architecture of the PXI-based communication system of the FDI.

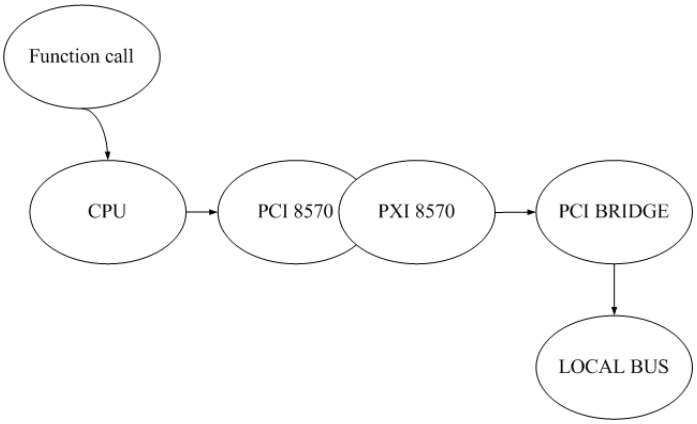


Figure 2. Procedure of the initiator-target chain of the FDI PXI communication.

consecutive 32-bit words, mapped on the FPGA memory. The operation is led without any burst mode on the local bus, neither on the PCI bus (two addressing cycles are needed). The reading cycle of a 32-bit word lasts about 3.3 μs corresponding to a throughput rate of about 1 MB/s, faraway from the theoretical limit (132 MB/s). However, considering that the reading cycle ends when the *TRDY* signal is de-asserted, the cycle should take about 500 ns, corresponding to a throughput rate of 8 MB/s. Therefore, an improvement of a factor 8 could be pursued.

Moreover, without understanding the source of this communication bottleneck causing a latency time of about 2.8 μs between two reading cycles, any hardware improvement on the local bus, as well as the use of the burst technique, would be useless. The source of the bottleneck must be investigated by analyzing the initiator-target chain reported in Fig. 2.

Thus, a further measurement was carried out by picking up the signals on the host PCI bus in order to look in depth at the transactions from the initiator CPU to the target PCI8570-PXI8570. The measurement shows that the extension card PCI 8570 is not addressed at the first bus cycle and the operation does not end normally when the target PXI8570 is ready, but further bus cycles are still required. The supplementary bus accesses cause a time overhead of about 2 μs. The time elapsed between the *TRDY_PCI8570* last rising edge of the first read cycle and the consecutive falling edge of the same signal (~750 ns) indicates the latency time required by the CPU for closing and opening a read cycle on the bus.

It lasts about 750 ns. This time interval is not affected by the software because the API function has requested the reading of two consecutive 32-bit words.

Excepting for the transaction from the function call to the CPU, the performance analysis highlighted all the steps of the initiator-target chain of the FDI communication bus by showing that the main communication bottleneck arises from the addressing of the extension kit (Table I).

A further study with a PCI analyzer was carried out to investigate the failure of the extension kit addressing. In fact, the monitor of all the PCI bus signals allows the status at the end of each bus cycle to be decoded.

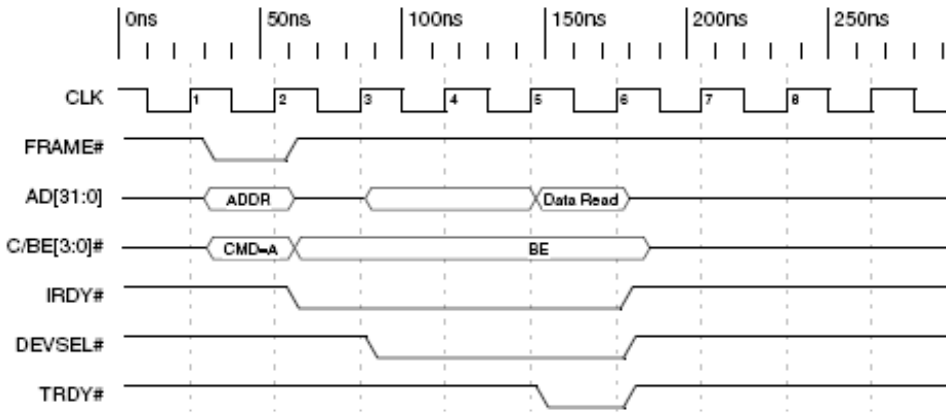
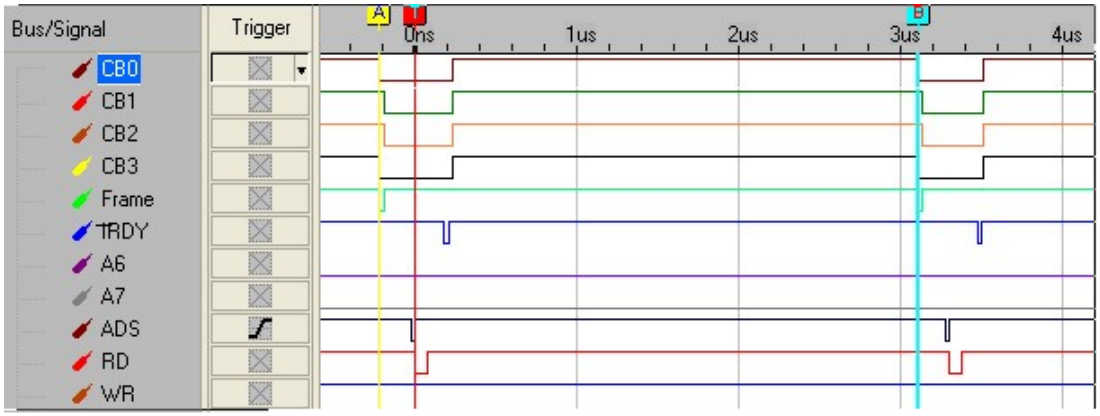
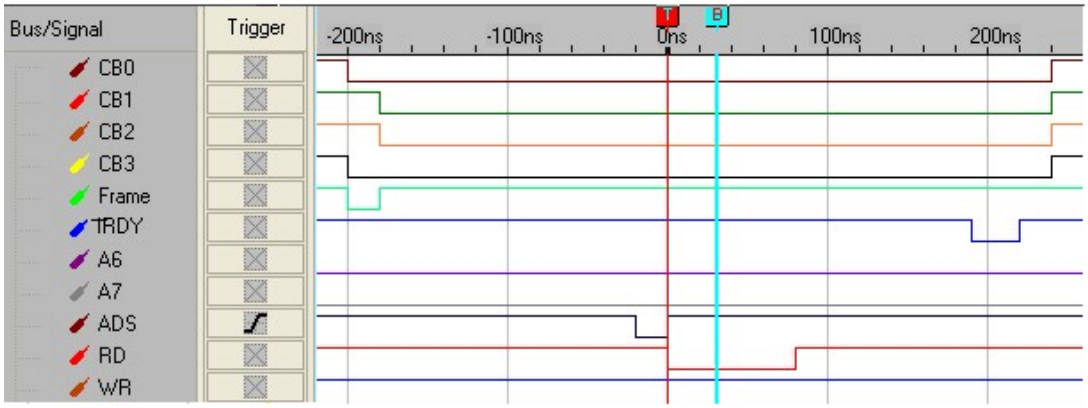


Figure 3. PCI signals for a single read operation.



(a)



(b)

Figure 4. Local bus read operation: a) two consecutive reading; b) zoom on the read cycle.

In Fig. 6 the report of two reading cycles is depicted. The bus cycles fails because the target (the extension kit) is disconnected without data (*Tdwod*) and a *Target Retry* message (TR) is sent. Such a latency time is introduced by the extension kit in case of single access operation, as confirmed by the manufacturer. This analysis confirms that the time to close and open a read cycle is about 750 ns. In more details, it takes 210 ns to drive the PCI signals and 500 ns to perform a new single access. The operation is managed by the firmware of the bridge PCI9030.
The analysis showed that the extension kit choosen decreases deeply the performance in case of single access operation on the bus.

Table I. Time transactions of the FDI communication architecture.

Open-close time of a read cycle	*Addressing of the extension kit and coming back*	*Addressing of the local bus and coming back*	*Local reading cycle*
750 ns	2 μs	400 ns	100 ns

IV. Conclusions

A procedure for analyzing communications bottlenecks on PXI bus in automatic measurement station is proposed by considering the FDI architecture based on a PCI/PXI extension kit. The investigation method identifies the initiator-target transactions on the bus because PCI performance depends mainly on the hardware components and on the overall system architecture. The FDI communication bus chain was measured by means of a state logic analyzer by highlighting that the main bottleneck is due to the addressing of the PCI/PXI extension kit.

Acknowledgments

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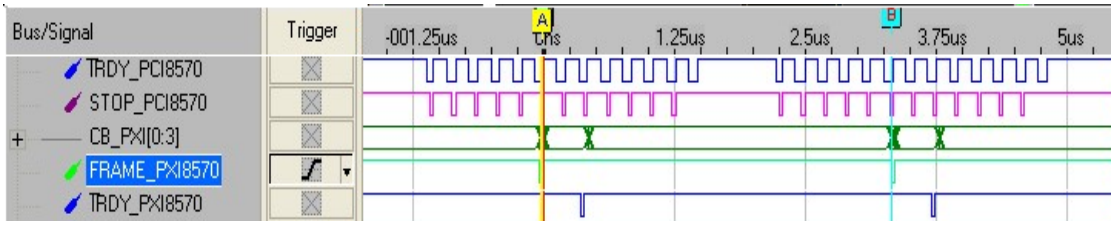

Figure 5. Host PCI bus signals (PCI8570) and extension bus signals (PXI8570)

suggestions.

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Sample	TimeRel	Wait	Size	Burst	Command	Address	Data	Status	Err	INTx#	Ext74
TRIG:	0.0ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
1:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
2:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
3:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
4:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
5:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
6:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
7:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
8:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
9:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
10:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
11:	210.7ns	.	AD32	.	MemRd	FD008000	.....	TdwodT--		----	1111
12:	210.7ns	.	AD32	.	MemRd	FD008000	0000000K	--		----	1111
13:	752.5ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
14:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
15:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
16:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
17:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
18:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
19:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
20:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
21:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
22:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
23:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
24:	210.7ns	.	AD32	.	MemRd	FD008004	.....	TdwodT--		----	1111
25:	210.7ns	.	AD32	.	MemRd	FD008004	0000000K	--		----	1111

Figure 6. Analysis of the PCI bus transactions by a PCI analyser

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