17th Symposium IMEKO TC 4, 3rd Symposium IMEKO TC 19 and 15th IWADC Workshop
Instrumentation for the ICT Era
Sept. 8-10, 2010, Kosice, Slovakia

Improved digital phase measurement

Cristian Zet [1], Cristian Foşalău[1]
[1] *Faculty of Electrical Engineering, Technical University "Ghe Asachi" of Iasi, Iasi, Romania, czet@ee.tuiasi.ro*

Abstract – The paper presents a new method for measuring the phase shift between two signals. The method can be used as full FPGA implementation or in microcontroller based systems. In contrast with the classic method, where the measuring time is obtained from the reference clock signal by dividing it with high value factors, this method gets the measuring time from one of the signals by dividing it with a small factor, 10 for example. Thus, it results a dramatically diminish of the measuring time or a significant error improvement.

1. Introduction

There are various ways to measure the phase shift between two signals [1], [2], [3], [4]. The classic diagram of a digital phasemeter [2] is presented in Fig. 1.

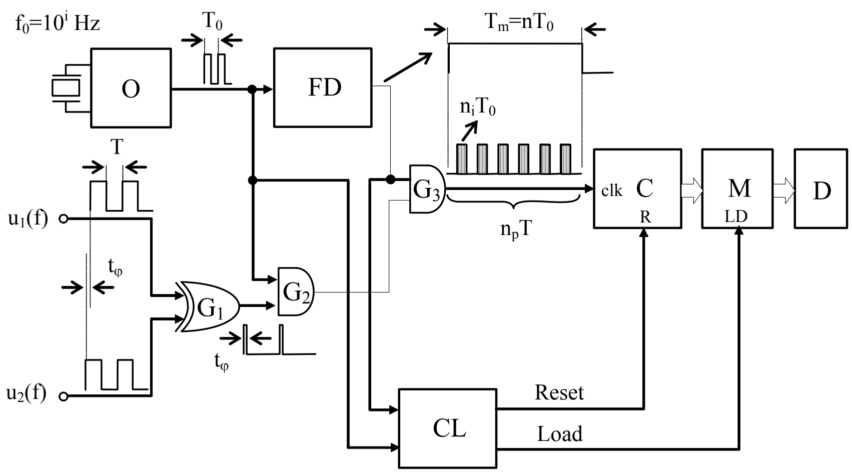

Figure 1. The classical diagram of the digital phasemeter

First the signals which phase shift is being measured pass a XOR gate G_1. At its output a pulse train is obtained, each pulse having the length equal with the time shift between the two signals. The gate G_2 replaces each pulse in the pulse train with a packet of clock pulses with the same duration, in each packet having n_i clock pulses. From the clock signal coming from the oscillator O, is obtained the measuring time (T_m), with a frequency divider FD, that allow after the gate G_3 a n_p number of packages towards the counter C. Along the measuring period T_m the pulses reach the pulse counter C, and the result at the end is:

$$N = n_p \cdot n_i = 2 \cdot \frac{n \cdot T_0}{T_0} \cdot \frac{t_\varphi}{T} = 2 \cdot n \cdot \frac{t_\varphi}{T} \tag{1}$$

where n is the dividing ratio of FD. If n is 180, the result N is exactly the phase between the two signals.
The error that affects the measurement is generated by the fact that the frequency of the input signal does not fit exactly in the measuring time, thus resulting in a loss of maximum a packet of pulses, that means a loss of n_i pulses. This leads to a relative error:

$$\frac{\Delta\varphi}{\varphi} = \frac{n_i}{N} = \frac{\frac{t_\varphi}{T_0}}{2 \cdot n \cdot \frac{t_\varphi}{T}} = \frac{1}{2 \cdot n} \cdot \frac{f_0}{f} \tag{2}$$

2. New method description

The new method is based on two ideas: the first one is to get the measuring time from the input signal in order to fit the period of the input signal in it, and the second is to count also the pulses during the $T/2-\varphi$ period. The idea is not easy to be implemented with logic circuits, but while things are moving nowadays toward FPGA, the realisation is more facile. Another way to materialize it is in a microcontroller based system using two counters and software computing.
The block diagram of the phasemeter is shown in Figure 2.

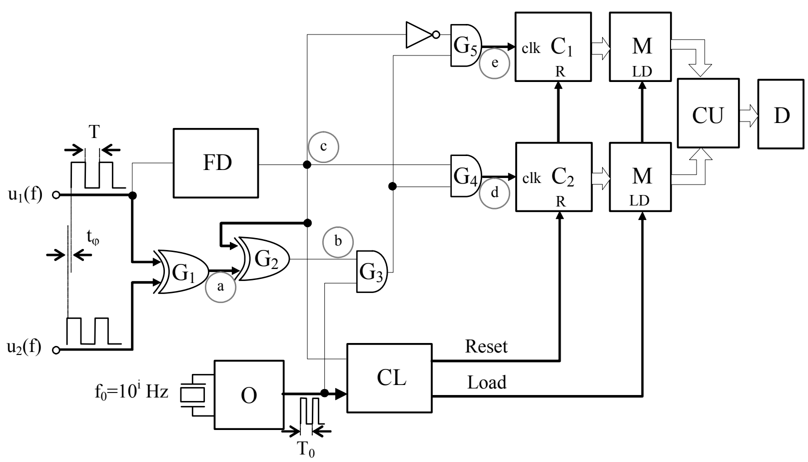

Figure 2. The block diagram of the new digital phasemeter

The signal $u_1(f)$ is taken as reference signal. The frequency divider (FD) divides with N one of the input signals in order to obtain the measuring time. The divider ratio can be any integer value, but experiments showed that a factor of N=10 will ensure enough accuracy "c". The gate G_1, having the same role as in the classic method, is used to obtain a pulse train having the pulse length equal with the time shift between the two input signals (waveform "a" in Figure 3). The gate G_2 will let the G_1 signal unchanged for the first half of the measuring time and will invert the signal for the second half (waveform "b" in Figure 3). The gate G_3 replaces every pulse with a short train of clock pulses "d". The pulses corresponding to the two halves of the measuring period pulses are then guided, via G_4 and G_5 towards the two counters (C_1 and C_2), "d" and "e". At the end of each half, the content of each counter is stored in the corresponding memory M and after this the counter is cleared. The computing unit CU is computing the phase from the two values, which is finally available on the display D.
The waveforms associated to the above schematic are available in Figure 3 where:
- Clk is the clock signal from the oscillator (period T_0)
- $u_1(f)$ and $u_2(f)$ are the input signals whose phase difference has to be measured
- a, b, c, d, e are signals indicated in Figure 2.

During the first half (c in logic 0) of the measuring period, C_1 counts the clock pulses along the phase shift time (t_φ), resulting N_1 counts. The pulses of the second half ("c" in logic 1) correspond to $T/2-t_\varphi$ and are collected in counter C_2, resulting N_2 counts.

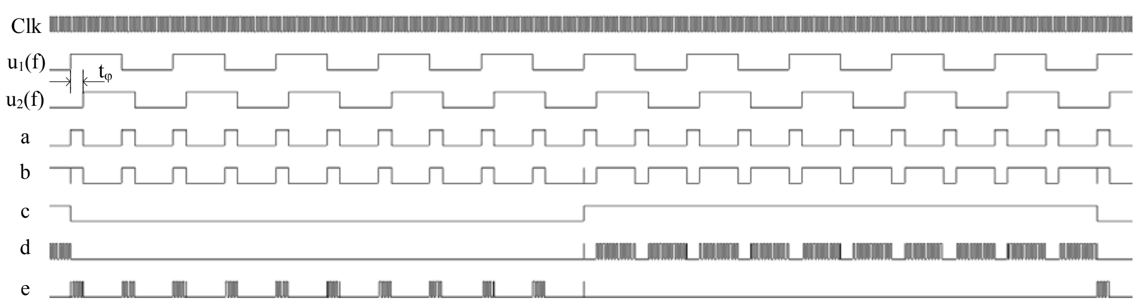

Figure 3. The waveforms associated to the new digital phasemeter

3. Mathematical support

As it presented above, the information about the phase between the two input signals is contained in the two numbers: N_1 and N_2. The computing unit CU must compute the result from these two numbers.
During the first half of the measuring time (signal "c" is logic 0), at the output of the gate G_1 n_{p1} pulses will come out:

$$n_{p1} = \frac{N \cdot T}{2} \cdot \frac{2}{T} = N \tag{3}$$

For the second half n_{p2} pulses will be present at the output of G_1, where:

$$n_{p2} = \frac{N \cdot T}{2} \cdot \frac{2}{T} = N \tag{4}$$

At the output of the gate G_3, instead of the n_{p1} and n_{p2} pulses we have packets of clock pulses. First n_{p1} packets have:

$$n_{i1} = \frac{t_\varphi}{T_0} \tag{5}$$

and last n_{p2} packets have:

$$n_{i2} = \frac{\frac{T}{2} - t_\varphi}{T_0} \tag{6}$$

where T_0 is the clock period.
Now we can compute the numbers of pulses resulting in each half of the measuring time:

$$N_1 = n_{i1} \cdot n_{p1} = N \cdot \frac{t_\varphi}{T_0} \tag{7}$$

$$N_2 = n_{i2} \cdot n_{p2} = N \cdot \frac{\frac{T}{2} - t_\varphi}{T_0} \tag{8}$$

N_1 and N_2 are the numbers stored in the counters C_1 and respectively C_2. The phase can be computed from these two numbers:

$$\frac{N_1}{N_1 + N_2} \cdot 180 = \frac{N \cdot \frac{t_\varphi}{T_0}}{N \cdot \frac{t_\varphi}{T_0} + N \cdot \frac{\frac{T}{2} - t_\varphi}{T_0}} \cdot 180 = \frac{t_\varphi}{T} \cdot 360 = \varphi \tag{9}$$

The equation (9) can be computed either by a hardware computing block, either by a processor, and the result will be numerically equal with the phase between the two signals in degrees.

4. THE ERROR ESTIMATION

The method produces the result with certain error. In contrast with the classic method, that can loose one whole package of clock pulses (2), here it can be lost only one pulse per packet, the total number of lost pulses being *N/2* for each half of the measuring time.
The total maximal error can be estimated as:

$$\frac{\Delta\varphi}{\varphi} = \frac{N_2}{N_1 + N_2} \cdot \left(\frac{\Delta N_1}{N_1} + \frac{\Delta N_2}{N_2} \right) \tag{10}$$

or replacing the absolute error with *N* (the dividing factor of the frequency divider FD):

$$\frac{\Delta\varphi}{\varphi} = \frac{N}{N_1} = \frac{T_0}{t_\varphi} \tag{11}$$

Figure 4 plots the estimated error from equation (11) for a 1.4 kHz signal frequency and 4.3MHz clock frequency, the phase being varied from 5 to 175 degrees.

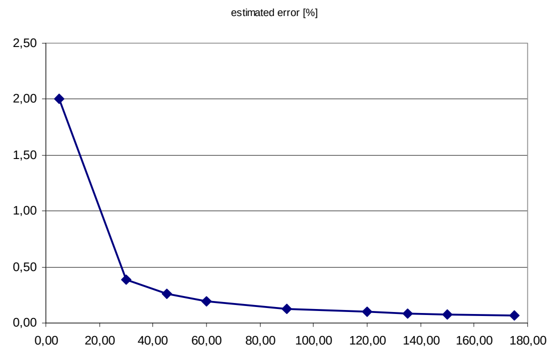

Figure 4. Plot of the estimated error (equation (11))

A significant increase can be observed for small angles (under 30 degrees), but this can be overcome by interchanging the signals on the inputs.

5. Experimental data

The circuit has been implemented in an Altera Flex10k FPGA and tested with square waves internally generated. The frequency of the input signals was 1.4kHz and the clock frequency was 4.3MHz as above. The frequencies were chosen in order to overcome the perfect fitting of the clock in the signal frequency. Experimental data are provided in the following table.

Table 1. Experimental data for new phasemeter

t_φ [μs]	φ_{REF} [deg]	φ [deg]	ε_φ [%]
10	5	5,02	0,40
60	30	30,06	0,20
90	45	45,02	0,04
120	60	60,05	0,08
180	90	89,96	0,04
240	120	119,95	0,04
270	135	134,98	0,01
300	150	149,96	0,03
350	175	174,94	0,03

The experimental error is plotted in Figure 5 (diamond). We noticed that the error bellow 0.1% for angles larger than 45 degrees, almost constant, and it is slightly increasing for smaller angles, up to 2% for 5 degrees.

The results have to be compared with the classic method presented in paragraph 1. The classic phasemeter has been implemented in the same FPGA and tested with the same signals and with almost the same measuring time. In the first case the measuring time was 7.2ms, and in the second was 10ms. The data collected are presented in Table 2.

Table 2. Experimental data for classic phasemeter

t_φ [μs]	φ_{REF} [deg]	φ [deg]	ε_φ [%]
10	5	5,30	6,00
60	30	30,80	2,67
90	45	44,46	1,20
120	60	59,26	1,23
180	90	91,43	1,59
240	120	118,62	1,15
270	135	134,05	0,70

300	150	149,10	0,60
350	175	175,23	0,13

It is easy to notice that the error is slightly bigger than the new proposed method, sometimes one order of magnitude higher. This error is also plotted in Figure 5 (circle).

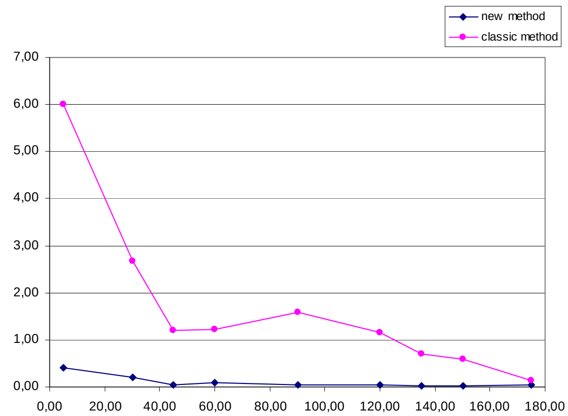

Figure 5. Plot of experimental errors [%]: ♦ new method, • classic method

4. Conclusions

A new method for digital phase measurement has been presented. It can be easy implemented in either FPGA-s or in microcontroller systems and it minimizes both, the measuring time and the error.

Acknowledgments

The paper has been supported from project PN2 72157/2008 funded by the Ministry of Education and Research from Romania.

References

[1] M. Sedlacek, M. Krumpholc, ,"Digital measurement of phase difference - a comparative study of DSP algorithms", *Metrology and Measurement Systems*, Polish Academy Of Sciences Committee on Metrology And Scientific Instrumentation, Vol. XII – No. 4/2005, pp.427-428

[2] Nemat A.,"A Digital Frequency Independent Phase Meter.", *IEEE Transactions on Instrumentation and Measurements*, Vol.39, No.4, PP 665 - 666, August 1990

[3] S.M. Mahmoud," Error Analysis of Digital Phase Measurement of Distorted waves", *IEEE Transactions on Instrumentation and Measurements*, Vol. 38,, No. 4, 1 February 1989, pp. 6-9

[4] K. M. Ibrahim and M. A. H. Abdul-Karim, "A novel digital phase meter," *IEEE Transactions on Instrumentation and Measurements,* Vol. 36, pp. 711-716, September 1987.