

Embedded Hardware to Synchronize the Triggering of Measurement Instrument Networking

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Abstract- The research is devoted to investigate about the coordination in the time domain of the operations executed by the Measurement Instruments (MIs) connected by Hardware Interface (HI) to the node of the Distributed Measurement System. A new architecture of HI is proposed to trigger the MIs in order to (i) avoid the random effects of concurrency of the software processes running on PC, (ii) reduce the upper bound of the execution time of the procedure running on Real Time Operating System, and (iii) shorten the random time delay to detect the trigger condition, introduced by the polling cycle on the Programmable Logic Device (PLD). The proposed architecture of the HI includes the PLD as wireless interface, and the board designed to synchronize the trigger. It is equipped by PIC, Counter block, and Clk block. Experimental tests validate the HI pointed out and the proposed strategy to trigger the MIs in the synchronized modality.

I. Introduction

The synchronization is a new challenging requirement that emerges also in the contest of industrial automation application [1]-[2], monitoring system [3]-[4], inspection and management of strategic power plant [5]-[8], computer network [9]-[10] and sensor network applications [11].

Nowaday, synchronized measure is a new service achievable by Distributed Measurement Systems (DMSs). The practical requirements of the synchronization concern with the correlation in the time domain of the measurements given by independent Measurement Instruments (MIs) connected to the nodes of the DMS. They involve (i) the detection of the time delay among independent measurements, (ii) the compensation for the delay, and (iii) the implementation of the protocol to guarantee the accurate synchronized operation.

The synchronization can be obtained in two different ways: (i) sharing the common control signal or (ii) sharing the common sense of time.

The accuracy of the synchronization obtained with the first solution is strongly depending on the behavior of the communication network. A predictive behavior can be obtained avoiding the packet collision into the network [12]. The accuracy of the synchronization obtained with the second solution strongly depends on the performance of the synchronization protocol used into the network. Usually, the MI is interfaced to the node of the DMS by Hardware Interface (HI) and the synchronization procedure operates on the clock, internal or external, of this last. Therefore, the HI works in synchronized modality with the accuracy level granted by the particular synchronization method used.

In the synchronization contest, one of the problems not taken into account by the standard [13] is the random time delay introduced by the HI. In [14]-[19] is shown that it is possible to reduce the standard deviation of the random time delay by modifying both the controlling process of the MI and the operating system.

In [20] was proposed the use of the Programmable Logic Device (PLD) to interface the MI to the DMS and overcome the limitation arising from different solutions based on software strategies. The advantage is that the concurrency causes among the software processes are completely avoid, and, consequently, the execution time of the interesting procedure devoted to the command execution for the MI should be deterministic.

Nevertheless, operating conditions can occur making not deterministic the detection of the trigger for the MI. In [21] is highlighted that if the trigger occurs after the check on the PLD, it will be detected at the next check. In this case, the final result is that the start time of the command execution is random and depends on the time delay between the trigger and the trigger check. In the paper a different HI is taken into account to interface the MI to the node of the DMS. The proposed architecture of the HI includes the PLD as wireless interface, and the board equipped by PIC, Counter block, and Clk block. The board is designed to synchronize the trigger by reducing the random variation of the time delay and the polling cycle to check the trigger condition.

The paper is organized as follows. Initially, the performed operations by the proposed HI are described. Successively, the actual realization of the proposed trigger synchronizing board is described. For sake of completeness, the synchronization phase by means of the proposed HI is abstracted. Finally, the results of

experimental tests are shown to validate the HI pointed out and its usefulness to trigger the MIs in synchronized modality.

II. Hardware interface to reduce the random time delay variation by avoiding the polling cycle

The new proposed HI is used to synchronize the MIs with sub- μ s accuracy. Fig.1 shows the block diagram of the hardware architecture of the proposed HI connecting the MI to the node of the DMS. It is constituted by: (i) board Rabbit RCM4400W [22], and (ii) trigger synchronizing board equipped by PIC16F84a, 8-bit Counter block, Clk block.

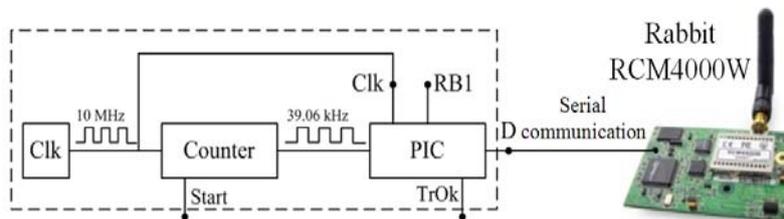


Figure 1. Block scheme of the proposed HI architecture reducing the random time delay variation to check the trigger condition.

A. Performed operation by the proposed HI

The board Rabbit RCM4400W receives from the Master PC on the WiFi interface the information about the *trigger condition* to execute the triggering of the MI, and transmits it on the serial interface, pin D, to the PIC [23]. The software running on the PIC checks the *trigger condition* by means of the interrupts arising from the Counter block, and sends the *trigger signal* to the MI by rising the signal on the pin RB1. The Clk block is used as reference clock to temporize with high accuracy the Counter block and the commands execution into the PIC. The Counter block is used as frequency divider. Indeed, because the Clk block has frequency f_c equal to 10MHz and the number of bits of the Counter block is 8bit, the PIC receives the interrupt each 25,6 μ s, while the elementary operations to check the trigger condition are performed by the PIC in 12,5 μ s. In this way the end of performed operations is guaranteed before that successive interrupt occurs.

The pins TrOk and Start are used to perform the synchronization of the Counter block of two different HIs by means of the external Starter block, as shown in Fig.2a). The Starter block is constituted by one logical port *and*. Indeed the PICs left the logical state of the pin TrOk high for all the synchronization phase duration. While each input does not receive the high signal level from the pin TrOk of the two HIs, the signal at the output pin Ps is low. Once received all the agreements, the output signal at the pin Ps is high. This signal is also used to reset the Starter latches.

On each board, a latch is connected to the pin Start of the Counter block to ensure the correct functioning, once the Starter is disconnected.

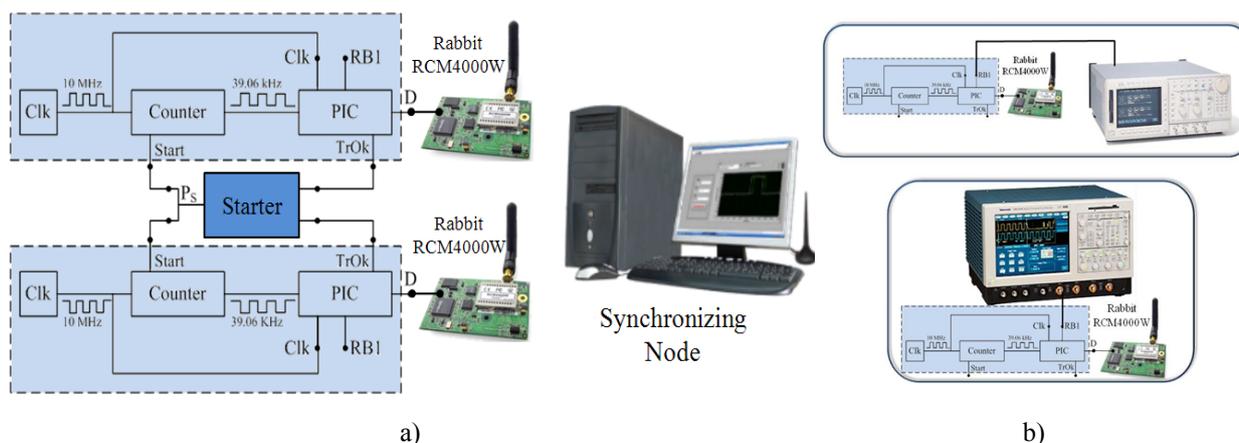


Figure 2. a) Block scheme of the connection into the Synchronization Phase of the HIs, and b) block scheme of the connection among HIs and MIs into the Triggering Phase.

B. Actual realization of the trigger synchronizing board

The scheme of the designed board is shown in Fig.3 and Fig.4. In the Tab.1 the component characteristics are denoted.

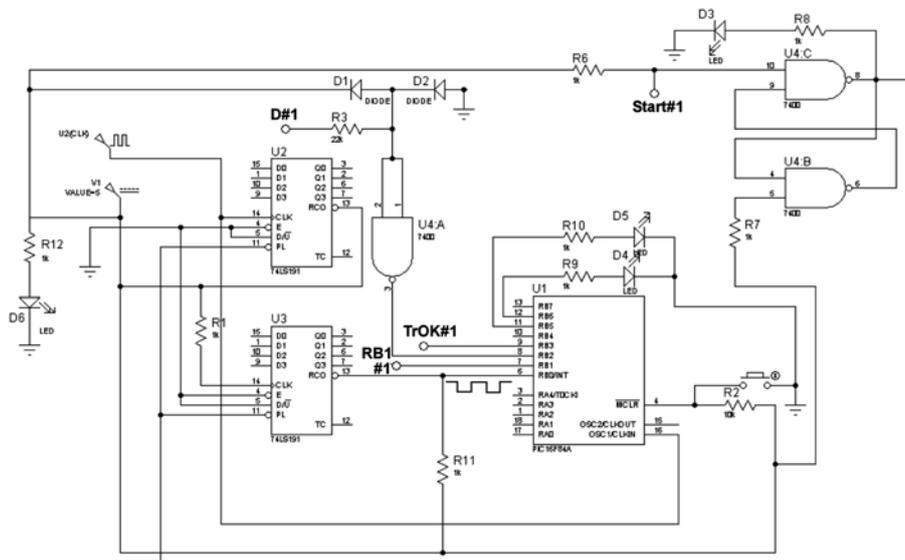


Figure 3. Circuitual scheme of the trigger synchronizing board.

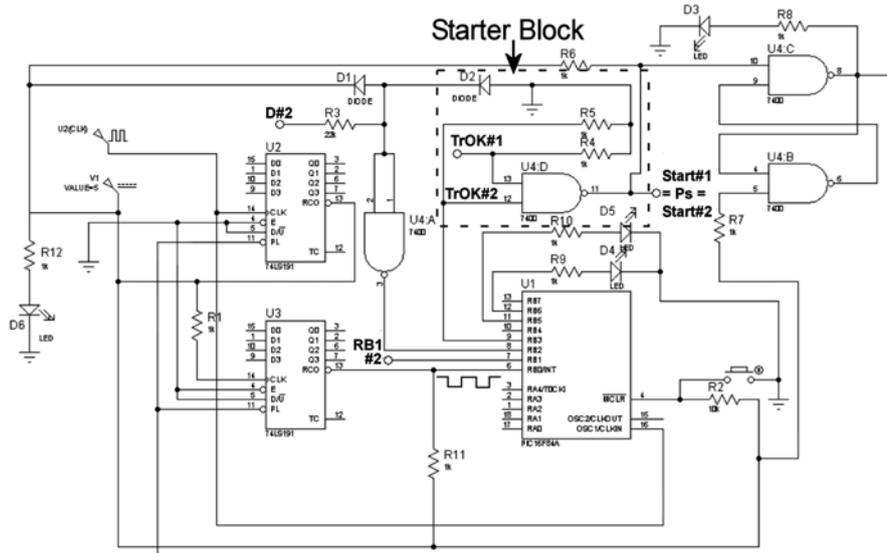


Figure 4. Circuitual scheme of the trigger synchronizing board including the Starter Block.

The CLK signal is obtained by the Pierce oscillator. In particular the logic *not* is obtained by using (i) integrated circuit HCF4049UBE, (ii) resistor with value equal to $(10.0 \pm 0.5)\text{k}\Omega$, and (iii) two capacitors with value equal to $(22.00 \pm 0.44)\text{pF}$. The oscillators are the XTAL003164 10MHZ. In order to grant the same operative temperature, both the oscillators are into silicon bath.

C. MI Synchronization by means of the proposed HI

Fig.2a) shows the block scheme of the hardware connections of the performed operations in the First Phase in which the synchronization is performed between two HIs. Fig.2b) shows the block scheme corresponding to the Second Phase in which

Table 1. Electrical components of the board.

Resistor	R1=R2= $(10.0 \pm 0.5)\text{k}\Omega$
	R3= $(22.0 \pm 1.2)\text{k}\Omega$
	R4-R12= $(1.00 \pm 0.05)\text{k}\Omega$
Diode	D1-D2=1N4001
	D3-D6=LED
Integrated Circuit	U1=PIC16F84A
	U2-U3=74LS191
	U4=74HC00
Capacitor	C1=C2= $(22.00 \pm 0.44)\text{pF}$

two HIs are employed to synchronize two stand alone MIs [10].

The First Phase, Fig.2a), involves the Master PC to send the trigger condition at each HI, and the external Starter block to synchronize the start of the counting between two HIs. The trigger condition corresponds to the number $n_c = n_{itp}2^N$, with n_{itp} number of interrupts that the PIC must to count before to execute the command for the MI, and N bit number of the Counter block. The Master PC evaluates n_{itp} according to the frequency of the Clk block and the bit number of the Counter block. The Master PC sends, also, the information concerning with the number of repetitive measures n_m with period v_m . If only one measure is requested, is $n_m=1$. Once set into the PIC the internal variable n_{itp} , n_m , v_m , the HI is ready. Therefore, it sends to the Starter block the *grant to start* signal by rising the voltage level on the pin TrOk, Fig.2a).

Once received all the grants, the Starter block sends to the two Counter the signal *Start to count*, by rising the voltage on the pin Ps. Because each HI receives the signal in the parallel modality, the time delay between the gate opening of the two Counter blocks can be assumed negligible. Consequently, the interrupt sent by each Counter block is synchronized with the other ones, and, as a consequence, the corresponding PICs are forced to operate in synchronized modality.

Once the Counter block starts the count, the Second Phase begins, Fig.2b). Each HI is: (i) disconnected from the external Starter block, (ii) moved to the measurement place, and (iii) connected to the MI. During this operation mode, each PIC receives the interrupt from the Counter block in synchronized modality with other PICs.

The operations performed by the PIC at each interrupt are the following: (i) the internal variable i is incremented, and (ii) i equal to n_{itp} is checked. When this condition occurs, HI sends the trigger signal to the MI by the pin RB1, and the new values are upgraded $n_{itp}=n_{itp}+v_m$, $n_m=n_m-1$. If the condition $n_m=0$ occurs, the measurement procedure is considered done and the PIC is waiting for new trigger condition from the Master PC.

III. Experimental tests

Experimental tests are executed in order to validate (i) the correctness of the performed operations by the trigger synchronizing board, and (ii) the usefulness of the HI to trigger the MIs.

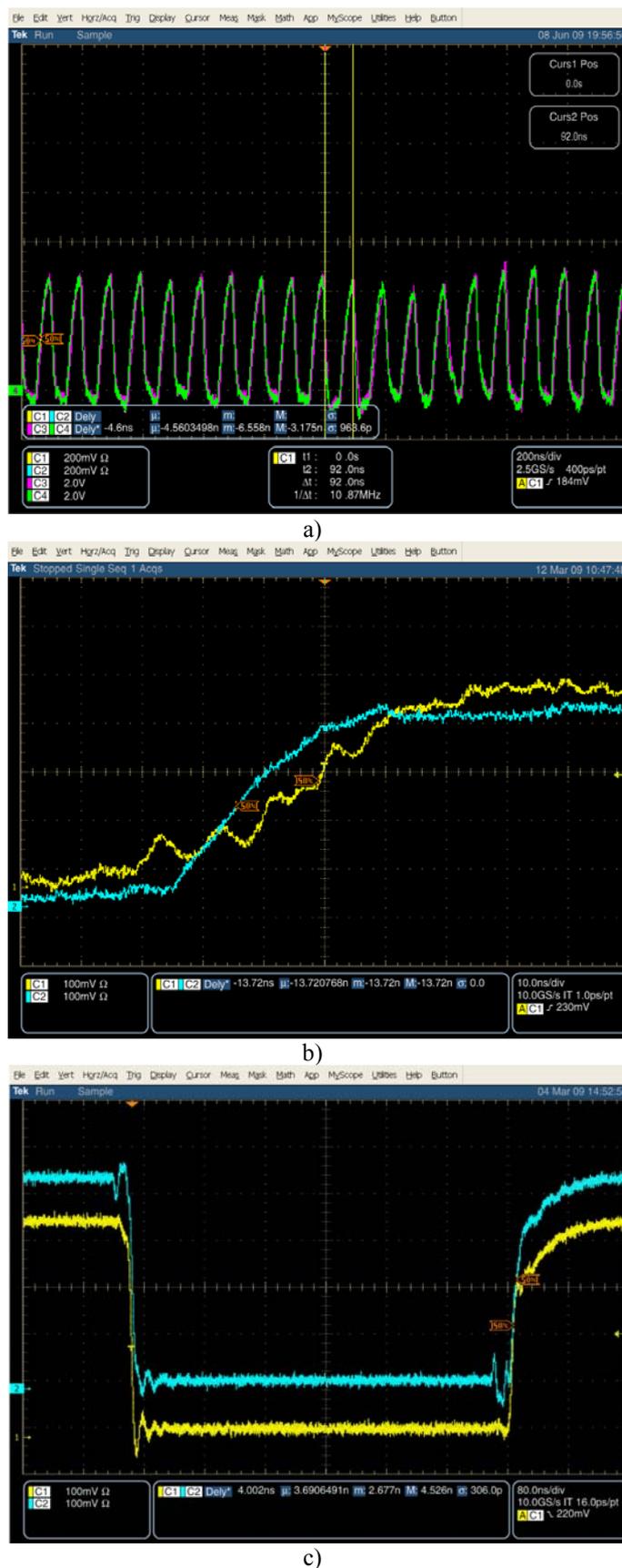


Figure 5. Snapshot of a) clock signals received by Counters, b) start signal received by the Counters, and c) output signals from the Counters.

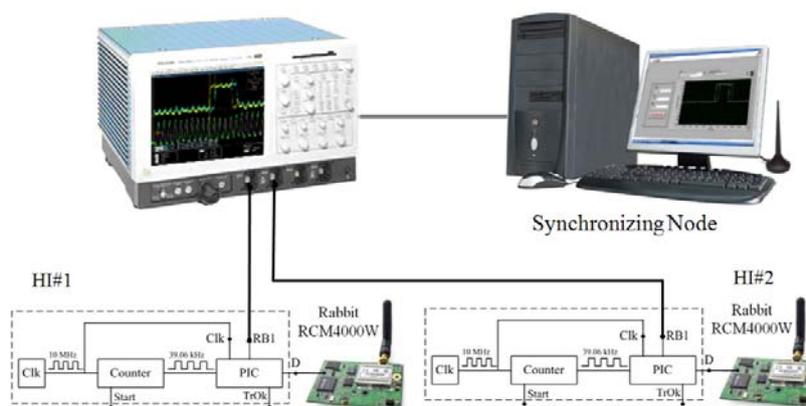


Figure 6. Experimental set up to evaluate the delay between the trigger signals generated by two HIs.

Beginning, the two HIs are synchronized, and, successively, disconnected from the external Starter block, moved to the measurement place, and made available for the Operative Phase.

Fig.5a) shows the snapshot of the two signals furnished by the Clk blocks. They are characterized by mean frequency equal to 10,87 MHz, and standard deviation negligible owing to the adequate thermostatic arrangements. Fig. 5b) shows the snapshot of the start signals received by the Counter blocks. They are characterized by mean delay equal to zero, and standard deviation depending on the voltage supply and temperature. In this case it is equal to 14 ns, according to [10]. Fig.5c) shows the snapshot of the output signals from the Counter blocks. In the test they are driven by common input signal equal to 1 MHz. The delay introduced by the Counter blocks is characterized by mean value equal to zero, and standard deviation equal to 0,53 ns according to the maximum variation range denoted in [11].

In order to detect and measure the time delay Δt between the trigger signals furnished at the pin RB1 of the HI#1 and HI#2, each one is connected to the input channel of the Digital Storage Oscilloscope (DSO), as shown in Fig.6. The Master PC is connected by GPIB interface bus to the DSO, and sends the trigger condition to the two HIs by WiFi connection. The trigger signal fed from the HI#1 is sent to the Ch#1 of the DSO, that of the HI#2 is sent to the Ch#2. The time delay between these two trigger signals furnishes the evaluation of the delay caused by the hardware and the software of the two HIs.

It is evaluated by means of the number of samples occurring between the cross of the established threshold by the two input signals. Denoted by i and j the indexes corresponding to the samples overcoming the threshold, Δt the time between two samples, is $\Delta t = |(i-j)*dt|$.

Fig.7 shows the trend of the Probability Density Function (PDF) of the time delay introduced by the Rabbit RCM4400W (Fig.7a) and the proposed HI in the case $f_{c1}=f_{c2}$ (Fig.7b).

The experimental results are obtained by setting: $n_{itp}=351562$, $n_m=4000$, $v_m=39062$ and performing the synchronization phase only one time. In the case of Rabbit (Fig.7a), the mean value of Δt is equal to 748,77 ns, and the standard deviation is 73,07 μs . In the case of the proposed HI (Fig.7b), the mean value of Δt is equal to 92,00 ns, and the standard deviation is equal to 0,35 ns.

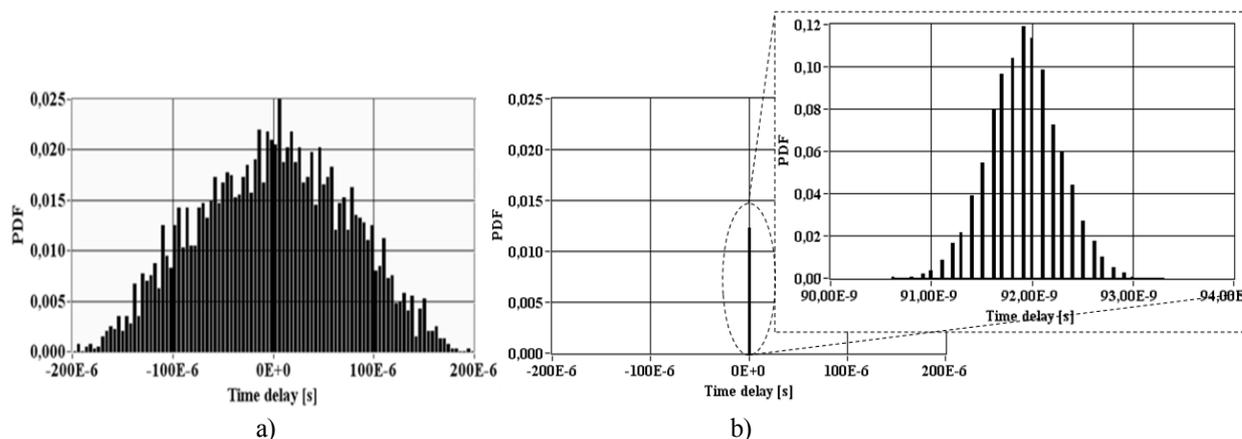


Figure 7. PDF of the delay introduced by a) the Rabbit RCM4400W, and b) the proposed HI.

IV. Conclusions

A solution based on embedded HI is proposed in order to reduce the random causes of the time delay in the detection of the trigger condition to start the command execution for the triggering of the MI. The proposed architecture of the HI includes the PLD as wireless interface, and the board equipped by PIC, Counter block, and Clk block. The hardware architecture and the logical operations performed are discussed. Experimental tests have been performed in the case two HIs have the same trigger condition and same clock frequency. The results of experimental tests confirm (i) the correctness of the performed operations by the trigger synchronizing board, and (ii) the usefulness of the HI to trigger the MIs.

References

- [1] R.E. Wilson, P.S. Sterlina “Verification of measured transmission system phase angles”, IEEE Trans. on Pow. Del., vol.11, N.4, Oct. 1996, pp.1743-1747.
- [2] H. Saitoh, K. Miura, O. Ishiok, H. Sato, J. Toyoda, “On-line modal analysis based on synchronized measurement technology”, Proc. PowerCon 2002, vol. 2, 13-17 Oct. 2002, pp. 817 – 822.
- [3] Y. Hirao, T. Kuroda, D. Zhang, Y. Kinouchi, H. Yamaguchi, K. Yoshizaki, “Synchronized measurements of maximum blood flow velocities in carotid, brachial and femoral arteries, and ECG in human posture changes”, Proc. of the 23rd Intern. Conf of the IEEE Eng. in Med. and Biology Soc, vol.1, 25-28 Oct. 2001, pp. 139 – 142.
- [4] M. Gilany, E.S.T. El Din, M.M. Abdel Aziz, D.K. Ibrahim, “An accurate scheme for fault location in combined overhead line with underground power cable”, IEEE Power Eng. Soc. Gen. Meeting, 2005, vol. 3, pp.2521 – 2527.
- [5] H. Saitoh, “GPS synchronized measurement applications in Japan”, Asia Pacific. IEEE/PES Transmission and Distribution Conference and Exhibition 2002, vol. 1, 6-10 Oct. 2002, pp. 494 – 499.
- [6] H. Ukai, K. Nakamura, N. Matsui, “DSP- and GPS-based synchronized measurement system of harmonics in wide-area distribution system”, IEEE Transactions on Industrial Electronics, vol. 50, N. 6, Dec 2003, pp.1159 – 1164.
- [7] S. Zelingher, B. Fardanesh, E. Uzunovic, A.P.S. Meliopoulos, G. Cokkinides, “Harmonic monitoring system via GPS-synchronized measurements - update and new developments”, IEEE Power Eng. Soc. Gen. Meet., June 2006.
- [8] J. Balcells, V. Parisi, D. Gonzalez, “New trends in power quality measuring instruments”, IEEE 2002 28th Annual Conference of the Industr. Electronics Society, IECON 02, vol. 4, 5-8 Nov. 2002, pp. 3344 – 3349.
- [9] J.C. Bellamy, “Digital network synchronization”, IEEE Comm. Magazine, vol. 33, N. 4, April 1995, pp.70 – 83.
- [10] Jinhua Lu, H. Leung, “Synchronization: a fundamental phenomenon in complex dynamical networks”, IEEE International Symposium on Circuits and Systems, 2005, ISCAS 2005, 23-26 May 2005. pp. 300 – 303.
- [11] L. Chen, J. Leneutre, “A secure and scalable time synchronization protocol in IEEE 802.11 ad hoc networks”, International Conference on Parallel Processing, ICPP 2006, 14-18 Aug. 2006, pp 8.
- [12] D.L. Mills, “Internet time synchronization: the Network Time Protocol”, Electrical Eng. Dept., Univ. of Delaware, <http://citeseer.nj.nec.com/mills91internet.html>.
- [13] IEEE std. 1588-2002 “IEEE standard for a precise clock synchronization protocol for network measurement and control systems”, Pub. by The Institute of Electrical and Electronics Engineers, New York (USA), 8 Nov. 2002.
- [14] D. Grimaldi, F. Lamonaca, “Measurement techniques to assess the time synchronization in distributed systems”, Proc. of IMEKO TC4 2008, Firenze, Italy, 22-24 Sept. 2008.
- [15] D.L. Carni, D. Grimaldi, G. Guglielmelli, F. Lamonaca, “Synchronization of measurement instruments co-operating into the W-DMS”, Proc. of IEEE IMTC/07, Warsaw, Poland, 1-3 May 2007.
- [16] D. Grimaldi, F. Lamonaca, “Analysis of the synchronization delay in the path PC-DSO co-operating into the W-DMS”, Proc. of IEEE Workshop “Intelligent Data Acquisition. and Advanced Computing Systems: Technology and Application (IDAACS’2007)”, Dortmund, Germany, 6-8 Sept. 2007.
- [17] D. Grimaldi, F. Lamonaca, G. Gentile, “Experimental analysis of the delay introduced by Linux OS in the communication PC-measurement instrument”, Proc. of IEEE Workshop “International Conference on Software, Telecommunications and Computer Networks (SoftCOM’2007)”, Split-Dubrovnik, Croatia, 27-29 Sept. 2007.
- [18] D. Grimaldi, F. Lamonaca, “Delay of the software commands in the path PC-measurement instruments”, Proc. of IEEE IMTC/08, Vancouver Island, Canada, 12-15 May 2008.
- [19] A.S. Tanenbaum, “Modern Operating Systems”, second edition, Prentice Hall, 2001.
- [20] D. Grimaldi, F. Lamonaca, “Reduction of Polling Cycle to Check Trigger Condition for Instrument Synchronization”, Proc. of IEEE I2MTC 2009, Intern. Instrum. and Measur. Techn. Conf., Singapore, May 2009.
- [21] D. Grimaldi, F. Lamonaca, “Reduction of the Random Variation of Time Delay to Synchronize Measurement Instruments”, Proc. of IEEE I2MTC 2010, Intern. Instrum. and Measur. Techn. Conf., Austin, Texas, May 2010.
- [22] Fairchild Semiconductor “MM74HC00 Quad 2-Input NAND Gate”, September 1983, Revised January 2005.
- [23] Fairchild Semiconductor “DM74LS191 Synchronous 4-Bit Up/Down Counter with Mode Control”, August 1986, Revised February 1999.