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Architecture of the Multi-Tap-Delay-Line Time-Interval Measurement Module Implemented in FPGA Device

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Abstract- This paper describes architecture of the Multi-Tap-Delay-Line (MTDL) time-interval measurement module of high resolution implemented in single FPGA device. A new architecture of the measurement module enables to collect of sixteen time-stamps during single measuring cycle. It means that measured time-interval can be precisely interpolated from collection of the sixteen time-stamps after each measuring cycle. Such architecture of the measurement module leads straight to increase of resolution, to limit total duration time of the measurements and to decrease of duty cycle of the measurement instrument.

Keywords*:* time-interval measurement, tapped delay lines

I. INTRODUCTION

High resolution TIMS are widely applied in many system. For example they can be applied in quantum cryptography experiments, in characterization of the clock phase fluctuations, in life-time measurements of the excited atomic states, in ultrasonic flow-meters or monitoring systems of time-of-flight mass spectrometers [2, 3]. Of course, it should be noticed, that system implemented in FPGA devices is not energy-efficient. Limiting the total number of time-interval measurements and increasing, in the same time the system resolution, effective duty cycle and the total power consumption could be decreased [1].

The measurement system presented in this paper enables not only for increasing the system resolution but also for significantly decreasing uncertainty of the single time-interval measurement.

A. Architecture of the TIMS

TIMS as a virtual instrument consists of hardware unit, flexible software and a computer.

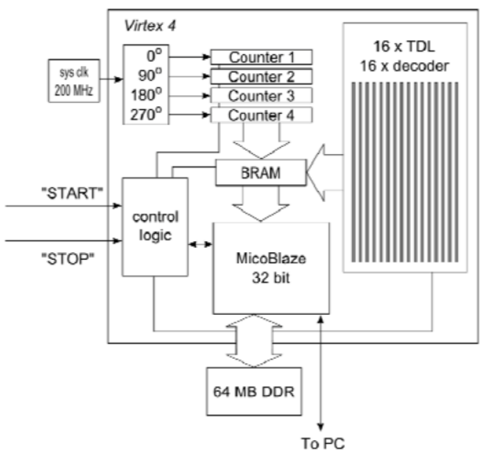

Figure 1. The block diagram of TIMS

The block diagram of the new TIMS architecture is shown in Fig.1. The system is implemented in Xilinx Virtex 4 FPGA structure and uses chip-outside-located 64 MB DDR of RAM for data collection.

The main unit of system is 32 bit soft processor – Microblaze. Other parts of the system are implemented as microprocessor peripherals. ISE and EDK programs have been used to implementation of the virtual microprocessor and its peripherals.

The implemented system consists of the group of sixteen two-hundred-element multi-tap delay lines with coupled registers, sixteen code converters, four clock cycles counters, blocks of inside memory (BRAM), interface and control unit . Carry chain of CLB's (Configurable Logical Block) is used to tapped delay lines and registers implementation [Fig. 2]. It is possible to change of the elements placement and connection to change of the line delay. Using this method, the characteristics of delay-line can be shaped.

First the tap's must be sorted, because time of clock (clk) net is not monotonic [Fig.3]. The values readed from the FPGA editor, not contains information about the fluctuations of the delays in FPGA structure. From this reason, system can read all TDL registers in raw mode, bypassing code converter and storing it in BRAM. It is not possible to read all the sixteen TDL at the same time (it is not enough BRAM for this operation in chip, which was used). There is 16-to-1 multiplexer to switch between TDL's registers. The signal multiplexer can be switch to second divided system generator. The raw waveform of recorded system clock is triggered by second divided clock and it is stored in BRAM. Data from BRAM is sends to computer. Calibration program on PC computer is seeking anomalies in waveform [Tab.1]. The anomalies are single or double (and so on) zeros or ones usually on beginning and ending of the sequences of the same value in the waveform. Program uses a special correlation procedure to computing the right place of the particular tap in the FPGA structure. The next procedure generates vhdl code of sorted TDL. This procedure is repeating for every TDL. After compilation the corrected TDL are implemented in FPGA.

Table 1. The example section of waveform before sorting a) and after sorting b) The tap 97, 98 and 100 is accordingly shifted into place and now is tap number respectively 100, 97, 98

a)

No.	Numer of tap											
	93	94	95	96	**97**	**98**	**99**	**100**	101	102	103	104
0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	1	0	0	0	1	1	1	1
2	0	0	0	0	1	0	0	0	1	1	1	1
3	0	0	0	0	1	0	1	0	1	1	1	1
4	0	0	0	0	1	0	1	0	1	1	1	1
5	0	0	0	0	1	0	1	0	1	1	1	1
6	0	0	0	0	1	0	1	0	1	1	1	1
7	0	0	0	0	1	0	1	1	1	1	1	1
8	0	0	0	0	1	0	1	1	1	1	1	1
9	0	0	0	0	1	0	1	1	1	1	1	1
10	0	0	0	0	1	1	1	1	1	1	1	1

b)

No.	Numer of tap											
	93	94	95	96	**98**	**100**	**99**	**97**	101	102	103	104
0	0	0	0	0	0	0	0	0	1	1	1	1
1	0	0	0	0	0	0	0	1	1	1	1	1
2	0	0	0	0	0	0	0	1	1	1	1	1
3	0	0	0	0	0	0	1	1	1	1	1	1
4	0	0	0	0	0	0	1	1	1	1	1	1
5	0	0	0	0	0	0	1	1	1	1	1	1
6	0	0	0	0	0	0	1	1	1	1	1	1
7	0	0	0	0	0	1	1	1	1	1	1	1
8	0	0	0	0	0	1	1	1	1	1	1	1
9	0	0	0	0	0	1	1	1	1	1	1	1
10	0	0	0	0	1	1	1	1	1	1	1	1

Quadruple of the clock cycles counter ensures sufficient set-up time during incrementation and the possibility of asynchronous read-out of data from one of the counter. Counter is choosen by the information of the number of tap form TDL. These data are used for computing all sixteen time-stamps from all TDL.

Each measured time stamp consists of main part, which is taken from one of the clock cycles counters and residual part, which is taken from one of the delay-line register through the data converter. Theoretical precision of TDL is 25 ps per tap.

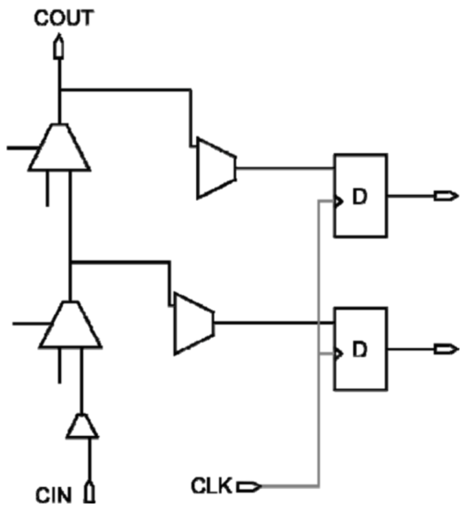

Figure 2. Two taps of TDL made of carry chain with registers before tuning

There is a great difficulty to implement of the code converter, which works in thermometric code. The main reason to use code converter is data acquisition. Single time-interval measurement can generate more than four hundred bytes of data. This value is similar to capacity one of the BRAM inside chip. The code converter reduces data for storage.

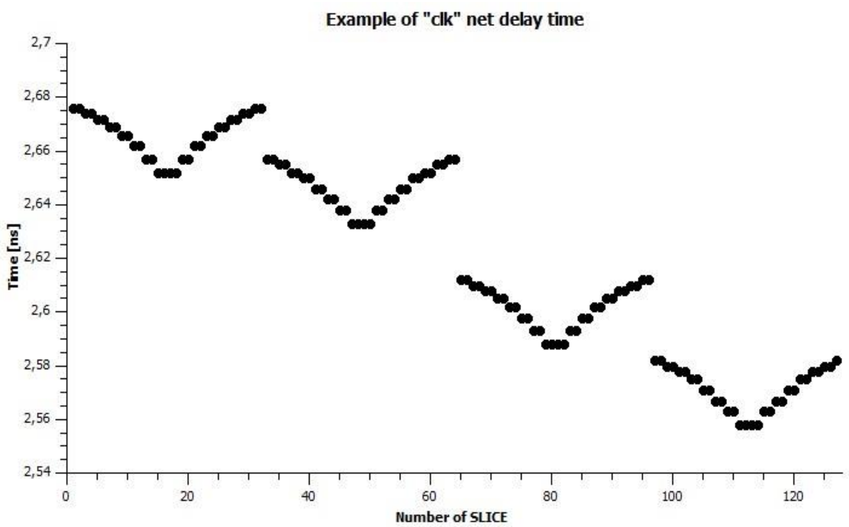

Figure 3. Example of "clk" net delay in FPGA device for 128 slices – read from the FPGA editor

Requirements for a code converter are compromise of speed and occupancy of small space of FPGA chip. Many converters 16-to-4 bits in parallel mode were implemented. Finally, chosen code-converter requires only two BRAM for one TDL comparing to more than six without code converter.

The DDR 64 MB RAM is used for data acquisition, when there is more than five hundred time stamps, if intensity of measurement time-interval is too fast to send data to the PC.

B. Principle of Time-interval measurement

The main task of the measuring system is registration and collection of time-stamps. The time-stamp is a combination of integer number of standard clock cycles and the TDL-register two-bits index that have 1 to 0 transition registered. The measured time-interval Δt_m is calculated by the difference of two time-stamps.

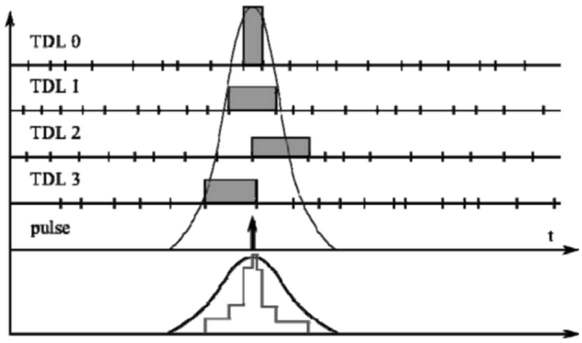

Figure 4. The idea of multiple TDLs measurement

Precision of TIMS in practice depends on the precision of interpolators, that measure residual time intervals and accumulated jitter of standard clock [1]. If a multi-tap delay lines are used in the design of interpolator then value of the single segment delay τ and its standard deviation determines precision of time-interval (Δt_m) measurement. If interpolator consists of n delay lines of relatively high resolution, then during the single measuring cycle it is possible to obtain n different results of time-interval Δt_m. Such solution leads straight to increasing of precision of time-interval measurement and reduces number of measurement cycles. This method significantly reduces the power consumption for battery-powered systems, because the number of measuring cycles is generally significantly decreased. Knowing delay lines characteristics such DNL (Differential Nonlinearity) and INL (Integral Nonlinearity) and using quantization-and-nonlinearity-minimization (QNM) method, it is possible to obtain two-sample-difference histogram, increases system resolution and decreases uncertainty of time-interval measurement [4].

In the presented system with 16 TDLs which consists of 200 taps (for each TDL), expected accuracy should be better than 15 ps for single-shot measurement.

C. Experimental Results

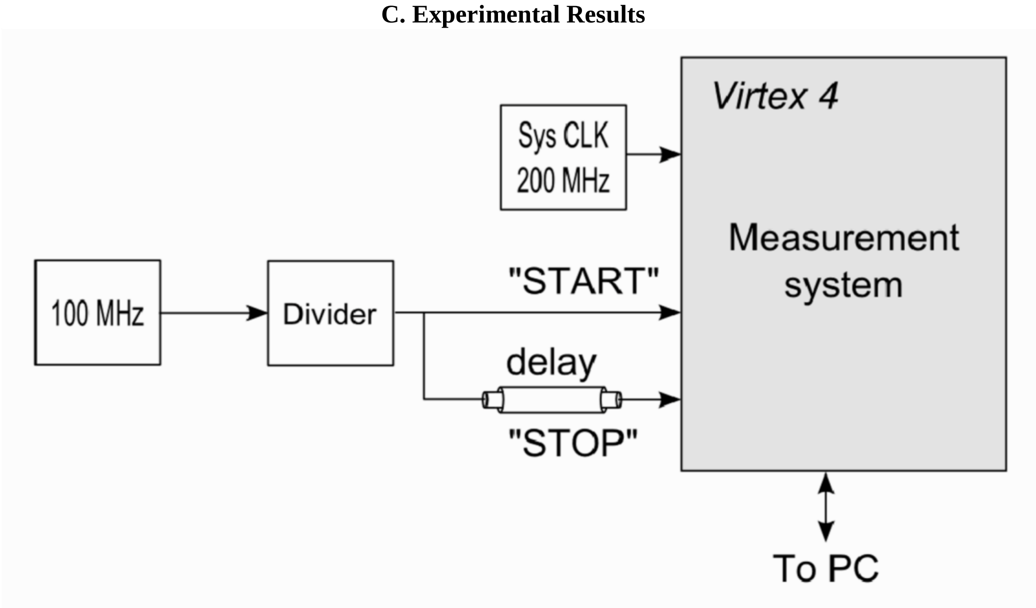

Figure 5. The experimental measurement system

A series of time-interval measurements was performed to verify the measurement system. For the test, a single section of coaxial cable was used as a delay element as it is shown in Fig.5.

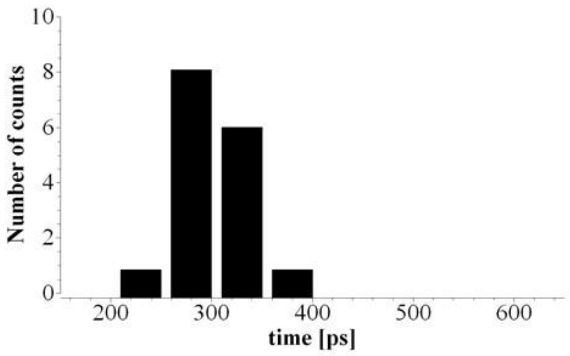

Figure 6. Time-stamp histogram obtained for start pulse

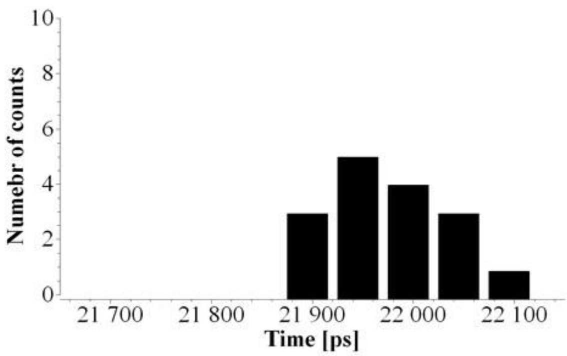

Figure 7. Time-stamp histogram obtained for stop pulse

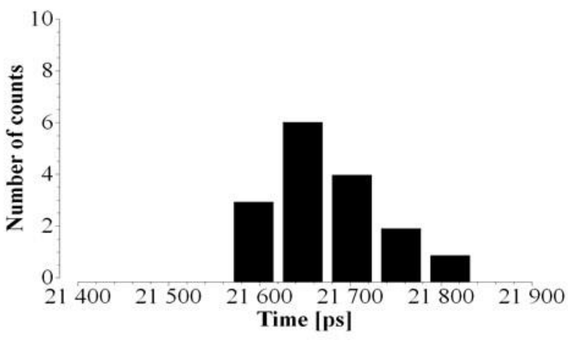

Figure 8. Time-interval histogram

Figures 6 and 7 shows time-stamp histograms obtained for start and stop pulses. One should notice that the surface of both diagrams is equal to the number of TDLs. Figure 8 shows time-interval histogram obtained as a difference between start and stop measurements. It is worth of being noticed that the uncertainty of time-interval does not increased significantly in comparison to source time-stamp uncertainties.

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