

## Low-Frequency Noise Measurement in Silicon Power MOSFETs as a Tool to Experimentally Investigate the Defectiveness of the Gate Oxide

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**Abstract** - In this work we analyse the applicability of low-frequency (LF) noise measurement in order to study the defectiveness in the gate oxide of power MOSFETs. To this purpose we implement a low-noise experimental set-up, which is able to measure the drain current flicker ("1/f") noise of the device under test (DUT). First, we show how these measurements can be used to empirically detect the physical model and related compact expressions, which best describe the source of fluctuations in this type of devices. Then, accordingly to the selected physical model, the defect density in the gate oxide is extracted. In order to validate the proposed methodology, experimental data are reported and discussed in the case of trench power MOSFETs. The measured noise spectra confirm the suitability of the laboratory set-up for this type of analysis and, by means of an empirical fitting of the data, the defect density is estimated, in accordance with the typical values expected for the technology considered.

**Keywords:** 1/f noise; flicker noise; power MOSFET; drain current noise; low-frequency noise measurements; gate oxide; defectiveness.

### I. Introduction

Low-frequency (LF) noise measurement represents a powerful tool to empirically investigate the defectiveness in semiconductor devices [1-3]. Its usefulness was largely proved in the field of CMOS devices with the aim of studying the impact of the technological parameters and adopted materials on the overall gate stack quality [4-6]. In particular, the drain current flicker (1/f) noise was shown to be related to the defects located at both the silicon-oxide interface and within the gate oxide [4]. These defects are responsible for dispersion effects and significantly impact on the reliability of the devices. Therefore the estimation of this phenomenon represents an useful assessment for MOSFET devices. Flicker noise was also studied in [7, 8] regarding power MOSFETs, aiming at investigating the effect of ionizing radiation on drain current noise.

In our previous works [9-11] we have developed an analytical model for the gate current flicker noise which was validated on MOSFET devices. In [12, 13] we have demonstrated the suitability of LF noise to analyse the impact of high-k materials as gate dielectric in CMOS technology. To this purpose drain current flicker noise has been measured and compared when considering different gate stack architectures. In this work we implement an experimental set-up for LF noise measurement in power MOSFETs. This analysis has a twofold purpose: i) to select, among those provided by the literature, the most suitable physical model which describes the source of fluctuations for the technology considered; ii) on the basis of the physical model selected and validated through the empirical data, to estimate experimentally the defect density in the gate oxide of the device under test (DUT). Although drain current flicker noise was also investigated in [7, 8] for power MOSFETs, there was no attempt to model the current fluctuations. On the other hand, conventional noise models have been only applied to CMOS technology [4, 12, 13], while their validation on power MOSFETs is still missing.

The paper is organized as described in the following: in section II the low-noise experimental set-up is described; in section III we report an example of application involving silicon trench power MOSFETs; finally, in section IV the main conclusions of this work are summarized.

### II. The low-noise laboratory set-up

The implemented experimental set-up, which derives from a refinement of that exploited in [14], is shown in Fig. 1. The use of a two-stage amplifier allows to separately evaluate the DC and LF components of the open-circuit drain voltage  $v_d(t)$  of the DUT, without saturating the Op-Amps and with adequate gain in the LF path.

The considered application requires to investigate the voltage fluctuations in the typical frequency range [0.1 Hz – 500 Hz] in which flicker noise dominates, although the range can be easily extended in order to study other sources of fluctuation.

In order to properly bias the DUT, the laboratory set-up must include a bias system which is able to provide accurate variable DC voltage levels at the two ports without introducing significant LF noise contributions in the bandwidth of interest. To this aim, the gate bias stage (as reported in Fig. 2) is based on a large value polypropylene film capacitor which is charged to desired value by means of an external reference source. The presence of an Op-Amp based buffer prevents the discharge of the capacitor. By adopting this biasing solution, we are able to merge the flexibility of an external reference source and the low-noise properties of an Op-Amp based buffer [14]. On the other hand, the biasing of the drain terminal requires a different solution since a large current must be supplied in power MOSFETs (in the order of hundreds of mA), which cannot typically be provided by a low noise Op-Amp. For this reason, as reported in Fig. 2, the drain DC current is generated through the series of a lead-acid battery and a resistor. The implication of the bias resistor on the noise measurements will be discussed in the next section. Moreover, since the series resistance of the power MOSFETs is in the order of (or lower than) 1  $\Omega$ , a four-wire connection is implemented.

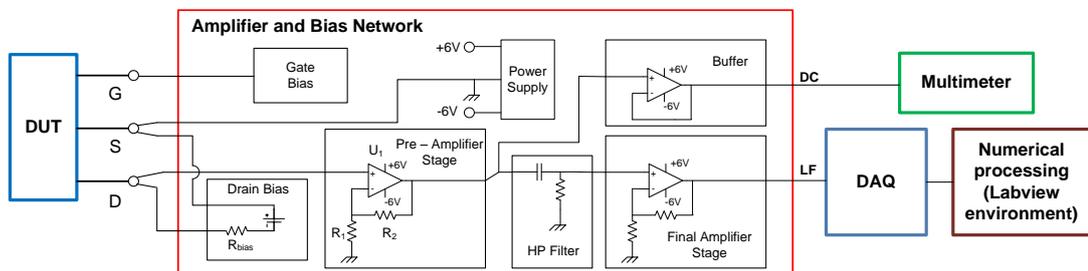


Figure 1. Schematic of the LF noise measurement system designed and implemented for power MOSFETs.

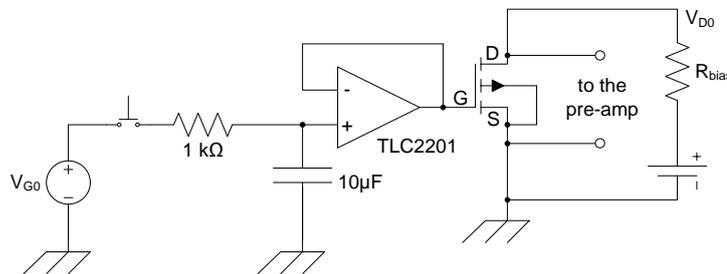


Figure 2. Schematic of the adopted low-noise bias system architecture.

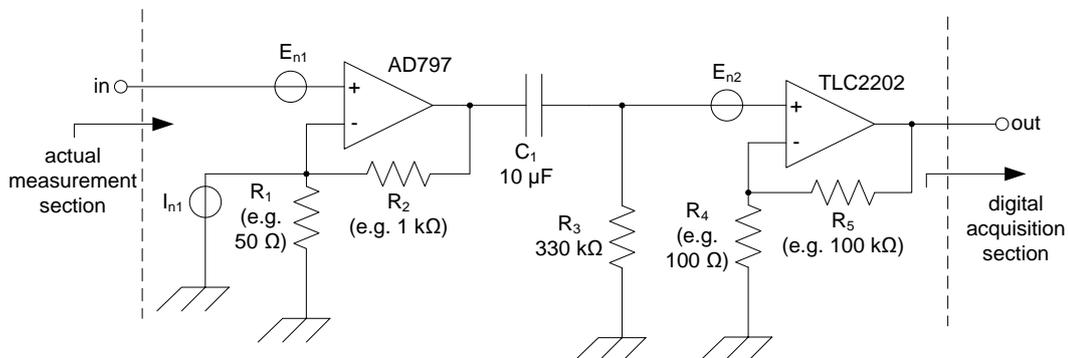


Figure 3. Schematic of the two-stage amplifier, including the most relevant equivalent noise sources of the Op-Amps.

The details of the drain amplifier stage are reported in Fig. 3. The pre-amplifier is based on an AD797 Op-Amp in a non-inverting configuration. The HP filter has a cut-off frequency of 0.05 Hz and the second stage

voltage amplifier is based on a TLC2202 Op-Amp. Both amplifiers have a variable gain. The maximum achievable gain depends on: i) saturation of AD797 Op-Amp; ii) bandwidth requirements; iii) adequate open-loop gain. In the case of noise measurement considered in this work, the DC value of the drain voltage is relatively low (a few hundreds mV or lower), since the device must be biased in triode region, as discussed in the next section. Supposing a supply voltage of  $\pm 6$  V, a bandwidth requirement of 1 kHz and a DC value of the input drain voltage of 100 mV, we find out a maximum voltage gain of about 50000. The values of the resistances reported in Fig. 3, leading to a nominal voltage gain of 21021, are the ones adopted in order to characterize the DUT described in section III.

The equivalent input noise (one-sided) power spectral density (PSD) of the circuit of Fig. 3 can be approximated as:

$$G_{fn}(f) \approx E_{n1}^2(f) + \frac{E_{n2}^2(f) + I_{n1}^2(f)R_2^2 + 4kT \frac{R_2^2}{R_1}}{\left(1 + \frac{R_2}{R_1}\right)^2} \quad (1)$$

where  $E_{n1}$  and  $E_{n2}$  are the input equivalent noise voltage sources of the AD797 and TLC2202 Op-Amps, respectively,  $I_{n1}$  is the input equivalent noise current source of the AD797 Op-Amp,  $k$  is the Boltzmann constant and  $T$  is the absolute temperature.  $E_{n1}$  and  $I_{n1}$  are assumed to be uncorrelated in eq. (1).

The signal amplified is acquired by means of a NI USB-4431 module. The sampling rate in our case is 1 kSa/s, since we are interested in the low-frequency noise, but can be easily extended to 102.4 kSa/s in order to analyse the higher frequencies of the spectrum. The digital processing is performed within the LabView environment and the PSD  $G'_{vd}$ , evaluated at the actual measurement section, is estimated by considering averaging techniques.

The noise floor of the set-up, reported in Fig. 4, is evaluated by short-circuiting to ground the input of the pre-amplifier and by referring it to the actual measurement section. We obtain a white noise of  $1.75 \times 10^{-18}$  V<sup>2</sup>/Hz and flicker component which assumes a value of  $2.1 \times 10^{-17}$  V<sup>2</sup>/Hz at  $f = 1$  Hz. By considering nominal values of  $E_n$  and  $I_n$  for AD797 and TLC2202, the PSD shown in Fig. 4 is in agreement with the value predicted by (eq\_EIN).

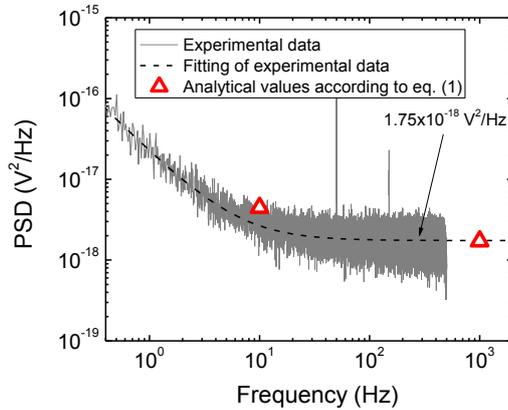


Figure 4. Set-up noise floor referred to the actual measurement section (input of the pre-amplifier, see Fig. 3).

### III. Experimental examples

When analysing, from a physics-based standpoint, the sources of fluctuation effects in a MOS device there are two main models widely accepted by the scientific community: McWorther number [15] and Hooge's mobility [16] fluctuation models. In the case of number fluctuation model the drain current  $1/f$  noise is generated by the fluctuation of charge carriers which are trapped and detrapped by oxide "traps" (i.e., defects associated with spurious energy levels). The PSD of the drain short-circuit current noise, in triode region, can be thus expressed as [15]:

$$G_{id}(f) = \frac{I_D^2}{WL} \frac{qkTN_t}{C_{ox}^2 f (V_{GS} - V_T)^2 \gamma} \quad (2)$$

where  $I_D$  is the DC drain current,  $W$  and  $L$  are the channel width and length,  $q$  is the elementary charge,  $C_{ox}$  is the gate capacitance in  $F/cm^2$ ,  $V_{GS}$  is the DC gate voltage,  $V_T$  is the threshold voltage,  $\gamma$  is an attenuation coefficient and  $N_t$  is the volumetric trap density in  $cm^{-3} \cdot eV^{-1}$ :

According to eq. (2), we are interested in the estimation of the PSD  $G_{id}$  of the drain current noise, which can be obtained from  $G'_{vd}$  (directly measured by our set-up) by means of

$$G'_{vd}(f) = G_{id}(f) \cdot (R_{ch} // R_{bias})^2 \quad (3)$$

where  $R_{ch}$  is the channel resistance. The bias resistance  $R_{bias}$  is chosen at least two orders of magnitude higher than  $R_{ch}$  in order to minimize the measurement uncertainty. In order to better understand the dependence of the expected noise level on the bias point and on the geometrical parameters, let us combine eq. (2) and (3) as

$$G'_{vd}(f) = G_{id}(f) \frac{R_{ch}^2 R_{bias}^2}{(R_{ch} + R_{bias})^2} = G_{id}(f) \frac{V_{DS}^2}{I_D^2} A^2 \propto \frac{V_{DS}^2}{WL} \frac{A^2}{(V_{GS} - V_T)^2} \frac{1}{f} \quad (4)$$

where  $A$  is defined as  $A = R_{bias} / (R_{ch} + R_{bias})$  and is very close to 1. Power MOSFETs are typically very large devices, hence, according to eq. (4), the noise level to be measured is expected to be much lower than the noise level in CMOS technology. Moreover, the noise level decreases as long as the gate voltage is increased and the drain voltage is reduced. However, eq. (2) is only valid in triode region and hence there is an upper limit for the drain voltage value to be applied.

In order to evaluate the performance of the experimental set-up and to show how the experimental data can be used for the detection of the best physical model, we will consider the power MOSFET technology reported in the following. The DUT is a p-channel silicon power MOSFET with a  $SiO_2$  gate oxide. In particular, we consider a 30-V trench power MOSFET developed by ST Microelectronics with a total width of 69 cm and a gate length of 0.5  $\mu m$ . The measured spectra, reported as an example in Fig. 5 for different gate voltages in triode region, are well above the noise floor of the set-up.

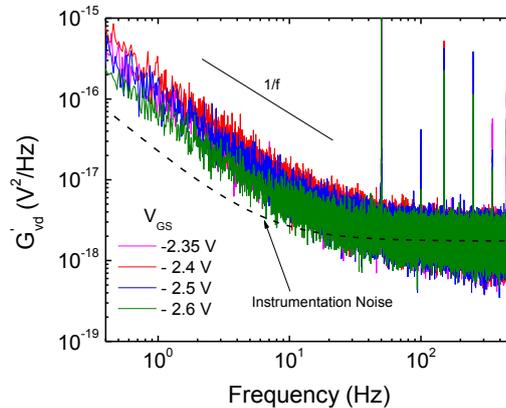


Figure 5. Voltage power spectrum, at different gate voltage bias levels, measured in a Silicon Power MOSFET.

The data shown here are then corrected for the noise floor, transformed in current spectra and normalized by the gate area and drain current, according to eq. (2) and eq. (3). These data are fundamental in order to select the physical model and then to estimate the trap density.

A method to evaluate the suitability of the number fluctuation model reported in eq. (2) consists in checking whether  $G_{id}/I_D^2 \propto 1/(V_{GS} - V_T)^2$ . The normalized current spectrum, evaluated at a fixed frequency of 1 Hz, is reported in Fig. 6 as a function of the gate voltage overdrive  $|V_{GS} - V_T|$ . Similar values are found in all the three samples considered in this measurement campaign. Thus, we can establish that the 1/f noise sources are well modelled by the number fluctuation model since the normalized drain current PSD is proportional to  $(V_{GS} - V_T)^{-2}$ .

Once the model has been validated through experimental data, from eq. (2) we are able to estimate the trap

density in the gate oxide as

$$N_t = \frac{G_{id} C_{ox}^2 W L f (V_{GS} - V_T)^2 \gamma}{q k T I_D^2} \quad (5)$$

The estimated value (reported in Fig. 7) is almost independent of the gate voltage and is about  $10^{16} \text{ cm}^{-3} \text{ eV}^{-1}$ . Typical values of the trap density in  $\text{SiO}_2$  dielectric are available in literature for the CMOS technology [17] and can be compared with our findings in power MOSFETs. Keeping in mind that we are comparing different technologies, reasonable values are obtained in this work.

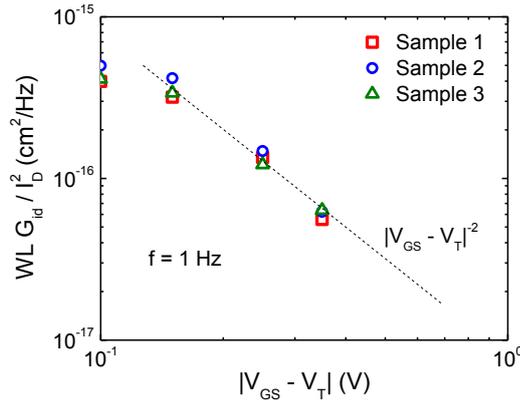


Figure 6. Normalized current power spectrum evaluated at 1 Hz vs. gate voltage overdrive.

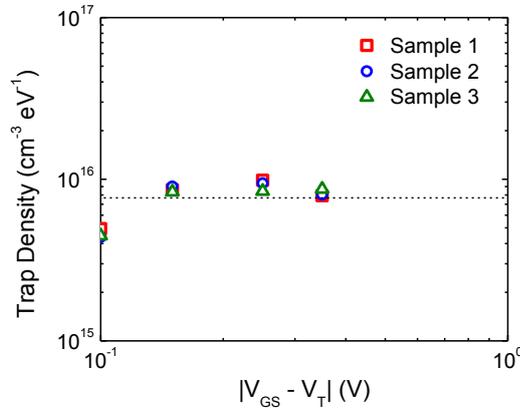


Figure 7. Volumetric trap density as a function of gate voltage overdrive.

#### IV. Conclusions

In this work, we implemented a low-noise laboratory set-up and related numerical processing techniques that allow to perform accurate LF noise measurements in power MOSFETs. The experimental results confirmed the suitability of this measurement technique to analyse the gate oxide quality in silicon trench power MOSFETs. Moreover, from a general standpoint, this kind of empirical investigation allows to select the most suitable physical model for the compact description of  $1/f$ -like fluctuations of the drain current. In particular in this paper, by measuring the LF noise spectra as a function of the gate voltage bias level, we proved that the so-called McWorther number fluctuation model is appropriate for the device technology considered. Thus, this model was adopted, in association with the experimental data, in order to estimate the trap density in the gate oxide. To the authors knowledge, this is the first time that such a technique is applied to trench power MOSFETs.

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