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A Novel Capacitance-to-Digital Converter for Capacitive Sensors with AC Excitation

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Abstract-This paper proposes a novel, simple and high accuracy Capacitance-to-Digital Converter (CDC). Capacitive sensors have numerous industrial applications such as humidity sensing, human touch sensing, flow measurement, ice detection, etc. In most of these applications a sinusoidal excitation is employed or preferred to achieve high sensitivity and accuracy. In order to get a final digital output from a conventional bridge based circuit with a capacitive sensor, an Analog-to-Digital Converter ADC is required. CDCs wherein capacitive sensor is an integral part of a sigma-delta ADC are available but they do not employ a sinusoidal excitation and hence may not give the best output for some of the above mentioned applications. This paper presents a new dual-slope CDC that is designed to accept output from a capacitive sensor, which is excited electrically by a sinusoidal source, and provides a direct digital output proportional to change in capacitance. Such a CDC, having a distinct combination of sinusoidal excitation and dual-slope principle, is best suited for various applications as it provides high accuracy, sensitivity, immunity-to-noise and interference, etc. A prototype CDC has been developed and tested in the laboratory. Experimental results showed the practicality of the proposed scheme.

I. Introduction

Capacitive sensors have wide range of industrial and scientific applications [1]. They are simple to construct and less expensive at the same time offer high sensitivity, accuracy, low power consumption, etc. [1-3]. Traditional bridge based circuits can obtain a modulated output voltage from capacitive sensors [1]. In most of the practical applications, a suitable demodulator followed by an Analog-to-Digital Converter (ADC) that digitizes the signal is required to process or store the sensor output data. For several sensing applications such as ice detection [3], humidity sensing [4], human touch sensing, etc. a sinusoidal excitation at specific frequency is preferred to achieve optimal performance. Direct Capacitance-to-Digital Converters (CDC) based on sigma-delta, dual-slope (for differential capacitive sensors) or micro-controller techniques [5-7] have been reported but they do not use sinusoidal excitation. This paper proposes a novel CDC for capacitive sensors. In this CDC, the sensor is excited from a sinusoidal source but still the CDC provides a direct digital output without the help of a dedicated ADC. This CDC is applicable for all types of capacitive sensors and specifically very useful for capacitive sensors which prefer sinusoidal excitation. A prototype of the new CDC has been built and its practicality has been tested using a standard capacitance box. The details are presented below.

A. New Capacitance-to-Digital converter for Capacitive Sensors with Sinusoidal Excitation

A block diagram representation of the proposed CDC is shown in Figure 1. The CDC consists of a capacitive sensor C_1, known capacitance C_S, SPDT switches S_1 and S_2, Control and Logic Unit (CLU) and an integrator formed by opamp OA, capacitor C_F, and resistor R. The CLU monitors outputs of the comparators OC, OC_1 and

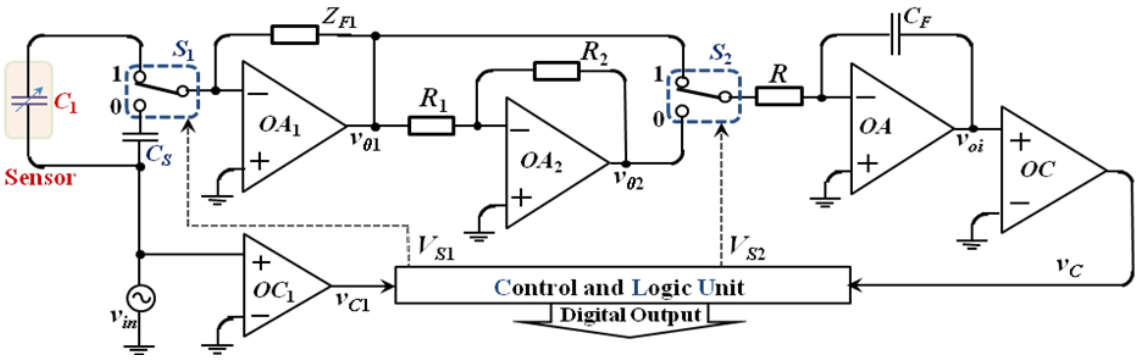

Figure 1. Schematic of the proposed Capacitance-to-Digital Converter

in turn controls switches S_1 and S_2 through the control signals V_{S1} and V_{S2}. The CLU is synchronised with the frequency ($f = 1/T_C$) of excitation source $v_{in} = v_m sin2\pi ft$ through the comparator output OC_1.

The CDC has an auto-zero phase and a conversion phase. The conversion phase consists of a preset charging period of T_1 and a discharging period of T_2 as shown in Figure 2. During T_1, the CLU sets S_1 in position-1 connecting the sensor capacitance C_1 in the circuit. Thus, a current $C_1\omega v_m Cos\omega t$ flows through C_1 from the sinusoidal source $v_{in} = v_m Sin\omega t.$, where $\omega = 2\pi f$. This current passes through Z_{F1} causing a voltage drop across it and the corresponding output voltage v_{01} of opamp OA_1 can be expressed as $v_{01} = -C_1 Z_1 \omega v_m Cos\omega t$ (refer Figure 2). v_{01} is given to position-1 of switch S_2 as well as to an inverting amplifier formed using R_1, R_2 and opamp OA_2, whose output v_{02} is given to position-0 of switch S_2. $R_1 = R_2$, hence $v_{02} = -v_{01} = C_1 Z_1 \omega v_m Cos\omega t$. Here Z_{F1} is realized using a capacitor C_{F1}, thus OA_1 is a charge amplifier. In this condition, the voltage signals v_{01} and v_{02} can be expressed as in (1).

$$v_{01} = -\frac{C_1}{C_{F1}} v_m Sin\omega t \quad v_{02} = \frac{C_1}{C_{F1}} v_m Sin\omega t \tag{1}$$

Whenever the output signal v_{C1} of comparator OC_1 is positive, switch S_2 will be at position-0. S_2 will be in position-1, otherwise. When it is in position-0, a current of $(C_1/RC_{F1})v_m Sin\omega t$ will flow through R from time $t = 0$ to $t = T_C/2$ and charges C_F. During this process, i.e., $t = 0$ to $T_C/2$, the integrator voltage v_{oi} will change by v_{K1} as given in (2).

$$v_{K1} = -C_1(2v_m / R\omega C_{F1} C_F) \tag{2}$$

If v_{C1} is low, S_2 will give the voltage signal v_{01} to the integrator input, hence a current $(C_1/RC_{F1})v_m Sin\omega t$ will flow through R charging C_F in the same direction for rest of the cycle $T_C/2$ to T_C. Thus, there will be an additional change of v_{K1} in v_{oi} (during $T_C/2$ to T_C). The same occurs for the next input cycle and this process will continue until time $t = T_1$. At the end of T_1, voltage v_{oi} (N_1) of the integrator is given by (3).

$$v_{oi}(N_1) = 2N_1 v_{K1} \tag{3}$$

As soon as time T_1 elapses ($=N_1 T_C$, i.e. after N_1 cycles of v_{in}) the CLU changes S_1 to position-0 using the control signal V_{S1}. In this condition, current through a known fixed capacitor C_S will flow through Z_{F1} as indicated in Figure 1. The CLU also resets the counter back to zero implying that the integration period is complete. As soon as S_1 is moved to position-0, the de-integration period starts. During this period, the CLU sets S_2 to position-1 whenever v_{C1} is positive and sets to position-0, otherwise. In this condition, during $t = T_1$ to $T_1+T_C/2$, integrator voltage will change towards zero by an amount v_{K2} given by (4).

$$v_{K2} = -C_S(2v_m / R\omega C_{F1} C_F). \tag{4}$$

During $t = T_1+T_C/2$ to T_1+T_C, switches are regulated in a similar manner such that the integrator voltage will further change by v_{K2}. This process will continue until v_{oi} reaches zero. When v_{oi} reaches zero, v_c will change from low to high. This will be detected by the CLU and CLU stops the de-integration period T_2. Change in the integrator voltage during the period T_2 ($=N_2 T_C$, i. e. N_2 cycles of v_{in}) is given by (5).

$$v_{oi}(N_2) = 2N_2 v_{K2} \tag{5}$$

The total charge acquired by C_F during T_1 is equal to the total amount discharged during T_2, thus giving the relation $v_{oi}(N_1) = v_{oi}(N_2)$ implying

$$C_1 N_1(4v_m / R\omega C_{F1} C_F) = C_S N_2(4v_m / R\omega C_{F1} C_F) \tag{6}$$

$$C_1 = (N_2 / N_1) C_S \tag{7}$$

Thus, digital value of sensor capacitance C_1 is obtained in terms of CLU counter output N_2 (counter output during T_2), preset count N_1 and known capacitance C_S.

Like in any typical dual slope converter, the proposed CDC also has an auto-zero phase as illustrated in Figure 2. The Auto-zero phase ensures that integrator voltage v_{oi} is zero before the conversion phase starts (if no auto-zero phase, v_{oi} can be +/- at the beginning of measurement). During the auto-zero phase, switch S_1 is kept in position-0 so that the known capacitor is connected in the circuit and the switch S_2 is controlled in such a way by the CLU to bring output voltage v_{oi} to zero. If v_C is sensed as high then the CLU further looks at v_{C1}. If v_{C1} is also high then CLU sets S_2 to position-0. If v_{C1} is low S_2 will be set to position-1. Suppose that v_C is sensed as low

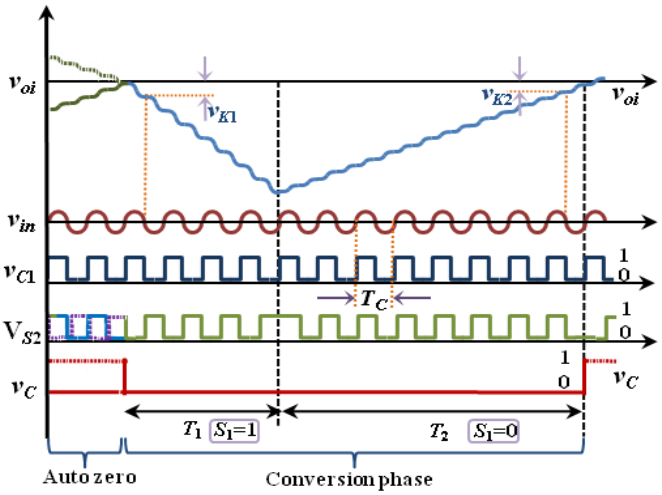

Figure 2. Signals at important points in the CDC.

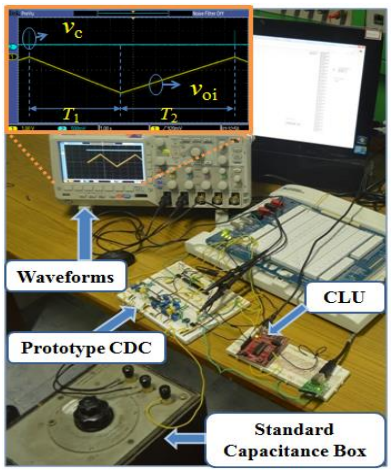

Figure 3. Experimental set-up.

and v_{C1} high, then S_2 will be kept at position-1. S_2 will be changed to position-0 when v_{C1} is low. In this manner, the CLU ensures that $|v_{02}|$ (when v_C high) and $-|v_{02}|$ (when v_C low) is applied as an input to the integrator circuit thus making v_{oi} ramp up or down appropriately, until v_{oi} reaches zero. The end of the auto-zero phase is marked either by a high to low or low to high transition of the comparator output v_C. Once the auto-zero phase is complete the conversion phase will be performed as explained above.

C. Sources of Errors

Various circuit parameters will affect the performance of the CDC. Some of the parameters that introduce errors in the output of the CDC are offset voltages of the opamp *OA* and comparator *OC*, bias currents of the opamps, delays in the switches and comparator, ON resistance of the SPDT switches, etc. In order to keep the errors due to offset voltages and bias current low, ICs with very low offset voltage and less bias current were selected to realize the opamps and comparators. The switches and comparators were selected considering the fact that the delay introduced by them is negligible compared to clock period T_C. Similarly, switches with low ON resistance, which is much less than the impedance offered by the capacitive sensor were employed.

D. Experimental set-up and results

First a SPICE simulation of the CDC has been performed for a ±100pF variation in C_1. The step size chosen for this test was 10 pF. Worst-case error noted from the simulation study was less than 0.004%. In order to verify the practicality of the CDC, a prototype was built and tested. OP07 IC was used for realizing the opamps. S_1 and S_2 were realised using CD4053 IC. LM311 IC's served as the comparators (*OC* and OC_1). R = 300 kΩ, C_F = 2µF and C_{F1} = 1nF were chosen in the prototype developed. CLU was realized using a MSP430G2553 from Texas Instruments. A photograph of the set-up is shown in Figure 3. Oscilloscope indicating important waveforms is shown inset. For the tests, a standard variable capacitance box with an accuracy of ±0.01% manufactured by Neptun, Geretsried, Germany was used as C_1. C_1 was varied from 600 pF to 800 pF (emulating a sensor with offset and cable capacitances) in steps of 10 pF (keeping C_S = 600pF). Results noted from the prototype for every 10pF, with the calculated error, are shown in Figure 4. Worst-case error observed during the test was 0.06%. The results show that the new CDC is capable of measuring change in capacitance accurately.

As mentioned earlier, the new CDC (employs sine wave excitation) is well suited for applications such as humidity sensing, ice detection, fluid flow measurement, etc. The prototype CDC, with capacitive electrodes, was used to detect the presence of an ice layer. Ice exhibits different relative permittivity with respect to frequency of excitation [3]. At low frequencies (about 1 kHz) its value is close to that of relative permittivity of water and at high frequencies (about 100 kHz) it exhibits low value. Water has same relative permittivity (about 80) for all frequencies. In the experiment, water layer was kept (inside a case with low relative permittivity and

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conductivity) on the capacitive electrodes and the CDC was operated first at 1 kHz and then at 100 kHz and its output responses were noted. Then water was removed and a thin layer ice was placed on the electrodes and the CDC's response was again noted while operating it at 1 kHz followed by 100 kHz. Figure 5 shows the change in the capacitance value observed in the presence of water and ice. It clearly shows that when water was placed the change in capacitance observed is almost same at both the frequencies but when ice was placed the relative change in capacitance was large at 1 kHz and low at 100 kHz. Thus the presence of ice can be accurately determined from the output of the CDC.

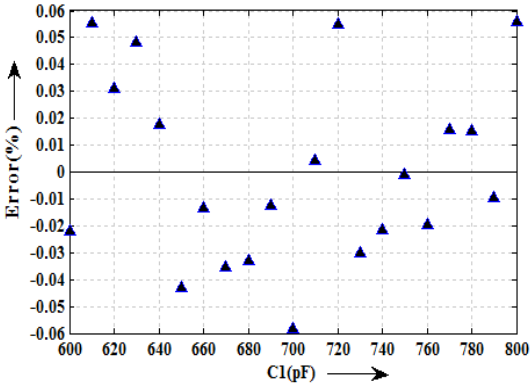

Figure 4. Percentage Error with variation in C_1 of the proposed CDC

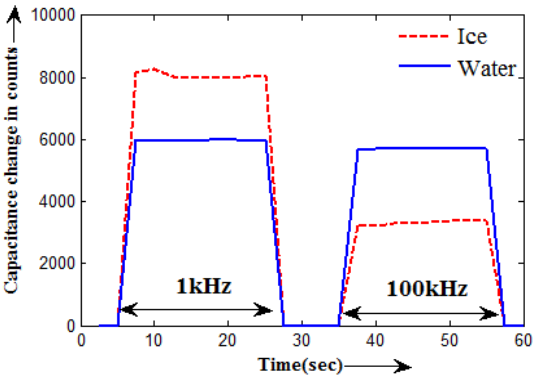

Figure 5. Detection of presence of ice using the new CDC. For water, output is same at f_{in} (source frequency) of 1 kHz and 100 kHz. It is different for ice, which helps to distinguish ice from water.

II. Conclusions

A novel CDC suitable for capacitive sensors that requires sinusoidal electrical excitation is presented. Principle of operation of the CDC, details of the prototype unit developed and test results are described breifly. Worst case error noted during the experiment was 0.06%. An error analysis has been conducted and found that the CDC output has very low effect due to variations in circuit parameters. The developed CDC will have many industrial applications such as humidity sensing, touch sensing, ice detection, etc. Presence of an ice layer was detected using the developed CDC along with suitable capacitive electrodes.

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