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New Effective Architectures and Conversion Algorithms for Adaptive Sub-ranging A/D Converters

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Abstract- The paper is devoted to the new effective architectures and conversion algorithms used in adaptive sub-ranging analog-to-digital converters (ADCs) whose digital parts allow the iterative calculation of output codes using digital estimation algorithms. Two classes of adaptive sub-ranging ADCs, i.e. recursive (cyclic) and pipeline ADCs, are considered in the paper. The paper develops the earlier research on the adaptive sub-ranging ADCs and removes the crucial disadvantages of these converters simplifying their architectures, i.e. decreasing significantly the high resolution of internal D/A sub-converters and very large values of internal amplifiers gains. The appropriate new conversion algorithms and the results of simulation experiments which compare ADC employing the proposed converter with the existing pipeline ADC are presented and discussed.

I. Introduction

The paper develops the investigations carried out in the Institute of Electronic Systems, Warsaw University of Technology on adaptive sub-ranging A/D converters (ADCs), in previous papers called also intelligent cyclic (recursive) or pipeline ADCs [1-4]. The adaptive sub-ranging ADCs employ an original A/D conversion method based on application of the analytical approach to optimization of adaptive estimation algorithms [5]. The approach permits to determine analytically the most efficient values of converter parameters which guarantee maximal performance of conversion under given permissible probability of internal saturations.

The conventional sub-ranging ADCs form the output codes of converted samples shifting sub-codes taken from the output of the internal A/D sub-converters with low resolution and appropriate "gluing" them to the end of the output codes obtained in the previous iterations [6,7]. The adaptive sub-ranging ADCs employ adaptive estimation algorithms for output codes calculation, which requires the specialized digital part integrated with the analog part of the converter. In the subsequent iterations of conversion, more and more significant (properly estimated) bits appear in the code calculated in the digital part of ADC. The rate of increase of the number of significant bits depends on the parameters of the analog ADC components and the corresponding algorithm of the output codes calculation. Application of long-bit operations in the digital parts of the adaptive sub-ranging ADCs permits to remove the inevitable in conventional converters restriction on the gains of internal amplifiers which should have only the values of gains equal to integer powers of two. Impossibility to set the gains to each theoretically required value limits the entire utilization of resources of the analog components of the conventional converters. To avoid errors related to the saturations caused by technological errors and noises, the conventional sub-ranging ADCs employ so called overlap or redundant bits [6,7], which results in decrease of the inter-stage amplifiers gains and incomplete utilization of the analog components and, in consequence, decreases their potential resolution. In the adaptive sub-ranging ADCs, the possible saturations are excluded by setting the gains of internal amplifiers to the maximal values determined analytically, guaranteeing the given (acceptable) probability of saturation. Grater gains of the amplifiers and the appropriate algorithm of conversion enable reaching the overall parameters (e.g. effective numbers of bits – ENOB) of the adaptive sub-ranging ADCs better than in the conventional sub-ranging ADCs with similar analog components and comparable probability of saturation [1-3].

The practical implementation of the recursive (cyclic) adaptive sub-ranging ADC [4], operating according to the approach presented in [1,2], in CMOS technology, indicates that design of internal high-resolution D/A converters (DACs) and amplifiers whose gains have very large values, calculated consistently with results of [1,2], is a very challenging task. For example, the gain before the last cycle of conversion should be approximately equal to $2^{N-N_{ADC}}$, where N is the expected resolution of the sub-ranging ADC and N_{ADC} is the

resolution of its internal sub-ADC. The amplifier circuits with such gains are very complex. Therefore, we started investigations on new, more effective architectures of adaptive sub-ranging ADCs, in which both the resolutions of the internal sub-DACs and the gains of the internal amplifiers would be lower than in the standard adaptive sub-ranging ADCs. The changes of the architectures applied in the adaptive sub-ranging A/D converters results in changes in the approach to optimization of the converters operation and significant changes in the digital coefficients used previously in these converters for output codes calculation. The conversion algorithm presented in this paper was developed on the basis of slightly other assumptions for the errors and noises distributions in comparison to previous works of the author and his co-workers [1-3], i.e. particular errors and noises are considered as separate components and their values are within the assumed limited ranges.

II. Architectures of adaptive sub-ranging A/D converters

The proposed architectures of the adaptive sub-ranging ADCs which use the correspondingly modified adaptive conversion algorithms are presented in Fig. 1. Fig. 1a relates to the recursive (recirculating [6], cyclic) architecture of sub-ranging ADCs used e.g. in such converters as AD678, AD679, AD779. However, the architecture presented in Fig. 1a is different than in the ADCs mentioned above because the resolution of the internal sub-DAC (SDAC$_k$) is the same as the resolution of the flash sub-ADC (SADC$_k$), whereas in AD678, AD679, AD779 the resolution of the internal DAC is equal to the overall output resolution of these ADCs. Fig. 1b relates to the pipeline architecture of sub-ranging ADCs used e.g. in such converters as AD9467, AD9240, AD6645, MAX1205. A structure of the k-th stage of the proposed architecture is the same as in the conventional pipeline ADCs [6,7] and the difference, in comparison with the proposed converters, is only in the values C_k of the inter-stage amplifiers gains. On the other hand the basic difference between the architectures considered in this paper and the ADCs architectures considered by the author and his co-workers in the previous papers (e.g. [1-3]) is that the subsequent cycles/stages of ADC have the sub-ADCs and sub-DACs with the same resolution and send to the next cycles/stages only the analog residual signals like in classical pipeline converters. This enables that the gains of the internal amplifiers can be significantly lower than for the standard adaptive sub-ranging ADCs [1-3].

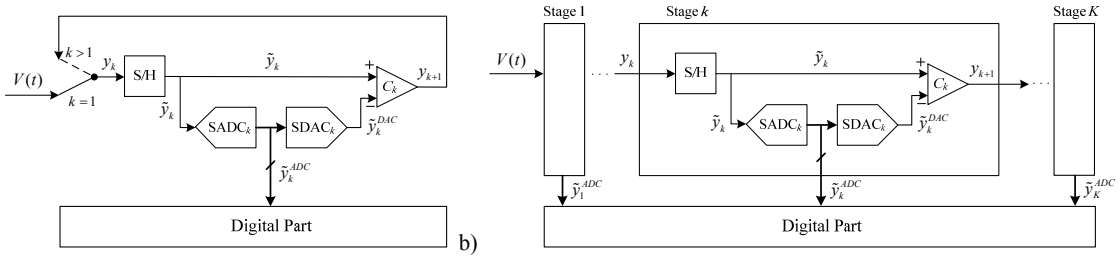

Figure 1. Architectures of adaptive recursive (a) and pipeline (b) sub-ranging A/D converters.

The considered sub-ranging ADCs shown in Fig. 1 operate in the following way. In the k-th cycle ($k = 1,2,...,K$) of the recursive sub-ranging ADC operation or in the k-th stage of the pipeline ADC, the analog input signal is sampled by the sample-and-hold (S/H) circuit. In the first cycle/stage, the input signal of S/H $y_1 = V(nT) = V$ is simply a signal being converted, and in the next cycles/stages the input signal of S/H y_k is the residual signal from the output of the previous cycle/stage. The output signal from S/H circuit $\tilde{y}_k = y_k + \nu_k^{S/H}$ (including the noise or error of S/H circuit $\nu_k^{S/H}$) is quantized by the internal fast A/D sub-converter (SADC$_k$) with the number of output bits equal to $N_{ADC,k}$, usually taking values from 1 to 6 bits. The $N_{ADC,k}$-bit digital output $\tilde{y}_k^{ADC}$ produced by SADC$_k$ drives the internal D/A sub-converter (SDAC$_k$) which forms the analog signal $\tilde{y}_k^{DAC}$ - the quantized version of the input signal of SADC$_k$ $\tilde{y}_k$. The model of the analog signal $\tilde{y}_k^{DAC}$ at the output of SDAC$_k$, which takes explicitly into account the limited input range $[-D, D]$ of SADC$_k$, is as follows:

$$\tilde{y}_k^{DAC} = \begin{cases} \tilde{y}_k & \text{for } |\tilde{y}_k| \le D \\ D\ \text{sign}(\tilde{y}_k) & \text{for } |\tilde{y}_k| > D \end{cases} + \xi_k^{ADC} + \nu_k^{DAC}, \qquad (1)$$

where ξ_k^{ADC} is a quantization error and ν_k^{DAC} denotes an analog error/noise at the output of SDAC$_k$. The mid-riser form of the quantizer is assumed and the example of the transfer function for ideal (without errors) 3-bit SADC$_k$ and SDAC$_k$ is depicted in Fig. 2. The output of S/H circuit $\tilde{y}_k$ is also routed to the positive input of the

inter-stage amplifier with the gain C_k. The negative input of the amplifier is connected to the output of SDAC$_k$. The amplified signal $y_{k+1} = C_k e_k + v_k^{AMP}$, where $e_k = \tilde{y}_k - \tilde{y}_k^{DAC}$ and v_k^{AMP} denotes an output error/noise of the inter-stage amplifier, is directed to the input of the next (k+1)-th cycle/stage.

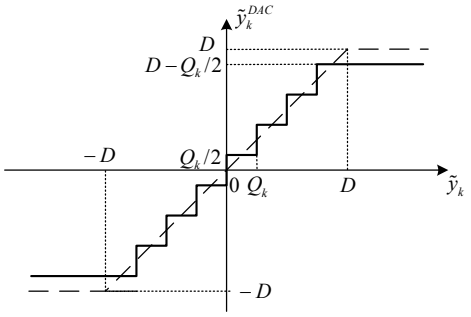

Figure 2. Ideal transfer function for 3-bit SADC$_k$ and SDAC$_k$.

The digital part of the converter computes the estimates (codes) $\hat{V}_k$ of the input samples V on the basis of sub-codes $\tilde{y}_k^{ADC}$ delivered by SADC$_k$ from the subsequent cycles/stages according to the following relationship:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k^{ADC} = \sum_{i=1}^{k} L_i \tilde{y}_i^{ADC} , \qquad (2)$$

where L_k are the values of digital coefficients used for calculation of the output codes and are directly related to the values of the inter-stage gains C_k. Typically in conventional sub-ranging ADCs [6,7], the inter-stage gains C_k have values equal to the integer powers of two $C_k = 2^{N_{ADC,k}-m_k}$, where $N_{ADC,k}$ is the number of bits of SADC$_k$ and m_k is the number of redundant bits used for digital correction of the errors caused by noises and distortions in analog components of sub-ranging ADCs, among others by imperfect inter-stage gains which exceed $2^{N_{ADC,k}}$ (in case of non-redundant stages) and cause saturations in the next cycles/stages. Commonly, one bit of redundancy is used ($m_k = 1$). The restriction on values of the gains ($C_k = 2^{N_{ADC,k}-m_k}$) is connected with the simple method of forming output codes, used commonly in the conventional sub-ranging ADCs. The method is illustrated in Fig. 3. The output codes from particular cycles/stages $\tilde{y}_k^{ADC}$ are subsequently shifted by $N_{ADC,k} - m_k$ (in this case 3) bits and next combined. To correct the errors in sub-ranging ADCs, there are also employed other structures of sub-ranging ADCs with so called "plus 0.5 bits" stages (e.g. 1.5-bits, 2.5-bits and so on) including additional comparators in particular stages [6,7].

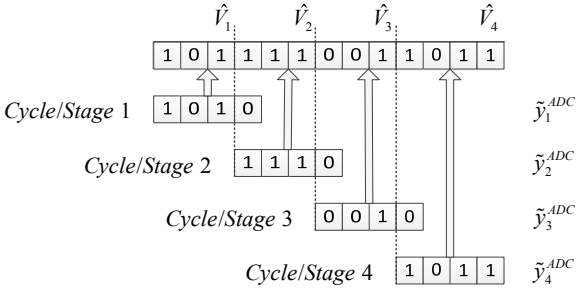

Figure 3. Forming of output codes in conventional sub-ranging A/D converters.

To obtain the most accurate estimates (codes) of the input samples, the values of the gains C_k in particular cycles/stages should be as large as possible to amplify the analog residual signals $e_k = \tilde{y}_k - \tilde{y}_k^{DAC}$ in such a way that the whole range of the A/D sub-converter in the next cycle/stage will be used. The best results give the values $C_k = 2^{N_{ADC,k}}$, but because of imperfections of the ADCs internal components, mentioned above, the saturation of SADC$_{k+1}$ can occur and the designers should decrease the gains. Due to the way of forming output codes in the conventional sub-ranging ADCs (Fig. 3), the gains C_k are decreased and set to the values $C_k = 2^{N_{ADC,k}-m_k}$ being the integer powers of two. These values are smaller than values theoretically sufficient for elimination of the saturation and it causes that the converter components are utilized incompletely. This results in worsening of the achievable overall parameters of sub-ranging ADCs (e.g. ENOB) in comparison with the

potentially available ones. To utilize entirely the input ranges of the internal coarse sub-ADCs as well as all information from the sub-codes $\tilde{y}_k^{ADC}$, the application of the specialized digital part in the sub-ranging ADCs with long-bit operations is proposed, similarly as in [1-3]. Then, the restriction on the gains C_k (having only the values equal to integer powers of two) is removed and any values, guaranteeing the assumed level of saturations, of the gains C_k and the digital coefficients L_k in (2) can be used. Of course, the digital part of the converter has to be extended to enable calculation of the output codes according to (2). But the calculations to be done are not very complicated and can be realized in the simple digital unit.

III. Optimization of adaptive sub-ranging A/D converters

The conversion algorithm used in the adaptive sub-ranging ADC for calculation of the output codes $\hat{V}_k$ is expressed by the relationship (2). The optimization of the converter operation consists in searching the values of the gains C_k and the corresponding digital coefficients L_k which give the best parameters of ADC taking into account possible noises and distortions of the converter components as well as their limited input ranges (1). As the basic measure of the conversion quality the effective number of bits (ENOB) was assumed. ENOB is directly connected with the root-mean-square value of noise and distortion (NAD) [8] which can be interpreted as a measure of the estimation errors of the output codes $\hat{V}_k$ (2). As was stated above, the greater values of the gains C_k permit to employ entirely the whole input range of the internal A/D sub-converters and, in consequence, to achieve the lower values of NAD and greater values of ENOB. At the same time, the gains cannot be too large, because of the possibility of internal saturations, and should be adjusted to the values of parameters (related to technological errors and noises) of particular analog components. The values of gains C_k and digital coefficients L_k should be optimized under the condition guaranteeing no saturation in the A/D sub-converters (SADC$_k$):

$$\left|\tilde{y}_k\right| \le D\,. \tag{3}$$

The strict analysis of distributions of the residual signals $\tilde{y}_k$ under general assumptions concerning errors and noises in the internal components of the sub-ranging ADCs is very complicated. There are some analytical results for pipeline ADC architectures obtained in case if there are no imperfections of the components and stage mismatches [9]. Other results of distributions analysis used for increase of resolution of multistage ADCs are presented in [10]. Below, another attempt of analysis of behavior of the residual signals $\tilde{y}_k$, which allows finding the values of the gains C_k which guarantee no saturation in the A/D sub-converters, is presented.
Assuming that the conversion in the previous (before k) cycle/stage of the adaptive sub-ranging ADC was performed without saturations (then $\tilde{y}_{k-1}^{DAC} = \tilde{y}_{k-1} + \xi_{k-1}^{ADC} + \nu_{k-1}^{DAC}$, see (1)), we can derive the relationship for $\tilde{y}_k$:

$$\begin{aligned}\tilde{y}_k &= C_{k-1}(\tilde{y}_{k-1} - \tilde{y}_{k-1}^{DAC}) + \nu_{k-1}^{AMP} + \nu_k^{S/H} = C_{k-1}(\tilde{y}_{k-1} - \tilde{y}_{k-1} + \xi_{k-1}^{ADC} + \nu_{k-1}^{DAC}) + \nu_{k-1}^{AMP} + \nu_k^{S/H} = \\ &= C_{k-1}(-\xi_{k-1}^{ADC} - \nu_{k-1}^{DAC}) + \nu_{k-1}^{AMP} + \nu_k^{S/H}\,.\end{aligned} \tag{4}$$

To follow the further analysis, we have to assume some distributions or ranges of particular variables (errors) in (4). Let us assume that the analog errors/noises ν_{k-1}^{DAC} at the output of SDAC$_{k-1}$ are within the range $[-\Delta_{k-1}^{DAC}, \Delta_{k-1}^{DAC}]$, where the level Δ_{k-1}^{DAC} of maximal errors/noises is related to the technology of ADC manufacturing and circuit solutions employed in ADC. Similarly, we assume that the analog errors/noises ν_{k-1}^{AMP} at the output of the amplifier are within the range $[-\Delta_{k-1}^{AMP}, \Delta_{k-1}^{AMP}]$ and $\nu_k^{S/H}$ at the output of S/H circuit within the range $[-\Delta_k^{S/H}, \Delta_k^{S/H}]$. We also assume that the quantization errors ξ_{k-1}^{ADC} are within the range $[-Q_{k-1}/2, Q_{k-1}/2]$, where Q_{k-1} is the quantization step of SADC$_{k-1}$. Taking into consideration these assumptions and using (4) we can state from (3) that the following inequality has to be satisfied for C_{k-1}:

$$C_{k-1}(Q_{k-1}/2 + \Delta_{k-1}^{DAC}) + \Delta_{k-1}^{AMP} + \Delta_k^{S/H} \le D\,. \tag{5}$$

Then, the greatest value of C_{k-1} guaranteeing no saturation in the k-th cycle/stage is as follows:

$$C_{k-1} = \frac{D - (\Delta_{k-1}^{AMP} + \Delta_k^{S/H})}{Q_{k-1}/2 + \Delta_{k-1}^{DAC}}\,. \tag{6}$$

The values of the digital coefficients L_k corresponding to the gains C_{k-1} in the previous cycle/stage used for calculation of the output codes can be calculated for $k > 1$ ($L_1 = 1$) according to:

$$L_k = \prod_{i=1}^{k-1} C_i^{-1} = \frac{L_{k-1}}{C_{k-1}}\,. \tag{7}$$

The relationships (2), (6), (7) define the conversion algorithm which guarantees no saturation of the sub-ADCs for the assumed models of errors and noises. However, there are also other sources of distortions in the sub-ranging ADCs, among others errors of the inter-stage gains setting, offsets or nonlinearities of internal components of sub-ranging ADCs, which can be taken into consideration on the maximal acceptable value of the gains C_k in the similar way. For example, if we assume that the actual gains have the values $C_{k-1}^{err} = C_{k-1}(1+\gamma_{k-1}^{C})$ and the relative gain setting errors γ_{k-1}^{C} are within the range $[-\delta_{k-1}^{C}, \delta_{k-1}^{C}]$, then $C_{k-1}^{err} \in [C_{k-1}(1-\delta_{k-1}^{C}), C_{k-1}(1+\delta_{k-1}^{C})]$ and the condition (3) can be written as:

$$C_{k-1}(1+\delta_{k-1}^{C})(Q_{k-1}/2+\Delta_{k-1}^{DAC})+\Delta_{k-1}^{AMP}+\Delta_{k}^{S/H} \le D\,. \tag{8}$$

In this case, the greatest values of C_{k-1} are determined by the following equation:

$$C_{k-1} = \frac{D-(\Delta_{k-1}^{AMP}+\Delta_{k}^{S/H})}{(Q_{k-1}/2+\Delta_{k-1}^{DAC})(1+\delta_{k-1}^{C})}\,. \tag{9}$$

This result, which takes into consideration the possible errors of the inter-stage gain setting (inter-stage mismatches), is very important from practical point of view because the errors connected with the inter-stage mismatches are the main reason of employing the redundant bits in the conventional sub-ranging A/D converters causing the limited utilization of the resources of the converters components [6,7].

IV. Results of simulation experiments

To illustrate the potential advantages of the proposed modified adaptive sub-ranging ADCs, the simulation models of the existing pipeline A/D converter AD9467 [11] and the adaptive sub-ranging ADC (AS ADC) using the algorithm (2), (6), (7) and having the same values of main parameters as AD9467, especially the same resolutions of sub-A/D and D/A converters in particular stages, were developed. The AD9467 architecture consists of seven stages: "a 3-bit first stage, a 4-bit second stage, and four 3-bit stages and a final 3-bit flash. Each stage provides sufficient overlap to correct for flash errors in the preceding stage" [11].
The performance of the converters was compared using the empirical values of Effective Number of Bits (ENOB) achieved after k stages which were calculated according to the definition given in [8]:

$$ENOB_k = \log_2\left(\frac{FSR}{NAD_k \cdot \sqrt{12}}\right), \qquad NAD_k = \sqrt{\frac{1}{M}\sum_{m=1}^{M}\left[\hat{V}_k^{(m)} - V^{(m)}\right]^2}\,, \tag{10}$$

where $FSR = 2$ V is the full-scale range of the converter and NAD_k is the root-mean-square value of noise and distortion [8] after k cycles/stages. The empirical values of ENOB were calculated on the basis of the results of conversion of the same sequences of signal samples $V^{(m)}$ $(m = 1,...,M)$, uniformly distributed in the whole input range of the converters, where $M = 100000$ is the number of samples converted in the given experiment.
The values of ENOB achieved after subsequent stages for the AD9467 model (red lines) and for the adaptive sub-ranging ADC (blue lines) are presented in Fig. 4. Because we have no information about the level of internal analog errors/noises in particular stages of AD9467, the maximal level of internal errors/noises was assumed arbitrary to a certain extent, on the basis of information published in [11]. The experiments were conducted for three values of the level of maximal errors/noises assumed for all analog errors/noises considered in Sect. III: $\Delta_k^{S/H} = \Delta_k^{DAC} = \Delta_k^{AMP} = 10,\ 50,\ 100$ µV – Figs 4a, 4b and 4c respectively.

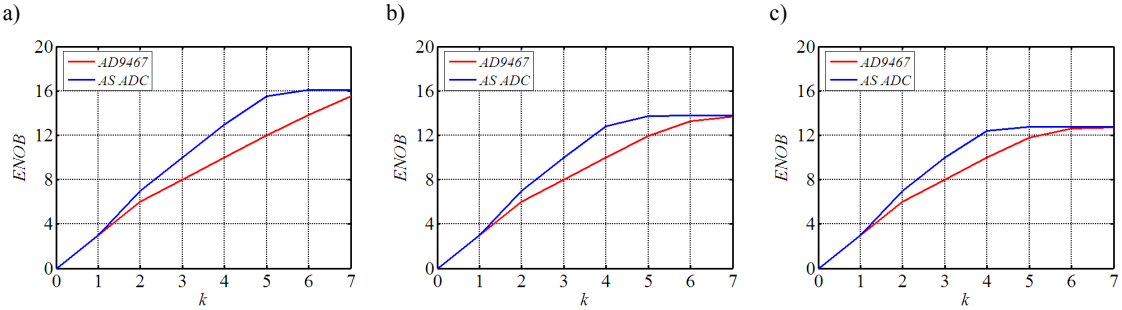

Figure 4. ENOB achieved after k stages for AD9467 and adaptive sub-ranging ADC models for different level of internal errors/noises: (a) 10 µV, (b) 50 µV, (c) 100 µV.

For all considered levels of noises, the values of ENOB achieved for the adaptive sub-ranging ADC grow significantly faster than ENOB obtained for AD9467. In all cases, the adaptive sub-ranging ADC needs only five stages (two stages less than AD9467) to obtain the same level of ENOB as AD9467 after seven stages. According to the data sheet [11], ENOB of AD9467 is about 12.2 bits, which relates to the results of simulations experiments obtained for the level of analog errors/noises equal to 100 μV . In this case, the adaptive sub-ranging ADC can obtain the same ENOB as AD9467 using only first five stages of AD9467. Moreover, ENOB obtained for the adaptive sub-ranging ADC employing four stages is very close to ENOB of AD9467 with seven stages. Other simulation experiments devoted to many different aspects of the new adaptive sub-ranging ADCs operation can be performed using the dedicated Matlab toolbox developed by the author [12]. The models of the converters and their components implemented in this Toolbox take into consideration many imperfections such as offsets, gain errors, differential and integral nonlinearities of internal sub-ADCs and sub-DACs, offsets, gain errors, common-mode errors and noises of amplifiers, offsets, gain errors and noises of S/H circuits, as well as the limited length of words used in the digital part of ADC for output codes calculations.

V. Conclusions

The modified adaptive sub-ranging ADCs employing the modified digital conversion algorithm and the simplified architectures have the significantly lower complexity in comparison with the standard adaptive sub-ranging ADCs proposed earlier in [1-3]. This is related to decrease of the resolutions of sub-DACs which are equal to the low resolution of sub-ADCs (in every stage/cycle of conversion), and to decrease of the gains of inter-stage amplifiers. These two changes decrease significantly the size and power consumption of the analog part of the adaptive sub-ranging ADCs. In comparison with the conventional sub-ranging ADCs, the proposed architectures employ the modified digital parts for output code calculation according to the proposed algorithm. The complexity of the digital part is higher than in conventional sub-ranging converters, but is not very high. The digital part performs only the simple operation of addition and multiplication.
Simultaneously, the modified versions of the adaptive sub-ranging ADCs preserve the most important advantage of the standard adaptive sub-ranging ADCs, i.e. the faster growth of ENOB achieved after particular cycles/stages in comparison with the known conventional sub-ranging ADCs with similar analog components.

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