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A New Peak Detector Based on Usage of CCCIIs

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Abstract: The paper presents a completely new realization of peak detector/full-wave rectifier of input sinusoidal signals, employing four CCCIIs (controlled current conveyors), metal-oxide-semiconductor transistors and single grounded capacitor, without any external resistors and components matching requirements. The circuit gives a DC output voltage that is the peak input voltage over a wide frequency range, with a very low ripple voltage and low harmonic distortion. The proposed circuits use an all-pass filter as a 90^0 phase shifter of the square value of the processed input signal. The proposed circuit is very appropriate to further develop into integrated circuits. To verify the theoretical analysis, the circuit PSpice simulations has also been included, showing good agreement with the theory.

Keywords: Controlled current conveyor (CCCII); controllable all-pass filter; harmonic distortion; precision peak detector; ripple voltage.

I. Introduction

Precise full-wave rectification function is one of the important requirements in many applications, such as instrumentation and measurement [1]. It is generally used in AC voltmeters and ampermeters, signal-polarity detectors, averaging circuits, sample-and hold circuits, peak value detectors, clipper circuits, and amplitude-modulated signal detectors. In all of these applications, the use of a diode to provide the rectification has the serious drawback of having to overcome the threshold voltage of the diodes. This problem prevents the rectification of signals below a voltage of about 0.6 V.

The current-mode (CM) circuits, such as the second–generation current conveyors CCIIs, have received considerable attention due to their better linearity, wider bandwidth, larger dynamic range, and low power dissipation compared with their voltage-mode counter-parts, such as operational amplifiers (OAs) [2]. The CCIIs, first introduced in [3], are functionally flexible and versatile. Thus, they have been used in a very large number of different applications such as universal filters, inductor simulators, capacitance multipliers, oscillators, full-wave rectifiers. It is the use of CCIIs, due to high output impendence of the current conveyor, that makes it possible to overcome the turn-on resistance of the diode, permitting the rectification of low-level signals (in most of the cases rectifier was based on usage of diodes) and also responding to frequencies over 100 kHz. However, the CCII can not control the parasitic resistance at x (R_x) port so when it is used in some circuits, it must unavoidably require some external passive components, especially the resistors. This makes it not appropriate for IC implementation due to occupying more chip area, high power dissipation and without electronic controllability. On the other hand, the introduced second-generation current controlled conveyor (CCCII) has the advantage of electronic adjustability over the CCII [4]. Also, the use of dual-output current-conveyors is found to be useful in the derivation of current-mode single input circuits. The use of the current conveyor to improve performance of an OA-based circuit was discussed further in [5]. Full-wave rectifiers based on a CMOS class AB amplifier and current rectifier operation are described in [6]. This circuit offers a wide dynamic range and shows a broadband operation. CMOS integrated active rectifier concept are an innovative approach for higher efficiencies [7]. These rectifiers provide output voltages nearly at the level of the input voltage combined with low power consumption, which has also been achieved through the circuit design suggested here.

A typical technique to design a peak detector employs, along with filtering circuits, op-amps as the active elements [8]. However, it may degrade the transient response of the sinusoidal peak detector. Hence, the transient performance of equipment that uses the typical technique can be improved by using the sinusoidal peak detector with fast transient response. Therefore, the shortcomings are obviously a large configuration but a small operating frequency range and, not less important, a slow response due to the filtering. In this paper, new development of an analogue peak detector is presented with the goal to alleviate the above problems.

The features of the proposed circuit are that: the circuit description is very simple; it employs four CCCIIs and single grounded capacitor as passive component, which is suitable for fabrication in monolithic chip. The angle pole frequency of the realized all-pass filter can be electronically controlled. In terms of frequency range, the proposed circuit operation covers a wide range of as many as six decades, with increased linearity and precision in determining the peak value. The performance of the proposed circuit are illustrated by PSpice simulations, they show good agreement with the calculation.

II. Proposed peak detector circuit

The proposed circuit of peak detector is shown in Figure 1.

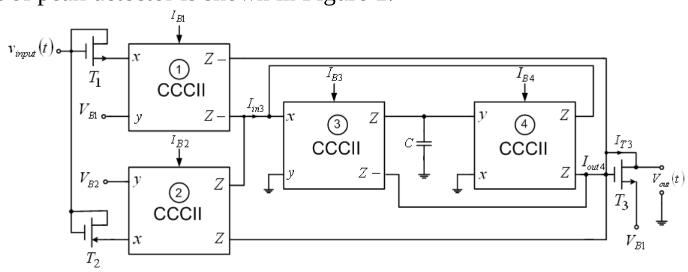


Figure 1. The proposed circuit of the peak detector

The input sinusoidal signal can be represented as:

$$v_{input}(t) = V_m \sin(2\pi f t) \quad (1)$$

where V_m is amplitude and f is frequency. The NMOS transistors (T_1, T_3) have threshold voltage $V_{Tn} \geq 0$, while the PMOS transistor T_2 has $V_{Tp} \leq 0$. The y ports of the first and second CCCIIs are biased at the threshold voltages of the MOS transistors as $V_{B1}=-V_{Tn}$ and $V_{B2}=-V_{Tp}$. The bulks of all of the MOS transistors are connected to their sources. The characteristics of the ideal CCCII are represented by the following hybrid matrix:

$$\begin{bmatrix} I_y \\ V_x \\ I_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & R_x & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_z \end{bmatrix} \quad (2)$$

If the CCCII is realized using CMOS technology, R_x can be respectively written as $R_x = \sqrt{1/(kI_B)}$. Here k is the physical transconductance parameter of the MOS transistor. I_B is the bias current used to control the intrinsic resistance at x port. In general, CCCII can contain an arbitrary number of z terminals; provide both directions of currents I_z. The internal construction of the CMOS CCCII is shown in Figure 2.

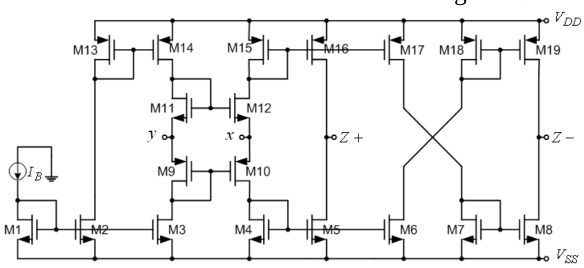


Figure 2. Schematic of the CMOS CCCII

It should be noted that the first, second and third CCCII in Figure 1 should has low impendance ($R_{x1} \cong 0$) by setting value of I_{B1}, I_{B2}, and I_{B3} as high as possible (in order to achieve low input impendance of the filter). The phase shift (for 90^0) of the square of the input signal is realized using an all-pass filter. The proposed current-mode first order all-pass filter is illustrated in Figure 1. It consists of 2 CCCIIs and one grounded capacitor. Considering the circuit in Figure 1 and using CCCII properties, the current transfer function can be rewritten to be:

$$\frac{I_{out4}}{I_{in3}} = \frac{sCR_{x4} - 1}{sCR_{x4} + 1} \quad (3)$$

From above equation, the current gain of the proposed circuit is unity and it also has the phase response as:

$$\angle H(\omega_p) = \phi(\omega_p) = 180 - 2\tan^{-1}(\omega_p C R_{x4}) \quad (4)$$

where $R_{x4} = \sqrt{1/k_4 I_{B4}}$. It can be seen in (4) that the circuit gives a phase shift from 0-(-180°). Moreover, the angle pole frequency can be electronically controlled by I_{B4}. Therefore, all of active and passive sensitivities are no more than unity in magnitude. If $v_{input}(t) > 0$, the current is conducted through the NMOS transistors T_1 to the output. However, if $v_{input}(t) < 0$, the PMOS transistor T_2 conducts the current to the output. Hence, the current-voltage relationships of the MOS transistors are given by:

$$I_{T1} = \frac{k_n}{2}(v_{GS1} - V_{Tn})^2 = \frac{k_n}{2} v_{input}^2(t);\ for\ v_{input}(t) > 0:\ I_{T2} = \frac{k_p}{2} v_{input}^2(t);\ for\ v_{input}(t) < 0 \quad (5)$$

NMOS and PMOS transistors conduct in opposite halves of the input signal. Such control enables current input from the port z+ of the first CCCII on the all-pass filter at the interval in which the input voltage signal is positive, i.e. from the port z- of the second CCCII when the input voltage is negative. Assume that:

$$k_{n(T1-T3)} = k_{p(T2)} \tag{6}$$

For the proposed circuit it follows that:

$$I_{T1} + I_{T2} + I_{out4} = \frac{k}{2}V_m^2 \sin^2(2\pi ft) + \frac{k}{2}V_m^2 \cos^2(2\pi ft) = \frac{k}{2}V_m^2 \tag{7}$$

The above represents the total current in the V_{out} node. This current will be equalised with the current of the T_3 transistor. It follows that:

$$I_{T3} = \frac{k}{2}V_m^2 = \frac{k}{2}V_{out}^2(t) \tag{8}$$

Based on (8), it is obvious that the voltage value at the output of the proposed circuit corresponds to the value of the amplitude of the input sinusoid signal. In the proposed circuit, rectification is not performed by diodes, and therefore it has fewer ripples, compared with the known diode rectifier circuits. It is also possible to perform low-voltage (below threshold level of the diode) rectification using the proposed circuit.

III. Error Analysis

Taking into account the non-ideal current gains of the CCCIIs α_1, α_2, α_3 and α_4 (ignoring the effects of voltage gains); the output voltage (Figure 1) is given by:

$$V_{out}(t) = \sqrt{\left(\alpha_1 v_{input}^2(t)_+ + \alpha_2 v_{input}^2(t)_{-+} + \frac{\alpha_4}{\alpha_3} v_{input}^2(t)^*\right)} \tag{9}$$

$$v_{input}(t)_+ = \begin{cases} v_{input}(t), \text{ for } v_{input}(t) > 0 \\ 0, \text{ otherwise} \end{cases}; \quad v_{input}(t)_- = \begin{cases} v_{input}(t), \text{ for } v_{input}(t) < 0 \\ 0, \text{ otherwise} \end{cases}; v_{input}(t)^* = V_m \cos(2\pi ft)$$

If electronically tuneable CCs (ECCIIs) are employed instead of CCs for the proposed circuit, the parameters α_1, α_2, α_3 and α_4 can be used as tools to change the values of the input voltages or to compensate for the error in their values. If (6) is not satisfied, the following inequality is obtained:

$$V_{out}(t) = \sqrt{\left(\alpha_1 v_{input}^2(t)_+ + \alpha_2 \frac{k_p}{k_n} v_{input}^2(t)_- + \frac{\alpha_4}{\alpha_3} v_{input}^2(t)^*\right)} \tag{10}$$

It is observed in (11) that the square of the negative cycles of input signal and 90° shifted input signal is multiplied by k_p/k_n instead of unity. Fortunately, using ECCs, $\alpha_1 = \alpha_2 k_p / k_n = \alpha_4 / \alpha_3 = 1$ can be adjusted. It is obvious that the equation (8) is valid under the ideal condition: $V_m = V_m^*$; $-2\tan^{-1}(2\pi f R_{x4} C) = \pi / 2$; $\alpha_1 = 1$; $\alpha_2 = 1$; $\alpha_3 = 1$; $\alpha_4 = 1$; $k_p / k_n = 1$; $\lambda_i v_{DS\,i} = 0, i = [1,3]$, where λ, the channel-length modulation parameter, models current dependence on drain voltage due to the Early effect, or channel length modulation. In proposed circuits $v_{DSi} = v_{GSi}$. The output voltage, $v_{out}(t)$ in non-ideal condition becomes:

$$v_{out}(t) = \sqrt{\left(\alpha_1 v_{input}^2(t)_+ (1+\lambda_1 v_{DS1}) + \alpha_2 \frac{k_p}{k_n} v_{input}^2(t)_- (1+\lambda_2 v_{DS2}) + \frac{\alpha_4}{\alpha_3} v_{input}^2(t)^* (1+\lambda_3 v_{DS3})\right)} \tag{11}$$

A question is raised as of the nature of the output voltage in the proposed detector in circumstances when ideal conditions are not met, i.e. when the time constant $\tau = R_{x4}C$ does not fully satisfy the relation $\tau = 1/(2\pi f)$, or if $\alpha_1 \neq 1$; $\alpha_2 \neq 1$; $\alpha_3 \neq 1$; $\alpha_4 \neq 1$; $k_p / k_n \neq 1$; $\lambda_i v_{DSi} \neq 0, \quad i = [1,3]$, i.e. it becomes important to determine the level of sensitivity to the changes in these parameters, within a range bordering with their nominal values. The sensitivity to a change in a parameter will be determined as the first derivative of the output voltage, according to the given (analysed) parameter. If the ideal conditions are not met, then:

- An alternate component (ripple) will occur, superposed to direct-current voltage at the output. The ripple voltage is obtained from the output waveform of the signal by using the following expression:

$$V_{ripple} = \sqrt{\sum_{i=1}^{N} (V_i - \bar{V})^2 / N} \tag{12}$$

where $\bar{V} = \sum_{i=1}^{N} V_i / N$, and $V_1, V_2, \ldots, V_N$ are the output voltages at sampling point $i = 1,2,\ldots,N$, respectively. The divergence in the parameter from the nominal, ideal value will cause a ripple in the output signal (the frequency of the input signal was assumed to be 2 MHz, while the amplitude of the input signal is assumed to be 1 V).

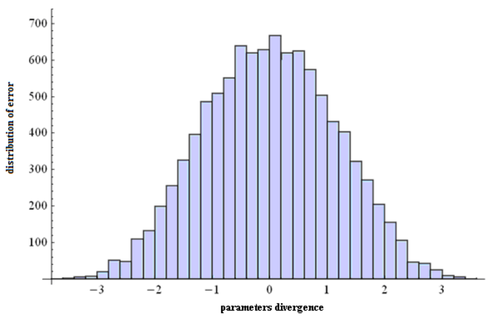
- The dependency of the ripple voltage at the output voltage in the proposed detector to the changes in parameter $\lambda_i v_{DSi} \neq 0, i = [1,3]$, is similarly as for α (in same range and has same nature).

The mean value of the voltage at the output of the detector will no longer equal the amplitude V_m. The mean value $v_{out}(t)$ will be taken as the result of measuring performed in non-ideal conditions, and this value will consequently be compared with the amplitude of the input signal V_m.

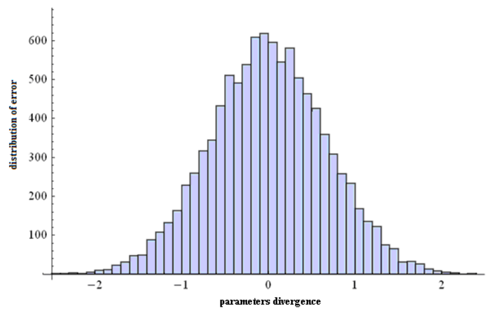
Table 1. The size of the error in determining the amplitude of the input voltage, which occurs as a consequence of the non-ideal nature of the components applied in the circuit proposed in Figure 1

Parameter	Sensitivity	Ripple	
		V_{pp} [mV]	V_{RMS} [mV]
V_m^*	0.5	10	3.5
τ	*Function determined as the first derivative of the output voltage.*	10	3.5
α_1	0.25	5	1.8
α_2	0	5	1.8
α_3	0.125	5	1.8
α_4	0.125	5	1.8
$k = k_p / k_n$	0.125	5	2.2
$\lambda_1 v_{DS1}$	0.25	5	1.8
$\lambda_2 v_{DS2}$	0.25	5	1.8
$\lambda_3 v_{DS3}$	0,125	5	1.8

Table 1 shows the parameters that are supposed to have the potential of varying around their nominal values: the sensitivity of the result of measuring the amplitude of the input voltage to a change in the circuit parameter; as well as the size of the ripple, occurring as a consequence of these variations. For example, if the parameter V_m^* should for any reason be changed by 1 % (so that its value becomes $V_m^* = 1.01 V_m$), the output value (the mean value $v_{out}(t)$) will be changed by 0.5 % while also – when all the stated parameters are shifted by +1 %, an error of 1.6 % is obtained.



a)



b)

Figure 3. a) The distribution of errors, for the even distribution of the divergence in the value of the parameters, from their nominal values; b) The distribution of errors, for the Normal distribution of the divergence in the value of the parameters, from their nominal values.

The situation, in which each parameter fluctuates randomly, at a simultaneous and independent rate, has also been analysed:

- Within the scope ranging from -3 % to +3 %, with an equal distribution;
- With a Normal distribution (the expected value: 0 %, standard divergence: 1 %) – this is within the approximate range of the previous even distribution.

The size of the error occurring due to the divergence of the parameters in accordance with the assumed distributions has also been calculated - Figure 3. For an even distribution, a change in the parameters within the range of -3 % to +3 % will result in an error that will practically not exceed the value of ±3 %. In the Normal distribution (N(0,1)), the practical error does not exceed the value of ±2 %. The results obtained by simulations and experimental checks have fully confirmed these assumptions.

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IV. Simulation results

The working of the proposed circuit has been verified using PSpice simulation program. The PMOS and NMOS transistors have been simulated by respectively using the parameters of a 0.25 μm TSMC CMOS technology [9]. The aspect ratios of a PMOS and NMOS transistor are listed in Table 2. Figure 2 depicts schematic description of the CCCII used in the simulations. The circuit was biased with ±1.25V supply voltages, C=0.1 nF, I_{B1}=I_{B2}=I_{B3}=300μA and I_{B4}=50μA. In addition, V_{B1}=-0.4238 V and V_{B2}=0.5536 V are chosen.

Table 2: Dimensions of the Transistors

Transistor	W (μm)	L (μm)
M1-M8	5	0.5
M9-M10	16	0.25
M11-M12	8	0.25
M13-M15, M17-M19	15	0.5
M16	15.1	0.5

Figure 4 shows the waveform of the proposed circuit for input signals of amplitude 1 V and frequency 2 MHz. From Figure 4 we can conclude that the signal at the output of the proposed circuit contains less ripple voltage in comparison with wave form of the previously reported circuits [10, 11], especially at a higher frequency range. This improvement is due to the absence of peak-value-to-minimum-value variation taking place twice in the output waveform for one cycle, in which one diode conducts for one half cycle and other diode conducts for the other half cycle. The proposed solution also enables performing low-voltage rectification (below threshold level of the diode).

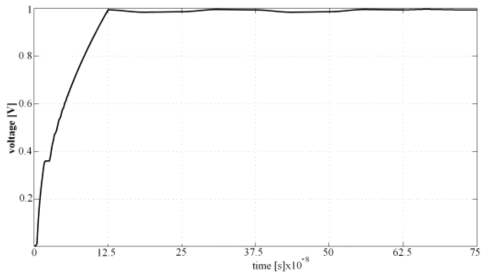
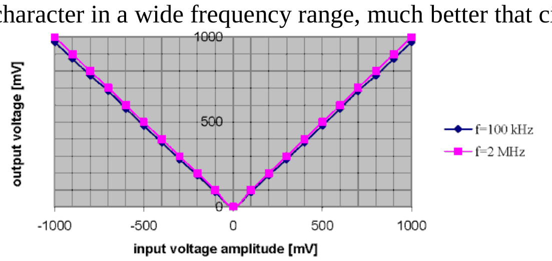
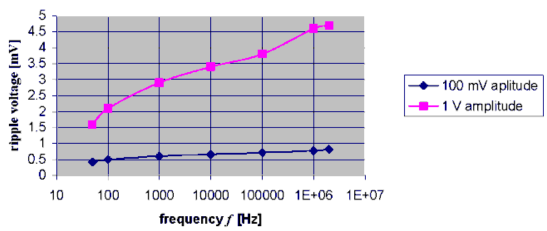


Figure 4. The rectified output waveforms of the proposed circuit for input amplitude voltage of 1V at 2 MHz.

The DC characteristics of the proposed circuit for a frequency of 100 kHz and a high frequency of 2 MHz are shown on Figure 5 a). Based on Figure 5 a), it can be concluded that the proposed circuit retains a linear character in a wide frequency range, much better that circuits reported in [7, 12].



a)



b)

Figure 5. a) DC output voltage versus DC input voltage; b) Ripple voltage versus frequency curve for the proposed circuit.

A. Ripple Voltage

For better performance of a rectifier, the value of the ripple should be very low [11]. Based on the obtained results, Figure 5 b), the ripple voltage of the proposed circuit is much lower than in previously reported circuits of rectifiers [9, 11, 13, 14]. For the proposed circuit, with an input signal of 100 mV, it was obtained a low ripple voltage of 0.45 mV at 50 Hz and 0.81 mV at 1 MHz. With an input voltage of 1V amplitude, the ripple voltages are obtained as 1.6 mV at 50 Hz and 4.6 mV at 1 MHz.

B. Harmonic Distortion

A further indication of the performance of each of the full-wave rectifiers can be gleaned by examining the

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distortion already present in a full-wave rectified signal. Because of its periodic nature, these harmonic components can be analyzed by the Fourier series. The magnitude of each harmonic of a waveform as shown in Figure 6 is obtained with fast Fourier transform using PSpice.

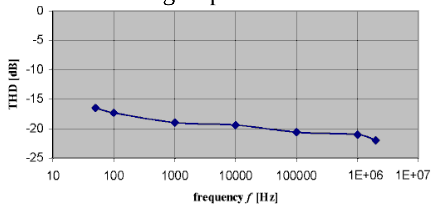

Figure 6. Total harmonic distortion (THD) versus frequency at input amplitude voltage of 1 V.

Figure 6 shows the total harmonic distortion of the output voltage of the proposed circuit, Figure 1. The THD of the proposed circuit is -16.5 dB at 50 Hz and -21 dB at 1 MHz with an input signal of 1 V. The THD is much lower than in [11, 14] (the THD of previously reported circuit slowly increases with frequency), because for higher frequency ranges, the switching ON and OFF of diodes becomes sluggish due to its higher impendence and more distortions.

V. Conclusion

In this paper an electronically tuneable current-mode peak detector has been presented. It is easy to fabricate in IC form to use in battery-powered or portable electronics equipments such as wireless devices. The circuit provides linear variation of the DC output voltage with the input voltage, with the output voltage amplitude being almost the same as the peak input voltage. The simulation results confirm the theory well. The ripple and THD of the output voltage of the proposed circuit is much lower than in previously realized rectifiers. The proposed circuit has high precision, wide bandwidth, and high accuracy.

Acknowledgements

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