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A Folding ADC Based on Switched Capacitor Circuits in 350-nm CMOS

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Abstract- This paper presents a 10-bit folding analog-digital converter (ADC) using switched capacitors (SC) circuits. In this architecture, the conversion is achieved when the signal crosses a certain voltage level and at this time, a voltage value is added or subtracted from the analog input signal. The proposed ADC consists in eight identical stages, to perform the conversion of one bit at a time. Each stage is built with a amplifier circuit using switched capacitor with gain 2. The ADC is designed in a standard 350 nm CMOS (Complementary Metal-Oxide-Semiconductor) technology. A conversion time of 570 ns and a SNDR of 56.8 dB were obtained by simulations with the ADC prototype, to a 10 bits resolution converter with 3.3 V power supply and a 8 mW power consumption.

I. Introduction

In applications where there is not much variation in the signal, as signals of sensor networks for temperature or pressure, biomedical signals, where the signals are often sparse and their frequency content varies with time. Rather than sampling such signals at a constant high rate, based on the highest expected frequency, one can allow the sampling rate to be dictated by the signal itself, resulting in event-driven sampling. One way to accomplish this is level-crossing sampling , in which a sample is produced only at the instant the analog input crosses a quantization level, thus resulting in event-driven operation [2].
Different studies have been developed with varied structures and among them an ADC that has gotten a good speed with a low consumption are the ADC with folding structures. Among them [2] developed an Asynchronous Folding ADC.
The use of the Switched Capacitor (SC) circuits applied in the Asynchronous Folding ADC designed in [2] to decrease power consumption and improve performance of the converter has been developed in [1]. In this paper it will be shown also that with this serial structure increase the number of bits is easy, enough just simply increase the number of circuit blocks. In this paper was performed in an improvement in the comparator circuits developed in [1], using the positive feedback, there was also an increase in the number of bits of the converter only with the increase of the number of stages, which is quite simple.
The main idea the switched capacitor technique consists in replacement of resistors by capacitors driven by keys while allowing the reduction of silicon area, increasing precision in the implementation of circuits and reducing power consumption.

A. Folding ADC

The general architecture of Folding ADC is shown in Figure 1. It is one of several possibilities serial or bit-per-stage architectures. It is consisted of identical cascaded stages, whose last stage is only composed of a comparator.

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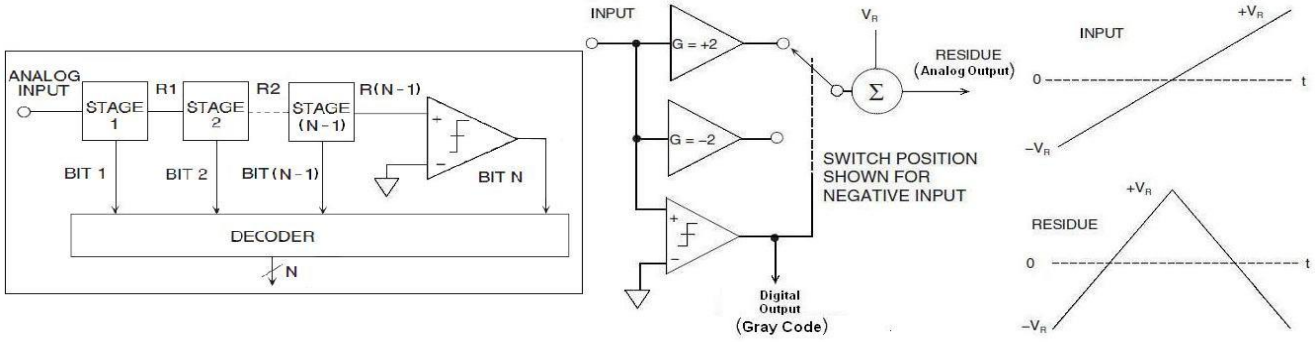

Figure 1: Block diagram and functional equivalent circuit of Folding ADC [3].

Each stage consists of one sub-ADC which is a comparator with a output for one bit, one sub-digital-analog converter (sub-DAC) of an unary output bit, in a switched topology, and a gain stage, to multiply the output signal by + 2 or - 2. This sub-ADC directly controls the sub-DAC to reconstruct the quantized analog signal. After this, the analog signal is subtracted from the quantized analog signal input stage. After subtracting the quantized signal from the analog input signal, this residue is amplified by the gain stage and then applied to the next stage [3].

The most critical point is the computation of the residue that is amplified by the gain stage and then applied to the following stage. As the proposed ADC uses irregular sampling, quantization levels are regularly disposed along the amplitude range of the signal. A sample is captured only when the analog input signal crosses one of these levels. In this moment, a voltage value is added or subtracted from the value of the analog input signal. This results in the additional requirement for the operational amplifier to maintain well defined amplitude levels when signals pass through several processing stages.

In the proposed ADC, when the analog input signal crosses the reference levels, only the derivative of the signal is inverted, reducing the additional requirement for the operational amplifier. It is similar to the bit/stage architecture based on absolute value amplifiers.

As the ADC proposed in this paper has a single benchmark to compare with the input signal, the minimum time between samples of each stage is the time taken to perform the conversion of the input signal by sub-ADC (σ_{COMP}), added to the time spent in the sub-DAC (σ_{DAC}) to reconstruct the signal that will be sent to the next stage. Therefore, since the circuit has nine stages and the full equal tenth stage has only the comparator has a cycle total delay (σ_T), which is the total time spent to convert a sample of the input signal of the ADC, which is given by:

$$\sigma_T = N * \sigma_{COMP} + (N-1) * \sigma_{DAC}$$

Thus, it can be seen that for the proposed ADC, time spent by the amplifier and comparator circuits are critical because it determines the time required to perform the conversion of a sample signal at its input. Once determined cycle total delay of the ADC, it can determine the maximum sampling rate ($f_{s,\,max}$) of the converter, which is given by:

$$f_{s,\max} = \frac{1}{\sigma_T}$$

In the same way one can proceed to determine the total power consumption (P_T) of the Folding SC ADC is the sum of the powers of each stage which is composed of a sub-ADC circuit and sub-DAC circuit, which can be determined by:

$$P_T = N * P_{subADC} + (N-1) * P_{subDAC}$$

Being, P_{subADC} is the power consumed by the sub-ADC circuit, this consists of the comparator circuit, of each stage, and P_{subDAC} is the power consumed by the sub-DAC circuit, which is composed of the amplifier circuit and the switched capacitor circuits, of each stage.

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B. Circuits and Methods

The schematic diagram of one stage is shown in Figure 2.

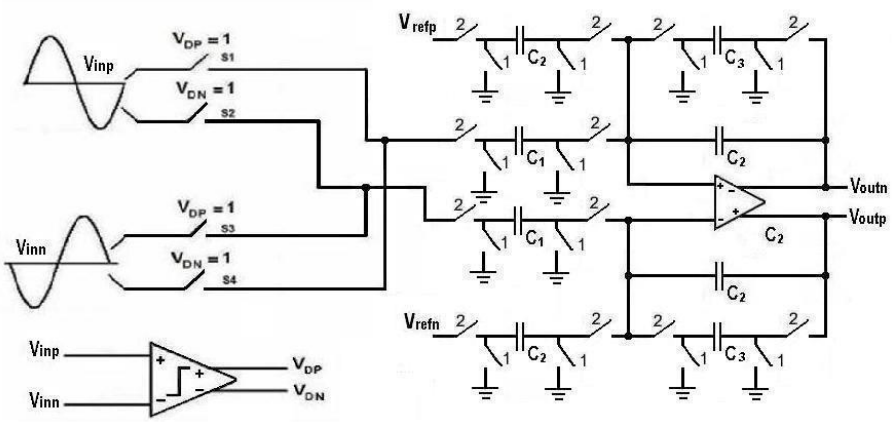

Figure 2: Schematic diagram to one stage of the folding ADC.

Making $C_2=C_3=C_1/2$, the output voltage of each stage in proposed ADC is given by:

$$V_{outp}-V_{outn}=V_{DP}(2*V_{inp}-V_{inn})*z^{-1}+V_{DN}(2*V_{inn}-V_{inp})*z^{-1}-(V_{refp}-V_{refn})*z^{-1} \quad (1)$$

This scheme has often been referred to as serial-Gray (since the output coding is in Gray code), or folding converter because the shape of the transfer function. Performing the conversion using a transfer function that produces an initial Gray code output has the advantage of minimizing discontinuities in the residue output waveforms and offers the potential of operating at much higher speeds than the binary approach.
The circuit of the proposed ADC was simulated using Design Architect of Mentor micromodels. It is shown in Figure 3, the input analog signal, the output analog signal and the output digital signal of the first and second blocks of the proposed Folding ADC. One can observes that whenever the analogue input signal crosses the reference voltage (Vref), one transition is generated in the digital output signal.

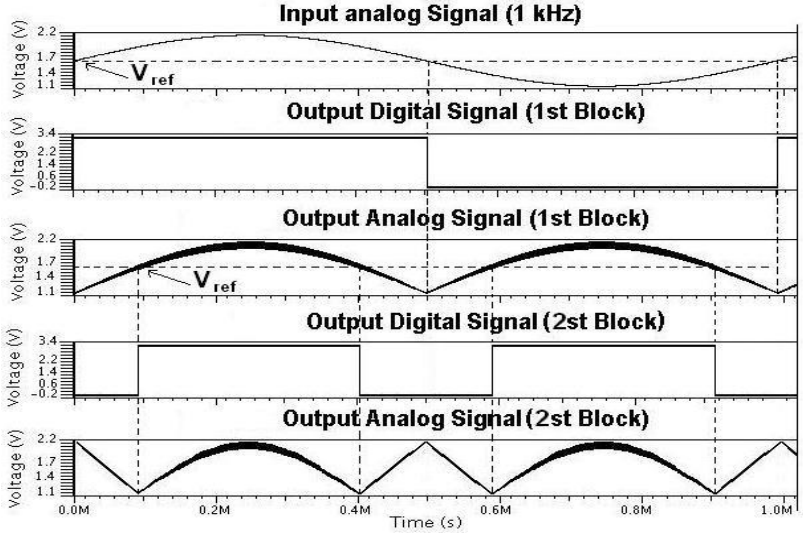

Figure 3: : 1.Input Analog Signal; 2. Output Digital Signal (1st stage); 3. Output Analog Signal (1st stage). 2. Output Digital Signal (2st stage); 3. Output Analog Signal (2st stage).

The proposed folding converter circuits was designed, implemented and simulated with CMOS standard technology of 350 nm. All used switches in this circuit were built with NMOS transistors, with reference voltages V_{refp} and V_{refn} equals to 2.15 V and 1.15 V, respectively.

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C. Building Blocks

The operational amplifier used in the design of the 1 bit/stage ADC is shown in Figure 4(a). The architecture employed is a two-stage amplifier using Miller technique for the frequency compensation. The names MN and MP denote NMOS and PMOS, respectively. The use of differential operational amplifiers brings several advantages as high rejection of power supply noise, higher output swings, etc.

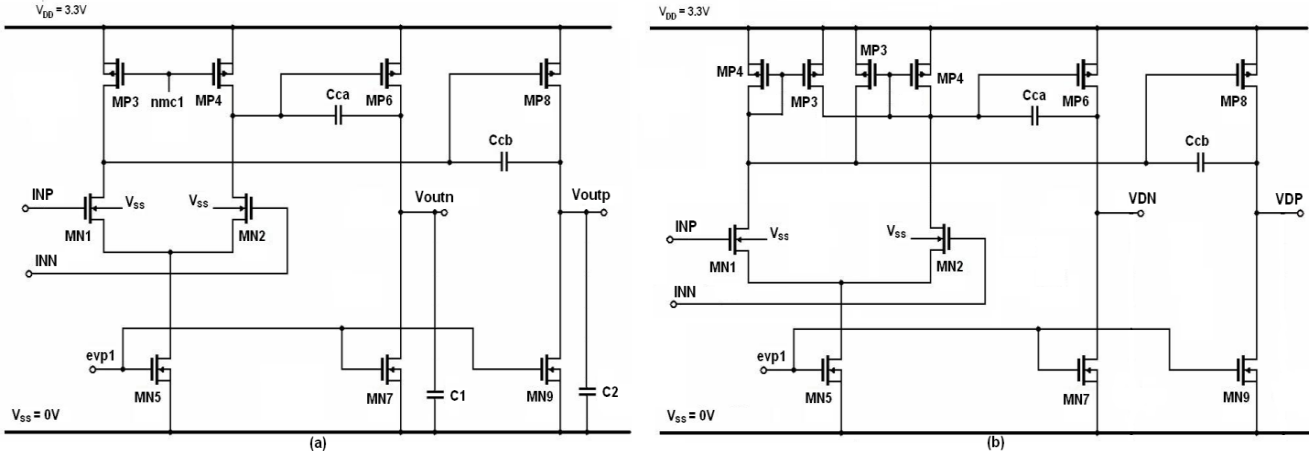

Figure 4: Schematic of: (a) an two-stage CMOS op amp with a n-channel input pair; (b) an two-stage CMOS op amp used as comparator with positive feedback.

The first stage of this operational amplifier, formed by the transistors MN1, MN2, MP3, MP4 and MN5, is a common source stage with current-source loads. The second stage of this operational amplifier is formed by the transistors MN7, MN9, MP6 and MP8. In the output stage of this operational amplifier capacitors C1 and C2 were placed to reduce noise in the output signal due to switched capacitor circuits. The transistor sizes of the operational amplifier are presented in table I and the amplifiers specifications are shown in table II.

TABLE I. DIMENSIONS OF THE OPERATIONAL AMPLIFIER'S MOSFET

Transistors	**W/L (µm/µm)**
MN1, MN2	5.53/1.0
MP3, MP4	15.90/1.0
MN5	11.37/1.0
MP6, MP8	127.73/1.0
MN7, MN9	49.46//1.0

The schematic circuit of comparator used in this project is displayed in Figure 4(b), it consists of a differential input stage of a comparator whit two paths of feedback. The first is current-series feedback through the commom-source node of transistors MN1 and MN2, this feedback path is negative. The second path is the voltage-shunt feedback through the gate-drain connections of transistors MP3, this path of feedback is positive. This positive feedback is used when you need a comparator with hysteresis due to the existence of noise in the signal to be compared. The transistor sizes of the comparator are shown in table II.

TABLE II. DIMENSIONS OF THE COMPARATOR'S MOSFET

Transistors	**W/L (µm/µm)**
MN1, MN2	50.0/1.0
MP3	10.0/1.0
MP4	10.6.1.0
MN5	12.0/1.0
MP6, MP8	64.0/1.0
MN7, MN9	25.0//1.0

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II. Simulation Result

The folding ADC presents in its digital output a Gray code, therefore to operate with standard digital-analog converters, binary input, the output code of the folding ADC must be decoded to binary.
The folding ADC proposed in this paper was designed and simulated with CMOS standard technology of 0.35 μm. All switches used in the circuit were built with NMOS transistors. The reference voltages V_{REFP} and V_{REFN} are equal to 2.15 V and 1.15 V, respectively. Figure 5 shows the FFT and SNDR of the output signal of the folding ADC for a sinusoidal input signal of 250 Hz. Table III shows the parameters obtained from the complete circuit simulation.

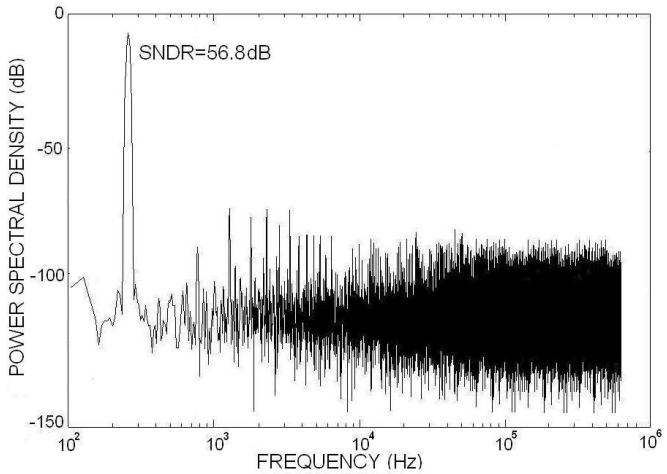

Figure 5: FFT and SNDR of output signal of the folding ADC.

By keeping the same internal structure of each stage and increasing the number of bits, the frequency of the input signal had to be reduced due to the bandwidth of the amplifiers and comparators.

TABLE III. RESULTS OF FOLDING ADC

Items	In [1]	In this paper
Input Frequency (fin)	1 kHz	250 Hz
Conversion Time	100 ns	570 ns
DC Gain (amp.)	60 dB	60 dB
GBW (amp.)	40 MHz	40 MHz
Resolution	8 bits	10 bits
Power Dissipation	5.9 mW	8 mW
ENOB	7.32 bits	9.14 bits
SNDR	45.8 dB	56.8 dB

As can be observed in Table III, in [1] applying an input signal of 1 Vpp, 1 kHz, the SNDR folding ADC reaches a maximum of 45.8 dB. With the use of positive feedback, we reduced the conversion error due to noise existing in the signal caused by the switched capacitor circuits. But it caused a greater delay in the comparator circuit which results in a longer delay to performing a conversion. Applying an input signal of 1 Vpp, 250 Hz, the SNDR 10-bit folding ADC reaches a maximum of 56.8 dB, which power dissipation is about 8 mW.
.

III. Conclusions

In this paper, was presented an 10-bit CMOS folding ADC architecture that can be used for converting low-frequency analog signals. Applying an input signal of 1 Vpp, 250 Hz, the SNDR folding ADC reaches a maximum of 56.8 dB. One of the most attractive for this converter is its low power consumption which is about 8 mW and was very simple increase the number of bits of the converter only with the increase of the number of stages.

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