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From system design to clock skew impact study in parallel sigma delta modulators using frequency band decomposition

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Abstract – This paper presents the study of a novel parallel architecture of analog-to-digital converters (ADCs) based on sigma delta (ΣΔ) modulators using frequency band decomposition (FBD). This architecture is intended for wideband applications with a fractional bandwidth equal to 40 % and composed of four channels of 6th order band-pass discrete time (DT) ΣΔ modulators with single-bit quantization. The simulation results prove that this architecture is able to provide a signal-to-noise ratio (SNR) over 50 dB. These results satisfy the wideband standard requirements. However, parallel architectures are sensitive to channel mismatches. In this paper, we are interested in studying the robustness of our FBD architecture to clock skew mismatch errors. It is shown that the clock skew causes the SNR to decrease by at most 6 dB.

Keywords: Wideband applications, parallel ADC, frequency band decomposition, band-pass ΣΔ modulators, clock skew.

I. INTRODUCTION

Oversampling analog-to-digital converters (ADCs) have been widely used in many applications because of their high accuracy with lower complexity compared to Nyquist ADCs. Sigma Delta (ΣΔ) converters have been the best candidates for audio applications since they can achieve over 16-bit resolution [1]. The main drawback is the limited bandwidth due to the noise shaping form. In fact, the bandwidth does not exceed 40 MHz and 125 MHz respectively in discrete time (DT) [2, 3] and continuous time (CT) [4, 5]. Therefore, extending these converters to broadband applications leads to parallel architectures which have come up an attractive candidate for analog-to-digital conversion that allows the increasing of the conversion band [6].

In fact, the major benefit of parallel architectures is that they ensure a high dynamic range while widening the conversion band, especially when used with ΣΔ modulators. There are three main parallel architectures [6] as the time-interleaved architecture (TIΣΔ) [7], the Hadamard modulated parallel architecture (πΣΔ) [8] and the Frequency band decomposition architecture (FBD) [9 10]. It was shown in a comparative analysis between these three classes of parallel architectures [6], that despite less implementation complexity of TIΣΔ and πΣΔ architectures, they are very sensitive to gain mismatches and offsets. Hence, this work proposes to design and test FBD architecture. Then, it deals with the clock skew impact study.

In the second section of this paper, we present the FBD architecture study and design. In the third section, an FBD architecture composed of four parallel channels based on 6th order band-pass ΣΔ modulators is proposed and modeled using SIMULINK/MATLAB. Although parallel architectures could address wideband applications, they still suffer from the problem of mismatch errors between channels. The fourth section deals with the study of the clock skew mismatch errors impact on the performances of the designed FBD architecture. Finally, the fifth section presents some conclusions and future works.

II. FREQUENCY BAND DECOMPOSITION STUDY AND DESIGN

Compared to other parallel architectures, the FBD architecture is less sensitive to channel mismatches, specially offset errors since all the modulators are band-pass (BP). Nevertheless, the challenge in this parallel architecture is its design complexity, because unlike the other architectures where the modulators are all low-pass (LP), the modulators in the FBD architecture are band-pass and tuned to the signal band of each channel. Thus, each channel of this architecture is unique with its own modulator and digital filter. Therefore, the choice is done on FBD architecture. It remains to define the number of parallel channels, the modulators orders and the required oversampling ratio (OSR) which is the sampling frequency (F_s) out of two times of the useful bandwidth (B).

From a stable k^{th} order LP ΣΔ modulator, a $(2k)^{th}$ order BP ΣΔ modulators are obtained when using the low-pass to band-pass transformation as given by (1) [11, 12] where F_c is the central frequency. Besides, we modify the parameter β while designing each band-pass modulator of the FBD architecture in a way that each modulator is tuned on its signal band of interest.

$$z^{-1} \rightarrow \frac{\beta z^{-1} - z^{-2}}{1 - \beta z^{-1}} \; where \;\; \beta = \cos(2\pi \frac{F_c}{F_s}) \tag{1}$$

When amplitude is set to $q/2$, the obtained expression of maximal SNR as a function of OSR and BP ΣΔ modulator order is given by (2) [13],

$$SNR_{max} = \frac{3(2k+1).OSR^{2k+1}}{4\pi^{2k}} \tag{2}$$

The parallel BP ΣΔ modulators are followed by a digital reconstruction stage that permits to combine the multiple ΣΔ modulators outputs to form the final reconstructed output. Two approaches have been proposed in the literature for the digital reconstruction: direct processing and digital processing with demodulation [14]. The direct processing is based on BP filters with high coefficients number whereas the digital processing with demodulation realizes the decimation in baseband. Using demodulation offers better performances with the same complexity. This is why we adopt this last approach in our proposed design for wideband applications.
The design must satisfy the wideband application requirements of a 50-dB SNR for an application with 40% fractional bandwidth, which is defined as the ratio between the receiver bandwidth and the carrier frequency [15]. Then, a 6th order BP ΣΔ modulator with an OSR of 20 per channel realizes a good compromise between the ΣΔ modulators complexity, the OSR and the number of channels in parallel. Consequently, the design leads to the proposed FBD architecture composed of 4 parallel channels of 6th order BP ΣΔ modulators. The model of this architecture, simulated in discrete-time, is presented in the next section, and simulation results will be discussed.

III. FBD ARCHITECTURE MODEL AND SIMULATION RESULTS

We adopt DT FBD architecture in order to overcome the problem of bandwidth limitation of the ΣΔ modulators. Thus, we propose an FBD architecture design to digitize a wideband application with a 40 % fractional bandwidth.

A. FBD Architecture Model

The model of the FBD architecture, designed using SIMULINK/MATLAB is presented in Figure 1. It is composed of four channels in parallel. The model is fed by a multi-tone signal (four sine-wave signals). Each sine-wave is tuned to the given channel bandwidth and each of them is composed of an anti-aliasing filter (AAF) followed by a sample and hold circuit (S&H) and a 6th order BP ΣΔ modulator.

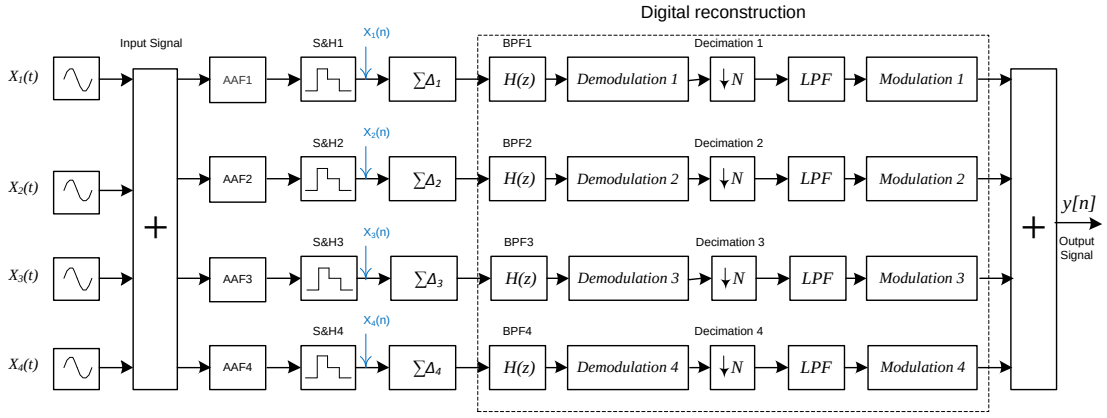

Figure 1: Proposed FBD architecture model.

The four modulators outputs are combined by a digital reconstruction block with demodulation. Each digital reconstruction stage is composed of a digital finite impulse response (FIR) BP filter that is tuned to the given channel bandwidth, a demodulation block that allows the frequency down-conversion to baseband, a baseband decimation filter followed by a low-

pass filter (LPF) that removes the out-of-band noise and a modulation block that performs frequency up-conversion to bring the signal to its initial band of interest. Finally, the parallel outputs are combined to form the output signal. Simulation results are discussed in the next subsection.

B. Simulation Results

A multi-tone signal composed of four sine-wave signals with a 0.6 V amplitude is applied at the input of the designed FBD architecture. Each sine-wave frequency is fixed at the central frequency of the associated channel bandwidth. The output spectrum is presented in Figure 2. Performances in terms of SNR, spurious free dynamic range (SFDR) and effective number of bits are estimated by means of spectral analysis applied to each modulator and to the whole FBD architecture. All these performance parameters are summarized in the Table 1. The obtained SNR of the reconstructed output signal reaches 50.1 dB which is needed for the chosen wideband application. These results are obtained with an FBD architecture without mismatch errors [6]. In fact, one of mismatch errors is the clock skew mismatch errors whose impact is studied in the next section.

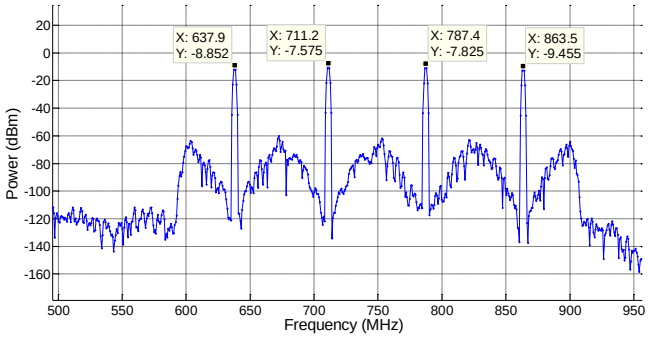

Figure 2: Output signal spectrum of the FBD architecture model without errors.

Table 1: Performances without errors at each ΣΔ output and at the output of the FBD architecture.

	SNR(dB)	SFDR (dB)	Resolution (bits)
ΣΔ1 output	47	56.5	7.5
ΣΔ2 output	51.2	58.8	8.3
ΣΔ3 output	47.8	56.4	7.8
ΣΔ4 output	46.5	54.9	7.2
Total output	50.1	59.4	8

IV. CLOCK SKEW IMPACT IN FBD ARCHITECTURE

We are interested in this section in studying the sensitivity of the designed architecture to the clock skew mismatch errors. The FBD architecture model considering this mismatch is studied and then tested to discuss the clock skew impact on the FBD architecture.

A. Clock skew model

Clock skew errors sequence of $\{\Delta_{t1}, \Delta_{t2}, \Delta_{t3}, \Delta_{t4}\}$ is applied at the input of the four channels of the FBD architecture as shown in Figure 3.

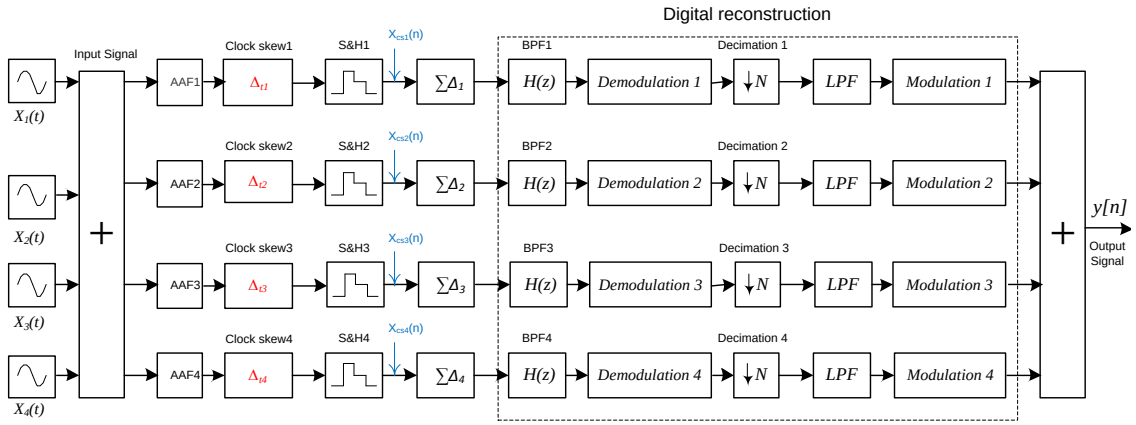

Figure 3: Proposed FBD architecture model with clock skew mismatch errors.

The impact of clock skew mismatch errors on the performances of the reconstructed output signal is analyzed. The signals at the input of the ΣΔ modulators before and after clock skew errors mismatch insertion are expressed respectively by (3) and (4).

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$$\begin{aligned} x_1(n) &= \sin(2\pi f_{in1} nT_s) \\ x_2(n) &= \sin(2\pi f_{in2} nT_s) \\ x_3(n) &= \sin(2\pi f_{in3} nT_s) \\ x_4(n) &= \sin(2\pi f_{in4} nT_s) \end{aligned} \quad (3)$$

$$\begin{aligned} x_{cs1}(n) &= \sin(2\pi f_{in1}(nT_s + \Delta_{t1})) \\ x_{cs2}(n) &= \sin(2\pi f_{in2}(nT_s + \Delta_{t2})) \\ x_{cs3}(n) &= \sin(2\pi f_{in3}(nT_s + \Delta_{t3})) \\ x_{cs4}(n) &= \sin(2\pi f_{in4}(nT_s + \Delta_{t4})) \end{aligned} \quad (4)$$

Equation (4) becomes (5) when using trigonometric formulas

$$\begin{aligned} x_{cs1}(n) &= sin(2\pi f_{in1} nT_s).\ \cos(2\pi f_{in1}\Delta_{t1}) + \cos(2\pi f_{in1} nT_s).\ \sin(2\pi f_{in1}\Delta_{t1}) \\ x_{cs2}(n) &= sin(2\pi f_{in2} nT_s).\ \cos(2\pi f_{in2}\Delta_{t2}) + \cos(2\pi f_{in2} nT_s).\ \sin(2\pi f_{in2}\Delta_{t2}) \\ x_{cs3}(n) &= sin(2\pi f_{in3} nT_s).\ \cos(2\pi f_{in3}\Delta_{t3}) + \cos(2\pi f_{in3} nT_s).\ \sin(2\pi f_{in3}\Delta_{t3}) \\ x_{cs4}(n) &= sin(2\pi f_{in4} nT_s).\ \cos(2\pi f_{in4}\Delta_{t4}) + \cos(2\pi f_{in4} nT_s).\ \sin(2\pi f_{in4}\Delta_{t4}) \end{aligned} \quad (5)$$

Considering low value for the clock skew errors (<0.1/F_s), the signal at the input of each channel could be expressed as given by (6):

$$\begin{aligned} x_{cs1}(n) &\approx \sin(2\pi f_{in1} nT_s) + 2\pi f_{in1}\Delta_{t1}.\cos(2\pi f_{in1} nT_s) \\ x_{cs2}(n) &\approx \sin(2\pi f_{in2} nT_s) + 2\pi f_{in2}\Delta_{t2}.\cos(2\pi f_{in2} nT_s) \\ x_{cs3}(n) &\approx \sin(2\pi f_{in3} nT_s) + 2\pi f_{in3}\Delta_{t3}.\cos(2\pi f_{in3} nT_s) \\ x_{cs4}(n) &\approx \sin(2\pi f_{in4} nT_s) + 2\pi f_{in4}\Delta_{t4}.\cos(2\pi f_{in4} nT_s) \end{aligned} \quad (6)$$

Taking into account ideal ΣΔ modulators plus perfect reconstruction signal, the output signal is expressed as given by (7):

$$\begin{aligned} y_{cs}(n) = {} & sin(2\pi f_{in1} nT_s).\cos(2\pi f_{in1}\Delta_{t1}) + \cos(2\pi f_{in1} nT_s).sin(2\pi f_{in1}\Delta_{t1}) \\ & + sin(2\pi f_{in2} nT_s).\cos(2\pi f_{in2}\Delta_{t2}) + \cos(2\pi f_{in2} nT_s).\sin(2\pi f_{in2}\Delta_{t2}) \\ & + sin(2\pi f_{in3} nT_s).\cos(2\pi f_{in3}\Delta_{t3}) + \cos(2\pi f_{in3} nT_s).\sin(2\pi f_{in3}\Delta_{t3}) \\ & + sin(2\pi f_{in4} nT_s).\cos(2\pi f_{in4}\Delta_{t4}) + \cos(2\pi f_{in4} nT_s).\sin(2\pi f_{in4}\Delta_{t4}) \end{aligned} \quad (7)$$

The expression (7) below contains in addition of the original signal, terms in quadrature proportional to the clock skew errors. These terms, when added at the output, result in the attenuation of the power level of the input signal replicas. The next section deals with simulation results in case of clock skew mismatch errors in the next subsection.

B. Simulation results and performances

The impact of the clock skew errors on the power level of the four sine-wave signals is studied. Generally, clock skew error is lower than 1/F_s [16]. A clock skew errors sequence of {0.8/F_s, 0.7/F_s, 0.9/F_s, 0.6/F_s}, which seems to present the worst degradation, is applied to the signals before S&H circuits in the FBD architecture. The output signal spectrum of the architecture model, presented in Figure 4, shows an attenuation of the signal comparing to the ideal case presented in Figure 2. This attenuation results in the degradation of the output signal's SNR which decreases from 50.1 dB to 44.3 dB. Performances in terms of SNR, SFDR and effective number of bits for each modulator and at the total output after adding clock skew mismatch errors are summarized in Table 2. There is a degradation of at most 3 dB at the output of the modulators. Nevertheless, the attenuation of the signal peaks caused by the clock skew mismatch errors, as shown by Figure 4, appears after channel reconstruction, where terms proportional to the clock skew delays and in quadrature with the original output signal are added, as in (6) and (8), causing the attenuation.

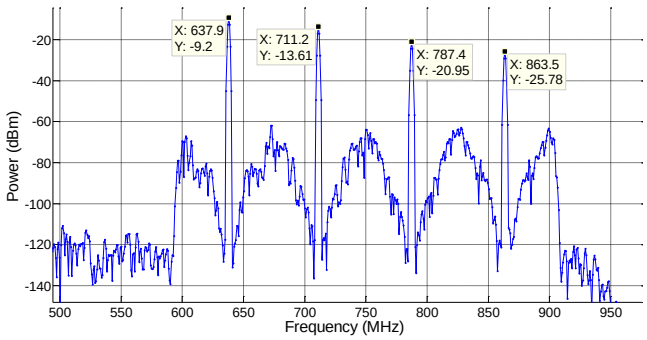

Figure 4: Output signal spectrum of the FBD architecture model with clock skew mismatch errors.

Table 2: Performances at each ΣΔ output and at the output of the FBD architecture with clock skew mismatch errors.

	SNR (dB)	SFDR (dB)	Resolution (bits)
ΣΔ1 output	50	59.3	8
ΣΔ2 output	48.4	59.6	7.7
ΣΔ3 output	47.5	57.8	7.6
ΣΔ4 output	47.4	57.7	7.6
Total output	44.3	57.4	7.1

The second step of this study is to vary the values of clock skew mismatch errors. We take back the {0.8/F_s, 0.7/F_s, 0.9/F_s, 0.6/F_s} clock skew sequence applied previously. However, we modify the values of the clock skews applied in channels 2 and 3, Δ_{t2} and Δ_{t3}, which become assigned to a set of values in [0, 1/F_s] with a step of 0.1/F_s. The study of the peak power level of the reconstructed output signal according to Δ_{t2} and Δ_{t3} when input signals are situated at frequencies different from the channels central frequencies, is presented in Figure 5. It is shown that the peaks power levels degradation is still at low levels, between -12.5 dBm and -14 dBm, compared to the level peaks degradation shown in Figure 4. Simulation results proved that the attenuation caused by clock skew mismatch errors does not exceed 6 dB if the input signal frequencies are different from the central frequencies of the channels bandwidths. Otherwise, the attenuation becomes at high levels and could exceed 15 dB as shown by Figure 6 when the input frequencies are at the channels central frequencies, which corresponds to the spectrum presented in Figure 4. These attenuations is related to the modulation and demodulation operations of the reconstruction stage that mixes ΣΔ modulators outputs with sine waves at the channels central frequencies.
Thus, we note that the demodulation and the modulation blocks increase this degradation when the input frequencies are tuned to the channels central frequencies. This explains the more than 15-dB degradation of power level peaks at the frequencies f_{in4} in Figure 4 and f_{in2} in Figure 6.

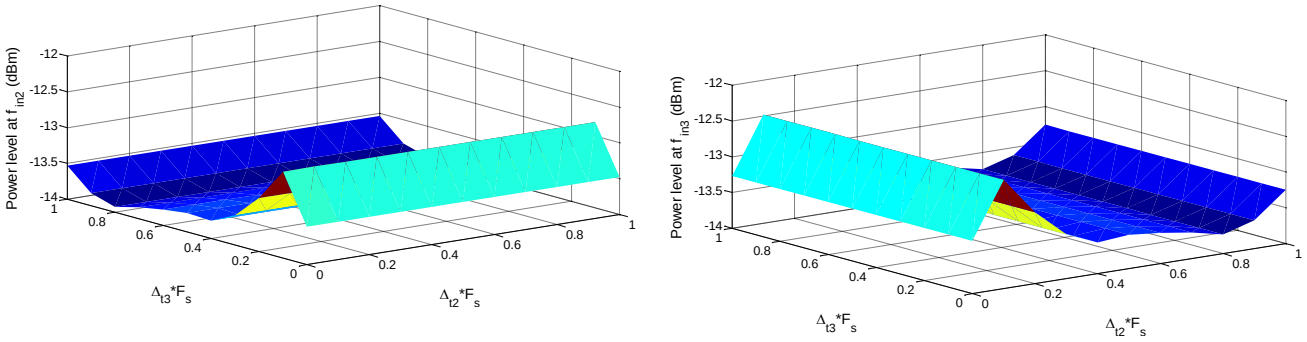

Figure 5: Power level degradation at f_{in2} and f_{in3}, different from central frequencies, for the reconstructed output according to variation of Δ_{t2} and Δ_{t3} in [0, 1/Fs].

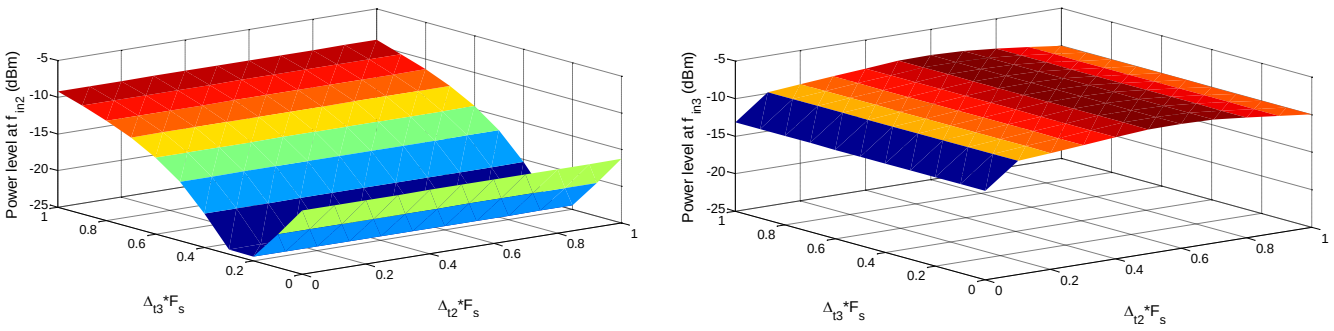

Figure 6: Power level degradation at f_{in2} and f_{in3}, centered at channels central frequencies, for the reconstructed output according to variation of Δ_{t2} and Δ_{t3} in [0, 1/Fs].

V. CONCLUSION

An FBD architecture model based on 6th order BP ΣΔ modulators has been proposed. The FBD architecture allows the digitization of a wideband band-pass application with a fractional bandwidth of 40 %. It uses an optimized number of channels equal to four. This architecture reaches an SNR over 50 dB as required by wideband applications. The study of the impact of the clock skew mismatch error between the different channels shows a low attenuation relative to the STF unless in the case where the input frequencies are centered at the central frequencies. If the channels central frequencies are chosen, the attenuation causes SNR degradation that exceeds 15 dB for a particular clock skew mismatch errors sequence. This attenuation is caused by the modulation and demodulation operations of the reconstruction block. A correction method of this mismatch error should be integrated to the digital processing stage of the designed FBD architecture.

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