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The Matlab Toolbox for Simulation Analysis and Design Support of New Adaptive Sub-ranging A/D Converters

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Abstract- The paper presents the toolbox for simulation analysis and support of the high-level design of new adaptive sub-ranging analog-to-digital (A/D) converters whose digital parts allow the iterative calculation of output codes using digital estimation algorithms. The developed appropriate methods and simulation tools enable the assessment of the converters characteristics taking into consideration many different non-idealities (e.g. offsets, noises, non-linearities, gain mismatches) of the internal components of ADCs. The simulation analysis can support the proper choice of the suitable converter configuration and tuning of parameters of the conversion algorithm, which enables to achieve the best characteristics of the converters under assumed level of errors of the components. The toolbox can be used at initial stages of design of the adaptive sub-ranging A/D converters to preliminary evaluation of the expected performance and its comparison with the performance of the existing comparable sub-ranging A/D converters.

I. Introduction

As in many domains of contemporary engineering and science, simulation methods of A/D converters (ADCs) analysis are widely used especially in investigations on new architectures or in initial phases of the converters design, see e.g. [1-2]. The simulation research on the behavioural models of ADCs and their internal components support specification of the most appropriate and sufficient requirements on basic parameters of the converters components and can significantly speed up the design process of ADCs. This paper completes, in this aspect, the paper [3] which presents the fundamentals of the new effective architectures and conversion algorithms for adaptive sub-ranging ADCs. These converters (in previous papers called also intelligent cyclic (recursive) or pipeline ADCs [4-5]) employ the original A/D conversion method based on application of the analytical approach, presented in [6], to optimization of adaptive estimation systems working in conditions of the limited input ranges of their components, as in all real devices. The approach permits to determine analytically the most efficient values of the adaptive sub-ranging ADCs parameters which guarantee maximal performance of conversion under given permissible probability of internal saturations. The appropriately selected values of gains of the inter-stage amplifiers and the corresponding algorithm of output codes calculation enable reaching the overall parameters (e.g. effective numbers of bits – ENOB) of the adaptive sub-ranging ADCs better than in the conventional sub-ranging ADCs with the same analog components [3]. The approach presented in [3] extends earlier ideas eliminating main disadvantages of the previous architectures of the adaptive sub-ranging ADCs [4-5], i.e. high-resolution of internal D/A sub-converters and very large values of internal amplifiers gains in the last cycles/stages of conversion. To confirm and assess the benefits of modifications proposed in [3], the specialized MATLAB toolbox for simulation analysis and support of the high-level design of the new adaptive sub-ranging ADCs was developed. The toolbox includes the simulation models of all basic internal components of the adaptive sub-ranging ADCs taking into account their errors, noises, offsets, non-linearities, as well as the models of the whole converters with their digital parts.

II. Fundamentals of adaptive sub-ranging A/D converters operation

The block diagrams of the considered recursive (recirculating [7], cyclic) and pipeline adaptive sub-ranging ADCs are presented in Fig. 1a and 1b, respectively. The converters consist of the following crucial components: sample-and-hold circuits (S/H), internal sub-ADCs ($SADC_k$), internal sub-DACs ($SDAC_k$), amplifiers (C_k) and digital parts.

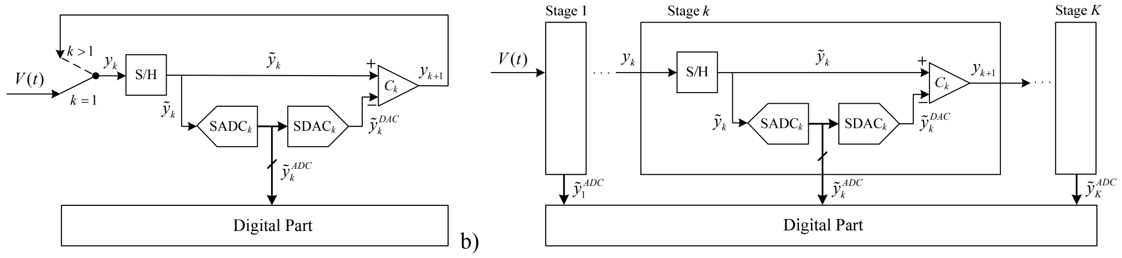

Figure 1. Block diagrams of modified adaptive recursive (a) and pipeline (b) A/D converters.

Every *k*-th ($k=1,2,...,K$) cycle/stage performs sample and hold (S/H) operation on the analog input signal y_k and produces the $N_{ADC,k}$-bit digital output $\tilde{y}_k^{ADC}$ and the residual signal $y_{k+1}=C_k(\tilde{y}_k-\tilde{y}_k^{DAC})+v_k^{AMP}$ which is routed to the input of the next (*k*+1)-th cycle/stage. In the first cycle/stage, the input signal of S/H circuit $y_1=V(nT)=V$ is a signal being converted and the last *K*-th cycle/stage produces only the digital output. v_k^{AMP} denotes an output noise of the inter-stage amplifier with the gain value C_k . The output signal of S/H circuit $\tilde{y}_k=y_k+v_k^{S/H}$, where $v_k^{S/H}$ denotes an output noise or error of S/H circuit, is quantized by the fast A/D sub-converter (SADC$_k$). The mid-riser form of a quantizer is assumed [3]. The digital word $\tilde{y}_k^{ADC}$ produced by SADC$_k$ drives the internal D/A sub-converter (SDAC$_k$) which forms the analog quantized version $\tilde{y}_k^{DAC}$ of the input signal of SADC$_k$ $\tilde{y}_k$. The model of the analog signal $\tilde{y}_k^{DAC}$ at the output of SDAC$_k$, which takes explicitly into account the limited input range $[-D,D]$ of SADC$_k$, is as follows:

$$\tilde{y}_k^{DAC}=\begin{Bmatrix} \tilde{y}_k & \text{for} & |\tilde{y}_k|\le D \\ D\ \text{sign}(\tilde{y}_k) & \text{for} & |\tilde{y}_k|>D \end{Bmatrix} + \xi_k^{ADC}+v_k^{DAC}\,, \tag{1}$$

where ξ_k^{ADC} is a quantization error (noise) and v_k^{DAC} denotes an analog error/noise at the output of SDAC$_k$. The digital part of the adaptive sub-ranging ADC computes the estimates (output codes) $\hat{V}_k$ of the input samples V on the basis of sub-codes $\tilde{y}_k^{ADC}$ delivered by SADC$_k$ from the subsequent cycles/stages according to the following relationship [3]:

$$\hat{V}_k=\hat{V}_{k-1}+L_k\tilde{y}_k^{ADC}=\sum_{i=1}^{k}L_i\tilde{y}_i^{ADC}\,, \tag{2}$$

where L_k are the values of digital coefficients used for calculation of the output codes and are directly related to the values of the inter-stage gains C_k . To obtain the most accurate estimates (codes) of the input samples, the values of the gains C_k in particular cycles/stages should be as large as possible to amplify the analog residual signals $e_k=\tilde{y}_k-\tilde{y}_k^{DAC}$ in such a way that the whole range of SADC$_{k+1}$ in the next stage will be used. The values of gains C_k and the corresponding values of the digital coefficients L_k should satisfy the condition guaranteeing no saturation of SADC$_k$:

$$|\tilde{y}_k|\le D\,. \tag{3}$$

For the following assumptions:

- analog errors/noises v_{k-1}^{DAC} at the output of SDAC$_{k-1}$ are within the range $[-\Delta_{k-1}^{DAC},\Delta_{k-1}^{DAC}]$, where the level Δ_{k-1}^{DAC} of maximal errors is related to the technology and circuit solutions employed in ADC,
- analog errors/noises v_{k-1}^{AMP} at the output of the amplifier are within the range $[-\Delta_{k-1}^{AMP},\Delta_{k-1}^{AMP}]$,
- analog errors/noises $v_k^{S/H}$ at the output of S/H circuit are within the range $[-\Delta_k^{S/H},\Delta_k^{S/H}]$,
- quantization errors ξ_{k-1}^{ADC} are within the interval $[-Q_{k-1}/2,Q_{k-1}/2]$, where Q_{k-1} is a quantization step of SADC$_{k-1}$,
- gain setting errors have the form $C_{k-1}^{err}=C_{k-1}(1+\gamma_{k-1}^{C})$ and the relative gain errors γ_{k-1}^{C} are within the range $[-\delta_{k-1}^{C},\delta_{k-1}^{C}]$, then C_{k-1}^{err} are within the range $[C_{k-1}(1-\delta_{k-1}^{C}),C_{k-1}(1+\delta_{k-1}^{C})]$,

the optimal (maximal) values of C_{k-1} and L_k guaranteeing no saturation in the subsequent cycles/stages are determined by the following relationships [3]:

$$C_{k-1}=\frac{D-(\Delta_{k-1}^{AMP}+\Delta_k^{S/H})}{(Q_{k-1}/2+\Delta_{k-1}^{DAC})(1+\delta_{k-1}^{C})}\,, \tag{4}$$

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$$L_k = \prod_{i=1}^{k-1} C_i^{-1} = \frac{L_{k-1}}{C_{k-1}}, \qquad L_1 = 1\,. \tag{5}$$

In conventional sub-ranging ADCs [7,8], the inter-stage gains C_k have values equal to the integer powers of two $C_k = 2^{N_{ADC,k}-m_k}$, where $N_{ADC,k}$ is the number of bits of SADC$_k$, and m_k is the number of redundant bits used for digital correction of the errors caused by noises and distortions in analog components of sub-ranging ADCs, among others by imperfect inter-stage gains which exceed $2^{N_{ADC,k}}$ (in case of non-redundant stages) and cause saturations in the next cycles/stages. Commonly, one bit of redundancy is used ($m_k = 1$). The values of the inter-stage gains $C_k = 2^{N_{ADC,k}-m_k}$ are smaller than the values theoretically sufficient for elimination of the saturation, determined by (4), and the converter components are utilized incompletely and the conventional sub-ranging ADCs are capable to achieve the worse values of overall parameters (e.g. ENOB) for the same parameters of internal components, than the proposed converters employing digital algorithms. The cost of employing the proposed method of A/D conversion is connected with the extension of the digital part of the sub-ranging ADCs, but the calculations determined by (2) are not very complicated.

III. Modelling of adaptive sub-ranging A/D converters and their components

To simulate and verify all aspects of operation of the proposed adaptive sub-ranging A/D converters the specialized MATLAB toolbox was developed. The toolbox enables to perform the simulation experiments concerning both details of ADCs operation and influence of particular parameters of their components on the parameters and characteristics of the whole ADCs. The toolbox allows also to compare the results (parameters and characteristics) obtained for the modified adaptive sub-ranging A/D converters with the results obtained for the simulation models of existing conventional sub-ranging ADCs (e.g. AD9467, AD9240, AD678, AD779, MAX1205) as well as with the results obtained for the earlier "standard" versions of adaptive sub-ranging ADCs [4-5]. The toolbox is a set of about 40 m-functions and can be used as an interactive tool which enables the choice of the type of experiment and introducing the parameters of the simulated converter and its components. The toolbox consists of the following groups of functions for:

- control of experiments of the particular types: a single experiment for the given set of converter parameters, an experiment with changing parameters, comparison of converters,
- design of the converter being investigated: introducing parameters of the converter and its components and definition of their models (with the considered errors) used in the simulation experiment,
- generation of test signals of different types: sinusoidal, ramp, random uniformly or normally distributed,
- simulation of signal processing by the particular cycles/stages and the digital part of ADC,
- processing of output data, calculations of converters parameters and characteristics such as SINAD, ENOB, INL, DNL, THD, FFT of output signals, and their visualization.

To simulate the non-idealities of the internal components of the adaptive sub-ranging ADCs, the mathematical models of all crucial converters components were developed and implemented in m-functions, i.e. the models of the following components:

- S/H circuits - taking into account their input offsets and output voltage distortions or noises. S/H circuits are modelled as amplifiers with the gain equal to unity and the given value of input offset voltage. Output errors or noises of S/H circuits are simulated as random changes of their output voltages distributed uniformly within the defined interval $[-\Delta_k^{S/H}, \Delta_k^{S/H}]$.
- Sub-ADCs - taking into account their offsets, gain errors, differential (DNL) and integral (INL) non-linearities. Sub-ADCs are modelled as the sets of transition levels (quantization thresholds) which are created at the stage of the sub-ranging ADC design (definition). Offsets are simulated as shifting of the transition levels by the given value, and gain errors as changes of the slope of the sub-ADCs transfer function. DNL errors are simulated as displacements of the transition levels around nominal values uniformly distributed in the interval $[-\varepsilon_k^{ADC} \cdot Q_k/2, \varepsilon_k^{ADC} \cdot Q_k/2]$, where Q_k is the quantization step (code bin) in the k-th cycle/stage and ε_k^{ADC} determines the level of DNL errors. INL errors are simulated as changes of the thresholds according to the following relationship:

$$T_i^{INL} = D\,\mathrm{sgn}(T_i)\left(\frac{|T_i|}{D}\right)^{1+\lambda_k^{ADC}}, \tag{6}$$

  where T_i are the nominal values of the transition levels, T_i^{INL} are the values of the transition levels with INL errors, and λ_k^{ADC} determines the level of INL distortions of the sub-ADC transfer function.

- Sub-DACs - taking into account their offsets, gain errors, differential (DNL) and integral (INL) non-linearities, and output errors or noises. Sub-DACs are modelled as the sets of the output voltages corresponding to the digital input codes. Similarly as for sub-ADCs, these sets of the output voltages are created at the stage of the sub-ranging ADC definition and their errors are simulated as displacements of the output voltages. Offsets are simulated as shifting of the output voltages by the given value, and gain errors as changes of the slope of the sub-DACs transfer function. DNL errors are simulated as the displacements of the output voltages around their nominal values uniformly distributed in the interval $[-\varepsilon_k^{DAC} \cdot Q_k/2, \varepsilon_k^{DAC} \cdot Q_k/2]$, where Q_k is the quantization step in the *k*-th cycle/stage and ε_k^{DAC} determines the level of DNL errors. INL errors of sub-DACs are simulated as changes of their output voltages analogically as changes of the transition levels in case of sub-ADCs, but with parameter λ_k^{DAC} determining the level of INL errors similarly as λ_k^{ADC} in (6). Additional output errors/noises of sub-DACs are simulated as random changes of their output voltages distributed uniformly within $[-\Delta_k^{DAC}, \Delta_k^{DAC}]$.
- Inter-stage amplifiers - taking into account their input offsets, gain errors, common mode errors and output errors or noises. Inter-stage amplifiers are modelled as linear amplification blocks with two (negative and positive) inputs and the given values of the gains C_k. Gain errors are simulated as the changes of the nominal values of the gains C_k to the values $C_k^{err} = C_k(1+\gamma_k^C)$, where the relative gain errors γ_k^C are uniformly distributed in the interval $[-\delta_k^C, \delta_k^C]$. Common mode errors are simulated as the difference between the gains of two inputs of the amplifier. Additional output errors/noises of amplifiers are simulated as random changes of their output voltages distributed uniformly within the given range $[-\Delta_k^{AMP}, \Delta_k^{AMP}]$.
- Digital parts of ADCs - taking into account the algorithm of output codes calculation and the limited length of the binary words used for output codes calculation.

The toolbox enables simulation investigations on influence of individual or jointly appearing non-idealities, mentioned above, on the total ADCs parameters or characteristics.

IV. Selected results of simulation experiments

Below, some selected results of simulation experiments are presented to illustrate the capabilities of the developed toolbox. The first experiment is devoted to usage of the toolbox for analysis of the attainable ENOB of the modified recursive sub-ranging ADC for the given parameters of the internal sub-ADC (SADC$_k$). An exemplary transfer function of the internal sub-ADC (SADC$_k$) which can be defined in the toolbox (e.g. on the basis of measurements of converter components), is presented in Fig. 2a (blue line). In this case, the resolution of sub-ADC is 3 bits, its offset is 0.001 [V], and the gain error is 0.02. Additionally, there are DNL errors modelled as independent random displacements of each quantization threshold. The displacements were uniformly distributed around nominal values of the thresholds in the interval $[-\varepsilon_k^{ADC} \cdot Q_k/2, \varepsilon_k^{ADC} \cdot Q_k/2]$, where Q_k is the quantization step and ε_k^{ADC} determines the level of DNL errors. In the considered case, $\varepsilon_k^{ADC} = 0.02$ was assumed. Fig. 2b presents ENOB as a function of the cycles/stages number for the recursive sub-ranging ADCs employing SADC$_k$ with the transfer function from Fig. 2a. Both figures include also plots for the ideal SADC$_k$ without errors. The empirical values of ENOB achieved after *k* stages were calculated according to the definition given in [9]:

$$ENOB_k = \log_2\left(\frac{FSR}{NAD_k \cdot \sqrt{12}}\right), \qquad NAD_k = \sqrt{\frac{1}{M}\sum_{m=1}^{M}\left[\hat{V}_k^{(m)} - V^{(m)}\right]^2}, \tag{7}$$

where $FSR = 2$ V is the full-scale range of the converter and NAD_k is the root-mean-square value of noise and distortion. The empirical values of ENOB were calculated on the basis of results of conversion of signal samples $V^{(m)}$ $(m = 1, ..., M)$, uniformly distributed in the input range of the converter, where $M = 100000$ is the number of samples converted in the given experiment.

The results presented in Fig. 2b show how ENOB changes after subsequent cycle/stages and indicate the upper limit for ENOB achievable for this set of the converter parameters as well as the number of cycles needed to achieve this limit. It is worth noticing that the conversion algorithm described by (2), (4), (5) and used in this experiment did not take into account the simulated errors of sub-ADC. We can conclude that the sufficient and necessary number of cycles to achieve about 9 bits of ENOB is four and the further increase of the number of cycles does not increase significantly ENOB of the converter with the assumed set of parameters. In the similar experiments, one can investigate the converter performance attainable for other sets of parameters of the components errors or noises as well as the effectiveness of new methods and algorithms developed for reduction of influence of these errors or noises on the total performance of the converter.

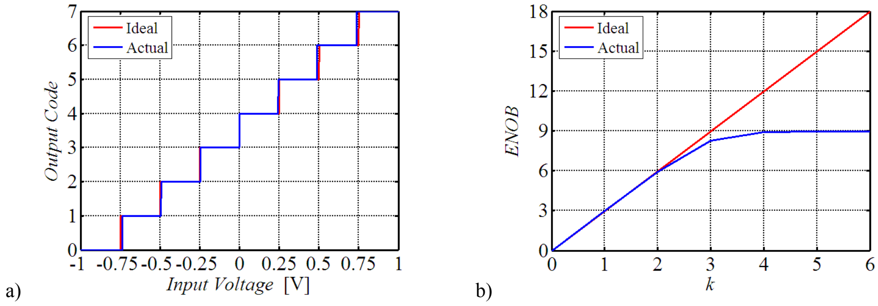

Figure 2. Exemplary transfer function of 3-bit sub-ADC (a) and ENOB vs. cycles number (b) for adaptive recursive sub-ranging ADC employing this sub-ADC.

In the next simulation experiment, influence of the level of gains errors in pipeline sub-ranging ADCs on the ENOB was considered. The experiment was performed for both the adaptive sub-ranging ADCs with the modified algorithm determined by (2), (4), (5) and for the corresponding (with the same resolutions of sub-converters and gain errors) conventional pipeline ADC with one bit of redundancy in each stage [7,8] (see also [3]). The following parameters was assumed in the experiment $FSR = 2$ V , $N_{ADC,k} = 4$ for $k = 1,2,....,8$. The gain errors were simulated as erroneous settings of the actual gains $C_k^{err} = C_k(1+\gamma_k^C)$ where C_k are the nominal values of gains and the relative gain errors γ_k^C are uniformly distributed in the interval $[-\delta_k^C, \delta_k^C]$, while the values of gains assumed for calculations of the digital coefficients L_k according to (5) were equal to the nominal values C_k . It was assumed that the remaining errors/noises of the converters components do not occur. Fig. 3 shows ENOB (7) as a function of the number of stages obtained for the conventional pipeline ADC (Fig. 3a) and for the adaptive pipeline ADC (Fig. 3b) under different values of $\delta_k^C = 0, 10^{-6}, 10^{-5}, 10^{-4}, 10^{-3}, 10^{-2}$. The results indicate the advantage of the adaptive pipeline ADC which achieves faster growth of ENOB for all values of δ_k^C. The adaptive pipeline ADC achieves the upper limits of ENOBs about one cycle earlier than the conventional pipeline ADC. On the other hand, the analysis of the results of simulations enables formulation of requirements for the gain errors necessary to achieve the given level of ENOB employing the given number of stages. Similar analyses can be performed for other parameters of the converter components under the certain values of the remaining converter parameters.

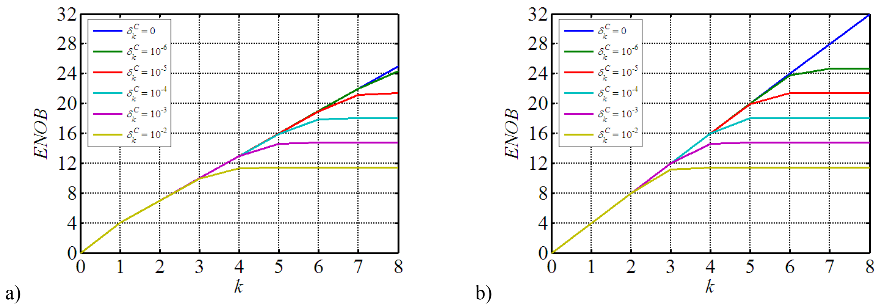

Figure 3. ENOB achieved after *k* stages for conventional pipeline ADC (a) and corresponding adaptive pipeline ADC (b) for different values of maximal gain errors γ_k^C .

The next experiment is devoted to the simulation assessment of the minimal number of bits N_{comp} used for the output codes calculation in the digital part of the adaptive sub-ranging ADC employing the modified algorithm (2), (4), (5) sufficient to obtain the achievable ENOB for the given parameters of the converter components. As an example, the same configuration of the adaptive sub-ranging ADC as used in the existing pipeline ADC AD9467 [10] was selected. AD9467 consists of seven stages with the following numbers of bits in the subsequent ($k = 1,2,....,7$) stages: $N_{ADC,k} = 3,4,3,3,3,3,3$, and one bit of redundancy in each stage [10]. Some results of comparison analysis of AD9467 and the adaptive sub-ranging ADC were presented in [3] where the advantages of the adaptive sub-ranging ADC over AD9467 were shown. In the experiment, which results are presented below, the assumed number of bits in the digital part was $N_{comp} = 24$. In the experiment, which results are presented in Fig. 4, we investigated the influence of the number of bits N_{comp} on the ENOB of the adaptive sub-ranging ADC. We considered two sets of parameters corresponding to results presented in [3], i.e. that the level of maximal output errors or noises of S/H circuits, sub-DACs and inter-stage amplifiers in each stage (for $k = 1, 2, \ldots, 7$) is the same $\Delta_k^{S/H} = \Delta_k^{DAC} = \Delta_k^{AMP}$ and is equal to $50\ \mu\text{V}$ (Fig. 4a) or $100\ \mu\text{V}$ (Fig. 4b).

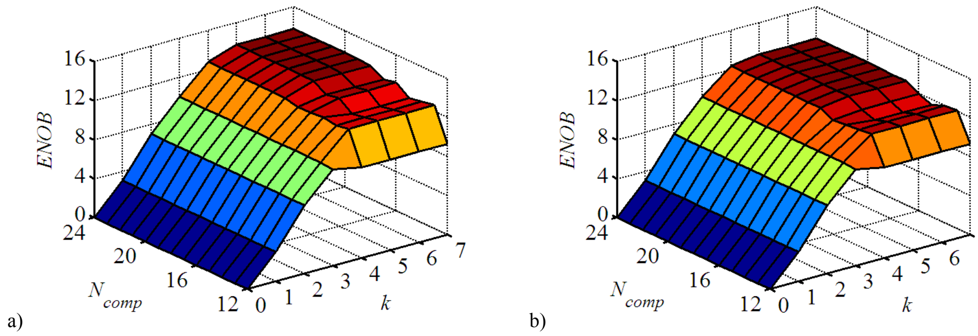

Figure 4. ENOB achieved after *k* stages for adaptive sub-ranging ADC for different number of bits N_{comp} and for the level of maximal analog errors or noises: (a) $50\ \mu\text{V}$, (b) $100\ \mu\text{V}$.

The results presented in Fig. 4 show that the sufficient number of bits used for the output codes calculation in the digital part of the adaptive sub-ranging ADC is 18 in the first case (Fig. 4a) and 16 in the second case (Fig. 4b). Application of the greater numbers of bits, which means application of more complex digital circuits, are not justified for the given parameters of errors or noises of the components. Analogous experiments enable the assessment of the values of different parameters of ADCs and their sets which are sufficient to obtain the expected values of the overall parameters of the sub-ranging ADCs.

V. Conclusions

The developed Matlab toolbox enables efficient and versatile analysis of particularities of the adaptive sub-ranging ADCs operation as well as quantitative assessment of the expected converters characteristics. It enables also evaluation of influence of the internal components non-idealities on the final characteristics of the whole A/D converter and definition of the minimal requirements on the converter components parameters in order to achieve assumed characteristics. The simulation-based comparisons between the proposed adaptive and existing sub-ranging ADCs employing the internal components with the same parameters and working for the same input signals can be performed using the toolbox.

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