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Design of an Ultra-Low Noise Analogue Front-End for Fast Voltage Pulses Measurement

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Abstract – **A $15\,MS/s$, $10\,ppm$ repeatable acquisition system to characterize $3\,\mu s$ rise-time trapezoidal voltage pulses is proposed. The system is based mainly on a low-noise, $5\,MHz$ bandwidth analog front-end. In this paper, the requirements, the concept and physical design are illustrated. Simulation results aimed at assessing the circuit performance are presented. An experimental case study on the characterization of a pulsed power supply for the klystrons modulators of the Compact Linear Collider (CLIC) under study at CERN is reported. In particular, the experimental metrological characterization of the prototype in terms of bandwidth and noise is presented.**

I. INTRODUCTION

In high-power applications, such as radars, particle accelerators, electromagnetic pulses, and pulsed lasers, pulsed power supply systems are becoming more widely used. In order to predict the amount of delivered energy and, thus, increase the efficiency of the power supply system, the generated pulses should be carefully characterized. Although the reference standards concerning pulse measurements [1] give both definitions and procedures used to evaluate the pulse parameters, a full characterization procedure in time-domain is not provided, thus, a custom method should be identified based on the application requirements. Moreover, the market interest and the research on pulse measurements are significantly dedicated to improving the immunity to interferences [2],[3],[4] demanded by the transmission protocols in Ultra Wide-Band (UWB) applications. This trend has not changed since the assessment on the state of the art for time-domain pulse waveform measurements in the nanosecond regime, produced by the National Institute of Standards and Technology (NIST) [5]. Since then, the main efforts were dedicated to upgrading the technology in order to push it to the sub-nanosecond regime. However, in particle accelerators for high-energy physics, new, more demanding applications arise. At CERN, a new particle accelerator is currently under study, the Compact LInear Collider (CLIC). The klystron modulators [6] will be operated in pulsed mode with a pulse length of $140\,\mu s$[7],[8]. To meet the requirements for the RF power quality, derived directly from the accelerator performance specifications, the modulator precision and flat-top *pulse-to-pulse repeatability*, should be guaranteed by a specific reference test-bed acquisition system. In Fig. 1 and Tab. 1, the typical input signal for the acquisition system and its characteristics, respectively, are reported. Therefore, the general interest in pulse measurement literature moves toward faster systems [9] and, in order to reach this essential goal, it relaxes the accuracy requirements. In the presented work, a new trend of slower signals, but with well-stringent accuracy requirements, arises.

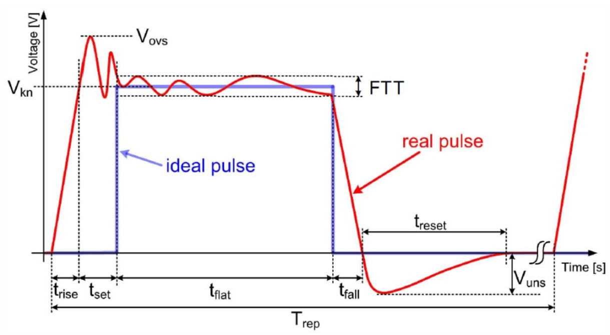

Fig. 1. Typical input pulse

Table 1. Input Pulse Characteristics

Pulse Specification		
Parameter	**Acronym**	**Value**
Nominal Pulse Amplitude Level	V_{kn}	$150\,kV$
Nominal Pulse Current Level	I_{kn}	$160\,A$
Pulse Peak Power	$P_{mod-out}$	$24\,MW$
Positive Going Transition Duration	t_{rise}	$3\,\mu s$
Negative Going Transition Duration	t_{fall}	$3\,\mu s$
Transition Settling Duration	t_{set}	$5\,\mu s$
Flat-Top Duration	t_{flat}	$140\,\mu s$
Repetition Rate	$REPR$	$50\,Hz$
Voltage Overshoot	V_{ovs}	$1\,\%$
Flat-Top Tolerance	FTT	$0.85\,\%$
Pulse-to-Pulse Repeatability	PPR	$\pm 100\ ppm$

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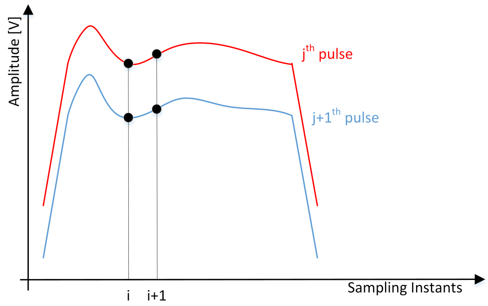


Fig. 2. Voltage flat-tops definition

II. REQUIREMENTS

The reference acquisition system consists of a high-precision high-voltage divider, able to convert the $150\,kV$ signals into $10\,V$ pulses, [10] and a high-speed high-repeatability acquisition system.

A. Pulse-to-Pulse Repeatability

The most challenging specification for this application, the so called *Pulse-to-Pulse Repeatability* (PPR), is defined as:

$$PPR = |V_{i,j} - V_{i,j+1}| \tag{1}$$

Considering two consecutive pulses flat-tops and their instantaneous voltage values in the "same" sampling instant *i*, $V_{i,j}$ and $V_{i,j+1}$ (Fig. 2), the main goal of the measuring system is to verify that:

$$PPR \leq PPR_{max} = 10\,ppm = 100\,\mu V \tag{2}$$

To assess pulses PPR in the order of $100\,ppm$ of $10\,V$, the acquisition system has to be repeatable better than $\pm 10\,ppm$ ($\pm 100\,\mu V$). The analogue conditioning system will manipulate these signals by amplifying them by a factor G and introducing a certain amount of noise *n*. After the manipulation, the second part of equation (1) will become:

$$|G \cdot (V_{i,j} - V_{i,j+1}) + (n_{i,j} - n_{i,j+1})| \tag{3}$$

By assuming that the input pulses are repeatable to within $\pm 10\,ppm$, the introduced noise could cause some "false measurements":

$$|10\,ppm + (n_{i,j} - n_{i,j+1})| > 10\,ppm \tag{4}$$

From statistical considerations about the combination of two noises $n_{i,j}$ and $n_{i,j+1}$, assumed to be uncorrelated, with $E[n_{i,j}] = E[n_{i,j+1}] = N_{rms}$, their difference can be obtained as:

$$(n_{i,j} - n_{i,j+1})_{rms} = \sqrt{E[(n_{i,j} - n_{i,j+1})^2]} = \tag{5}$$

$$= \sqrt{\underbrace{E[n_{i,j}^2]}_{N_{rms}^2} + \underbrace{E[n_{i,j+1}^2]}_{N_{rms}^2} - \underbrace{2E[n_{i,j} \cdot n_{i,j+1}]}_{0}} =$$

$$= \sqrt{2N_{rms}^2} = N_{rms}\sqrt{2}$$

Finally the Pulse-to-Pulse Repeatability definition given in (6) shall be statistically interpreted as:

$$|G \cdot (V_{i,j} - V_{i,j+1}) + N_{rms}\sqrt{2}| < T \tag{6}$$

where the threshold $T = G \cdot PPR_{max}$ is the maximum allowed variation of the signals.

B. The Analogue Front-End

The project requires, that the repeatability specification has to be verified only during the pulse flat-top, for the range of frequencies ($1\,kHz, 5\,MHz$). To prove pulse-to-pulse repeatability over a $5\,MHz$ bandwidth, the acquisition system has to sample at least at $10\,MS/s$ to respect the Nyquist criterion. In addition, the LSB has to be smaller than the repeatability threshold to be verified:

$$Q = \frac{10V}{2^{ENOB}} < 10\,ppm = 100\,\mu V \iff \tag{7}$$
$$\iff ENOB > 16.6$$

The best acquisition systems today on the market that operate at sampling rates equal or higher than $10\,MS/s$, cannot exceed 16 nominal bits, with $\pm 1\,V$ range, thus a new analogue pre-conditioning front-end has been designed. Its main requirement is relaxing the required specifications of the acquisition system, by amplifying only the significant part of the input signal. Essentially, this is achieved by subtracting the nominal value of the flat-top and the amplifying the resulting signal in order to center and zoom the flat-top in the acquisition system range.

C. Threshold-to-Noise Ratio

By assuming that both (i) two consecutive input pulses are actually repeatable and (ii) the analogue conditioning system has a good stability within the period of the train of pulses ($20\,ms$), the only factors that could affect PPR are quantization and the analogue front-end's noise. Under these hypothesis, the PPR specification can be translated into the system's noise characterization. In fact, from (6), the probability of "false measurement" is strictly related to the RMS value of the system's noise. The Threshold-to-Noise Ratio (TNR), can now be defined as:

$$TNR = \frac{T}{\sqrt{2} \cdot N_{rms}} \tag{8}$$

In practice, the TNR can be interpreted as a coverage factor; by assuming a gaussian distribution of the noise, a TNR of 3 means that the peak value of the overall noise

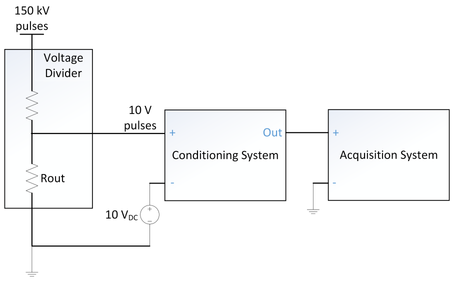


Fig. 3. Reference measurement system

will be below the threshold T 99.7% of time. Given the analogue conditioning system, the amount of noise it introduces, and therefore the TNR, is fixed. In order to increase the TNR, oversampling and filtering techniques could be applied. In fact, by oversampling, the noise power spectral density will be spread over a wider bandwidth. Thus, the TNR enhancement can be obtained by simply averaging or by using more sophisticated FIR filters in order to cut the out-bandwidth noise off [11]. In conclusion, the conditioning circuit's noise should be kept under strict control [12].

III. ANALOGUE CONDITIONING SYSTEM

A. Basic Idea: Flat-Top Removal

The repeatability specification has to be verified only for the pulse flat-top, thus the proposed conditioning system is based on the "Flat-Top Removal" technique: the nominal pulse voltage is subtracted from the pulse in order to translate the flat-top around zero. This allows the dynamic range of the acquisition system to be improved.

B. Concept Design

The main tasks of the conditioning system outlined in Fig. 4 are:

- Avoid affecting the working condition of the voltage divider by providing a high input resistance;
- Center the 10 V pulse flat-top around zero in order to improve the dynamic range of the acquisition system;
- Amplify the pulse flat-top in order to best fit the acquisition system range $\pm 1\,V$;
- Avoid saturation of the acquisition system input circuitry.

Finally, all the devices of the circuit to be designed have to work in their linear region in order to assure their long-term performance.

C. Physical Design

A possible implementation of a circuit performing the mentioned tasks is depicted in Fig. 5. The two input signals are firstly filtered through two simple RC low-pass filters in order to reduce the input noise, then two buffers are used to provide high-input resistance. Two diodes in antiparallel clip the input differential signal in order not to saturate the difference amplifier (nominal gain of 4) and ensure its long-term performance. In this stage, the input resistors (R3 and R4) are split in order to limit the current flowing through the diodes when they are active. Obviously, the same clipping operation has to be repeated at the output of the same stage. In order to conveniently set the clipping voltage, two opposite rails are used in this stage. A non-inverting stage (nominal gain of 5) was chosen because of its high input impedance, thus relaxing the quality requirements on resistor R7 as it is not involved in gain setting. Finally, after the second amplification stage, a last pair of clipping diodes are needed in order not to over-range the acquisition system input stage. The two rail voltages can be set according to the acquisition board input stage limits. The final part of the schematic (in green) represents the interface to the ADC. This has to be customized to different analogue input stages for the acquisition. Therefore, for the sake of the generality of this work , the complete interface is not discussed and all the tests carried out are referred to the "OUT" output terminal. The last consideration is about the requirements on resistor quality; in Fig. 5, all the resistors in red affect the overall gain stability and CMRR [13]. An array of 8 matched precision resistors is going to be used in the final circuit to achieve specified gain drift and CMRR.

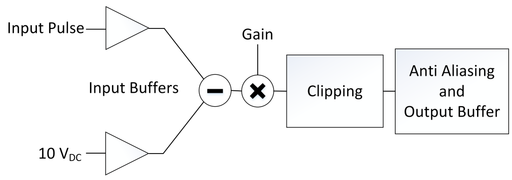


Fig. 4. Analogue Front-End Block Diagram

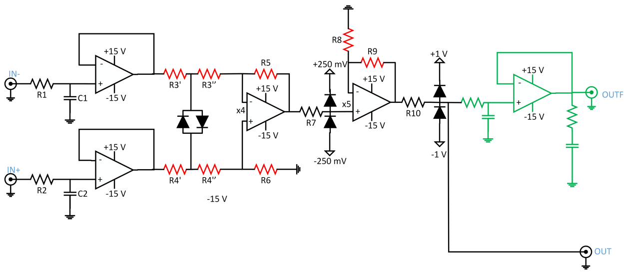


Fig. 5. Analogue Front-End Schematic.

IV. SIMULATION RESULTS

Two simulation analysis were carried out in order to assess the performance of the analogue front-end:

- Amplitude frequency response, for assessing the re-

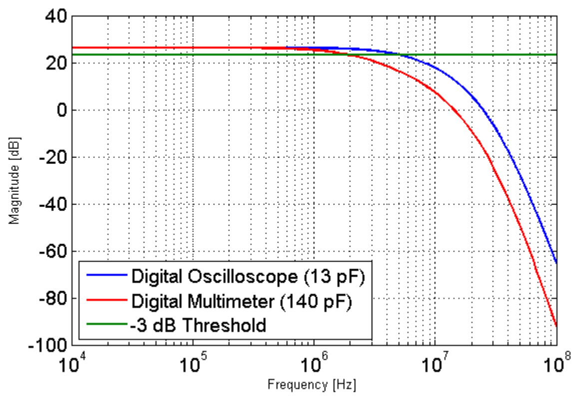


Fig. 6. Bandwidth Simulations with two different capacitive loads

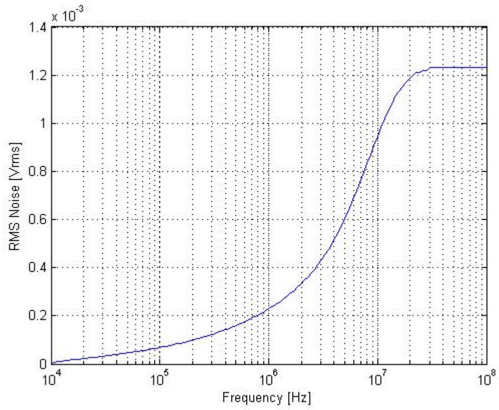


Fig. 7. RMS Noise evaluation

quired $5\,MHz$ bandwidth of the system (the phase delay introduced by the circuit was not evaluated because it is not relevant for repeatability measurements);

- Noise analysis, in order to estimate the rms noise introduced by the conditioning system and, thus, calculate the expected TNR (the noise Pspice model of the amplifiers was verified to be similar to datasheet specifications);

A. Amplitude Frequency Response

Comparable results between simulation and experimental tests were achieved by taking into account in simulation the capacitive load presented by the multimeter. With this aim, the experimental bandwidth was measured by a Digital Multimeter HP-3458A ($1\,M\Omega||140\,pF$) and the "OUT" pin was considered as an output terminal. In the results shown in Fig. 6 (red line), the capacitive load, coupled to the high output impedance of the circuit ($\approx 500\,\Omega$), heavily affects the bandwidth, by adding a relatively low frequency pole ($2\,MHz$) into the Bode diagram. Another simulation with a much smaller capacitive load, typical of high-bandwidth oscilloscopes, confirmed the bandwidth performance. In particular, in Fig. 6 (blue line), the full bandwidth of the designed circuit, with the $-3\,dB$ point moved up to $5\,MHz$, is shown.

B. Noise Analysis

A Pspice noise analysis allows the noise power spectral density (PSD) of a complex circuit to be assessed. The rms value of the estimated noise can therefore be obtained as:

$$N_{rms} = \sqrt{\int_{f_L}^{f_H} PSD(f)df} \qquad (9)$$

where the integration boundaries f_H and f_L used in simulation are respectively $10\,kHz$ and $100\,MHz$. In Fig. 7, an RMS noise of about $1.2\,mV$ is shown. A TNR calculation, reveals a value slightly above 1. However, the filtering effect of the limited bandwidth of the acquisition system, directly connected to the output of the conditioning system, must be considered. As an example, the state-of-the-art acquisition board NI-PXI-5922 from National Instruments has a nominal bandwidth of $6\,MHz$ when sampling at its maximum speed of $15\,MS/s$, thus, some filtering effect is expected (accordingly increasing the TNR). On the other hand, if the NI-PXI-5122 is considered, oversampling and decimation could improve the TNR consistently. In fact, by oversampling the signal at $100\,MS/s$ and averaging 10 consecutive samples, the noise will be reduced by a factor equal to $\sqrt{10}$, increasing the TNR up to about 3.7. In conclusion, the noise that should be considered when calculating the TNR, must be evaluated for a specific acquisition system.

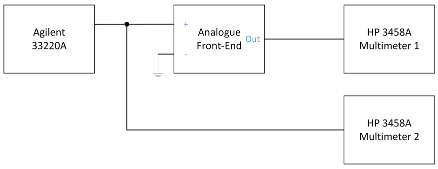
V. EXPERIMENTAL RESULTS

In this section, simulation analysis is compared with an experimental implementation at CERN, carried out within a case study for the CLIC project.

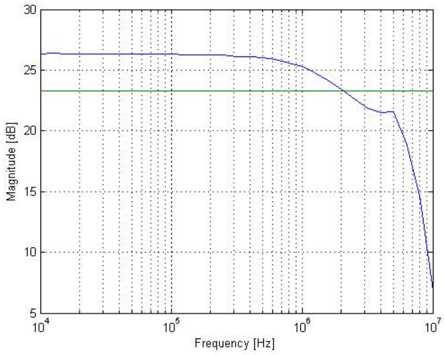
A. Amplitude Frequency Response

The measurement setup (Fig. 8) consists of an arbitrary waveform generator (Agilent 33220A) and two digital multimeters (HP 3458A). The two multimeters were firstly characterized up to $10\,MHz$ and, in the worst case, their difference was smaller than $0.6\,dB$. Even if the results are compatible with the simulation (when taking into account the high capacitive load of the DMMs), the measured shapes are consistently different beyond $5\,MHz$. This effect is probably due to different poles localized in that region and interacting each other. In fact, around $5\,MHz$, there is:

- the dominant pole of the conditioning circuit ($\approx$



(a) System Frequency Response Setup



(b) Amplitude Bode Diagram

Fig. 8. Bandwidth Experimental Evaluation

$5\,MHz$);

- the dominant pole of the multimeter ($\approx 10\,MHz$);
- a pole given by the coupling between the output resistance of the conditioning circuit and the input impedance of the multimeter ($\approx 2\,MHz$).

This effect can be made negligible in the final circuit by a suitable compensated ADC interface (green part in Fig. 5).

B. *Noise Analysis*

For this test, the simple measurement setup of Fig. 9 allows the Peak-to-Peak noise, as well as its RMS value, to be assessed using a digital oscilloscope (Tektronix MSO 4104). The scope internal noise was measured to be negligible with respect to the analogue front-end one by shorting the scope input to ground. The test showed that the RMS noise levels of the circuit, in experiments ($1.49\,mV_{rms}$) and in simulation ($1.22\,mV_{rms}$), are comparable. However, the prototype is not yet optimized in terms of noise immunity (e.g. not yet shielded) and the bandwidth of the digital oscilloscope is much more than $100\,MHz$, thus, a greater amount of noise is likely to be measured with respect to the simulation.

VI. CONCLUSION

A low-noise $5\,MHz$ bandwidth analogue conditioning circuit for fast trapezoidal voltage pulses measurement has been realized. The system's features were assessed by

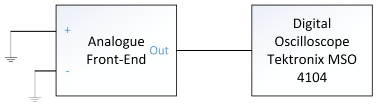


Fig. 9. Noise Evaluation Setup

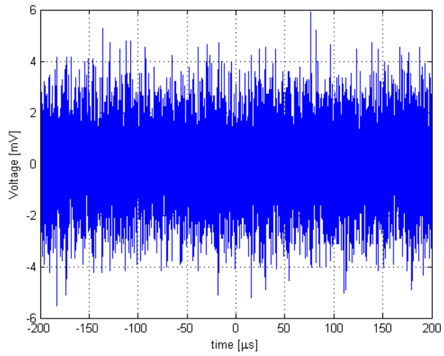


Fig. 10. Measured peak-to-peak Noise

Pspice simulations during the design process. Experimental tests on a case study at CERN for the CLIC project confirmed the expected performance. In particular, bandwidth and noise turned out to be the most critical aspects. While noise specification is already fully satisfied, the presence of multiple poles localized around $5\,MHz$ produces an unexpected behaviour of the circuit in that region. This undesired effect is expected to be solved when a compensated ADC interface is used as circuit termination.

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