

Current and voltage synchronous measurements using NI cRIO system with sigma-delta ADC NI 92xx and S.E.A. GPS modules

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Abstract - the article describes one of the solutions for improving the accuracy of synchronized measurement for electrical grids using sigma-delta ADC measuring systems. Key problems and their solutions are analyzed. A description is given for the developed algorithm and its implementation in FPGA on National Instruments cRIO platform. The voltage and current measurements were conducted on the NI 9225 and NI 9227 modules respectively. Synchronization is provided by the PPS signal, which is generated by a S.E.A. 9472 GPS receiver module. The essence of the proposed method consists of clocking the NI 9225 and NI 9227 modules by created in the FPGA software clock generator at the frequency of 12.8 MHz. This generator is based on the internal 200 MHz FPGA clock and synchronized to UTC by a PPS signal. The accuracy of the synchronization was experimentally confirmed by measuring the voltage via two identical measuring systems and comparing the results.

I. INTRODUCTION

Synchronous measurement technology is developing rapidly with the advent of satellite navigation systems in power grids. The first phasor measurement units (PMU) appeared in the early 1980s and were intended primarily to measure voltage and positive sequence current vectors (phasors) for fundamental harmonics and frequency [1-4]. The cost of a single PMU ranged from 10k to 70k USD, which hampered their widespread use in electrical grids [3]. Phasor measurement units were primarily implemented for the Wide Area Measurement System (WAMS), which allows monitoring of transients in the energy system, and to analyze the causes of faults.

Intelligent electronic devices (IED), merging units (MU) and optical current and voltage transformers began to be used when information and telecommunication technologies for implementing synchronous measurements on digital substations were developed [5]. IED functions are not only implemented for measuring current phasors and the voltages of single phase

fundamental harmonics, but also for measuring higher harmonics, as well as the possibility of electric power metering, and acquisition of current and voltage instantaneous values. Optical current and voltage transformers provide an instant flow of currents and voltages using protocol IEC 61850-9.2 with data rate of 40 or 80 points per period [5].

Due to high cost of PMU and the need for high speed communication channels for transmitting information to the phasor data concentrators (PDCs), WAMS-technology is primarily used in supply mains (voltage above 110 kV). However, a number of studies on the use of synchronous measurements in distribution networks [6-9] showed their use was promising for important tasks such as power quality analysis and the identification of sources of distortion in the network, localization of faults, the localization of non-technical electricity losses and many others. However, widespread adoption of this technology requires the development of relatively cheap multifunction IEDs, that cost only a few tens of dollars. It should be noted that the conditions exist for reducing large-scale production costs. The cost of specialized chips with the sigma-delta ADC input for the manufacture of electronic electric power meters, is no more than a few dollars, and the cost of the chip with a GPS receiver and GPRS transceiver does not exceed \$30.

Measuring systems built on the NI cRIO platform can be used for prototyping IED [10,11]. The basic cRIO consists of an integrated high-performance controller that has Real-Time processor and a multi-slot chassis with FPGA. There are several C-series input/output modules for the cRIO platform that are designed to meet the challenges of the power sector. The NI 9225 module is for measuring voltage and the NI 9227 module is for measuring current. Until recently, S.E.A. GPS modules were mainly used to synchronize cRIO measurements (in 2012 NI launched its own NI 9467 GPS module). In addition, the sources of PPS signals from third party GPS receivers can be used for synchronization. Despite the relatively high cost of IED on the NI cRIO platform, they

can be used for research and to refine the parameters of distribution networks in mobile laboratories. More detail regarding the operation of the cRIO system and modules, as well as their technical specifications are presented in Section II.

The difficulty of developing synchronous measurement systems based on NI cRIO 92XX modules, lies in the fact that their internal clock generators are independent and can't be directly synchronized with a pulse per second (PPS) signal. The following solutions can be used to organize synchronous measurements in this situation:

1. The PPS signal is applied to one of the NI 9225 module's unused input.
2. Free-running sampling process is integrated with a-posteriori synchronization.
3. Direct synchronization of the sampling process to Coordinated Universal Time (UTC) by a special circuit with feedback.

The article describes the work of the measuring system using the third solution. Section 2 describes the measurement system based on the cRIO with the NI 9024 controller and the NI 9118 chassis. The third section contains a description of the algorithm and program for synchronizing measurements of currents and voltages, executed by the NI 92XX modules, using the PPS signal from the S.E.A. 9472 module. Section 4 describes the experiment and its results. The essence of the experiment was to compare the results of reference voltage signal measurements made by two identical measuring systems.

II. DESCRIPTION OF THE MEASURING SYSTEM COMPONENTS

The cRIO measuring system was used as an IED prototype, consisting of a NI cRIO-9024 real-time controller with an NI cRIO-9118 chassis and C Series modules (Figure 1).

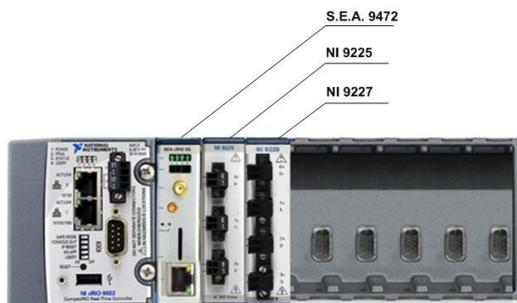


Figure 1. Picture of the measurement system based on the NI cRIO-9024 controller with a NI cRIO-9118 chassis and C-series modules

The NI cRIO-9024 real-time controller is equipped with a powerful Freescale 800 MHz CPU, 4 GB non-volatile flash memory, and Ethernet, USB and RS-232 interfaces. The controller executes the application with a

high degree of reliability and consistency, storing data in the internal flash memory and communicating with external devices via IO. The NI cRIO-9118 FPGA-chassis contains eight slots for C-series input/output modules. The chassis is equipped with Xilinx Virtex 5 LX 110 FPGA. The main clock of the FPGA-chassis is at a frequency of 40 MHz. FPGA provides access to low-level hardware resources of input-output modules. The work of FPGA is configured with software. At the hardware level, the program for FPGA creates synchronous input-output data, processing, analysis and transmission to the real-time processor. The program for cRIO is designed in the NI LabVIEW graphical programming environment. The program for the Real-Time controller is developed using the NI LabVIEW Real-Time Module. The program for the FPGA is developed using the NI LabVIEW FPGA Module.

Modules are installed in FPGA-chassis slots. The measuring system that has been developed contains three modules: S.E.A. 9724, NI 9225, and NI 9227. The S.E.A. 9724 Module receives GPS signals, and generates a PPS, delivering it to the FPGA every second. Likewise, the S.E.A. 9724 is equipped with a standard GSM 3G transceiver with a maximum transfer speed of up to 7.2 Mbit/s. The NI 9225 is a three-channel module for measuring voltage. Measurements range from -300 V to 300 V RMS (Root Mean Square). The NI 9227 data acquisition module is a four-channel current measuring module. Measurement range of -5 A to 5 A RMS. Each channel of the NI 9225 and NI 9227 is equipped with a 24-bit sigma-delta ADC, having a sample rate up to 50 kHz per channel.

The Real-Time controller (1) is connected to FPGA with (3) high speed bus (2). Input-output modules (4) are connected to FPGA clock and data buses. (Figure 2).

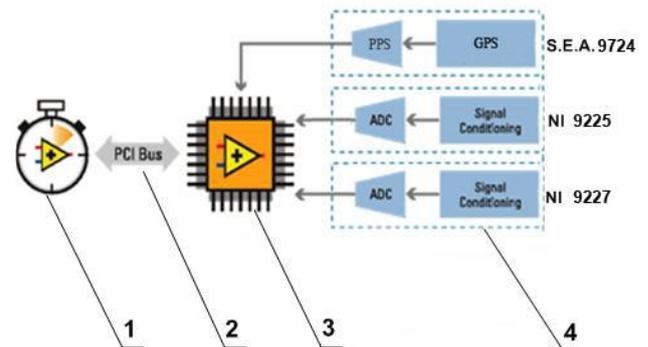


Figure 2. Block diagram of the measuring system based on the cRIO platform

III. DEVELOPMENT AND IMPLEMENTATION OF FPGA SYNCHRONIZATION ALGORITHMS

A. Fundamental synchronization problems

There are two major problems in developing the synchronization algorithm measurements from the PPS signal using NI 92xx modules with sigma-delta ADC:

1. No built-in ability to synchronize the chassis' internal clock signal generator with FPGA PPS signals.

2. The chassis' internal clock signal generator and the NI 92xx modules are independent of each other.

It should be noted that the first problem can be solved by using the NI 9467 GPS module that went on sale in 2012. This module uses the FPGA Timekeeper program to synchronize the FPGA with GPS. This program allows a GPS time stamp to be assigned to each FPGA operating cycle. Therefore, the samples produced by the FPGA from the data collection modules are synchronized with the time of the GPS. Unfortunately, this module, unlike the S.E.A. 9472 module, does not have a built-in 3G transceiver and requires a separate module with a transceiver.

The first problem can be solved by eliminating the use of the internal clock like source of precise time stamps, when using S.E.A. modules or the external PPS signal. In this case, a programmable FPGA clock can be used to synchronize with the UTC, compensating for the temporary instability of the crystal oscillator clock generator of the FPGA chassis.

The solution to the second problem is not difficult, since the NI 92XX modules allow external or internal programmable clock generators to be used. The main challenge in this is to create FPGA synchronized with the PPS software generator at a frequency of 12.8 MHz. An additional problem is that the frequencies of the clock generator chassis with FPGA (40 MHz and 200 MHz) are not in multiples of the of the NI 92xx module clock generator frequency (12.8 MHz).

B. Mathematical basis of the generation method for the 12.8 MHz frequency based on a 200 MHz generator

Consider in more detail the theoretical basis of receiving a signal frequency of 12.8 MHz from the signal of a clock generator chassis with FPGA. A generator with a frequency of 200 MHz is more suitable for this purpose. The oscillation period of this generator is 5 ns, and the period of the generator is 12.8 MHz, equal to 78.125 ns. Obviously, algorithmically, it is easy to implement an oscillator frequency of 12.5 MHz. The oscillation period is a multiple of 5 ns and is 80 ns. In order to do this, it is necessary to switch the output signal back and forth from 1 to 0 every 8 frames. The output signal in this case will be strictly periodic and have a duty cycle equal to 2. It should be noted that the NI 92XX modules allow a clock generator frequency to be used other than 12.8 MHz. However, at a clock generator frequency of 12.5 MHz, the frequency sampling of the measured signal is not a multiple of the power system's nominal frequency (50 or 60 Hz). This prevents a measuring system being used for implementing protocol IEC61650-9.2, which requires 40 or 80 samples per cycle. In addition, in order to ensure synchronicity, measurements in various IED will require periodic restarts of the sigma-delta ADC at agreed times

(for example, at the beginning of each second of UTC).

The operating principle of the sigma-delta ADC allows some temporary instability of the master generator and of the designated frequency resampling. If this sampling rate remains stable, the measurement should coincide with the results in a stable master generator. This allows a 12.8 MHz signal to be formed by a periodic 5 ns reduction of the generated output signal. The numbers 5 (oscillation period of a 200 MHz generator) and 78.125 (oscillation period of a 12.8 MHz generator) have the least common multiple, 625. Thus, 8 periods of stable and unstable 12.8 MHz generators will take place in the range of 625 ns (Figure 3).

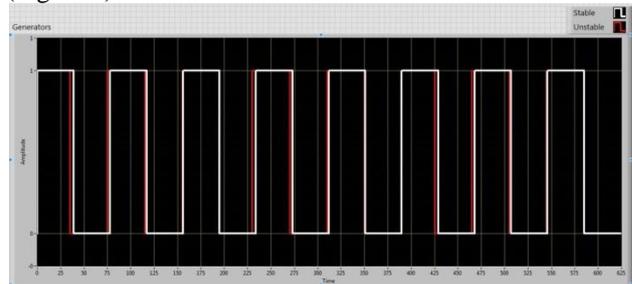


Figure 3. Comparison of signals for stable and unstable 12.8 MHz generators

In these eight periods in an unstable oscillator the 1st, 3rd and 6th periods have durations of 75 ns, and the 2nd, 4th, 5th, 7th, and 8th at 80 ns. In this case, the signal duty cycle during periods 2, 4, 5, 7, and 8 is 2; 2.143 in periods 1 and 6; and 1.875 in the third period. In a stable generator all 8 periods of stability, have a period of 78.125 ns and duty cycle of 2.

It is significant that the frequency of 1.6 MHz, corresponds to the period of 625 ns, the largest multiple of the clock frequency used in the sigma-delta ADC 92XX modules (50 kHz). This ensures the identity of the measurements performed by various IED.

C. Development and implementation of the 12.8 MHz frequency generation algorithm based on the 200 MHz generator in the FPGA

Synchronization methods between the data acquisition module shown in [12] and two cRIO chassis were adapted as a prototype for the implementation of the 12.8 MHz frequency generation algorithm based on the 200 MHz generator in the FPGA

The synchronous generation algorithm consists of two cycles, "Loop 1" and "Loop 2" (Figure 4). "Loop 1" cycle is synchronized from the FPGA generator with 40 MHz (7). "Loop 2" cycle is synchronized from the FPGA generator with 200 MHz (12). "Loop 1" cycle begins when the program is launched (5). This cycle waits for the rising edge of the PPS pulse from the 9724 S.E.A. module (6). When the rising edge of the PPS sets the start trigger cycle (restart) in a state of "true." In the next cycle, "Loop 2" starts (at the arrival of the front of the

first PPS) or restart (at the arrival of the front of the next PPS) (3). In this cycle, a reference signal is generated for the clock frequency of 12.8 MHz. 12.8 MHz signal generation is performed by alternately setting the durations of the output signal's high and low states. The required amount of delay is 7 or 8 cycles at 200 MHz. The amount of delay during operation is successively selected from an array of constants comprising 16 elements: {7, 8, 8, 8, 8, 7, 8, 8, 8, 8, 7, 8, 8, 8, 8, 8}. Transition to the first element is carried out after sampling the 16th array element. The output signal shown in Figure 3, is used as a reference signal for the NI 9225 (9) and NI 9227 (11) module's internal timebase clocks (8), (10).

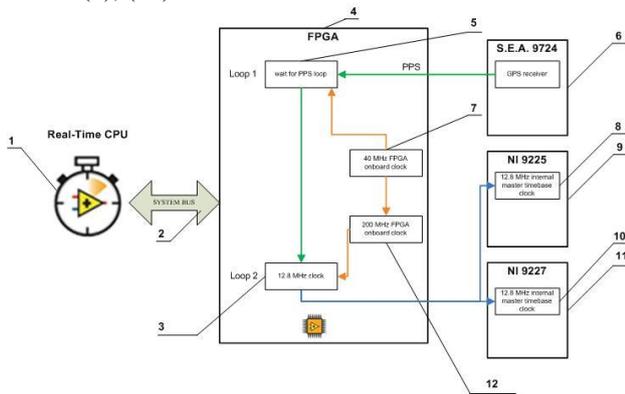


Figure 4. Clock timing diagram of data collection modules

Voltage and current samples received from the NI 9225 and NI 9227 modules via the system bus (2) are transferred to the cRIO's real-time controller (1) system. The real-time controller stores data in binary file format. Each file contains a sample for a predetermined measurement period. The resulting binary files are transferred to the server via FTP. Files on the server are used for subsequent analysis.

Two identical measuring systems were made and programmed for an experimental study of the effectiveness of the algorithm for synchronous measurements of C Series modules with sigma-delta ADC. A description of studies and their results are given in section IV "Experimental Results".

IV. EXPERIMENTAL RESULTS

Experimental studies to assess the accuracy of synchronization were performed by comparing the results of measurements of the reference voltage signal from two identical measurement systems (Figure 5).

Experiments were carried out with a predetermined sampling frequency of 25 kHz. Sinusoidal voltage was generated by programmable voltage sources and current from the Energoforma 3.3 [13] in single phase and had an effective value of 57.7 V at 50 Hz. Measured instantaneous voltage values are recorded on each cRIO

system with a sampling frequency of 25 kHz, respectively, to files for one second from the time of joining the rising edge of the PPS pulse.

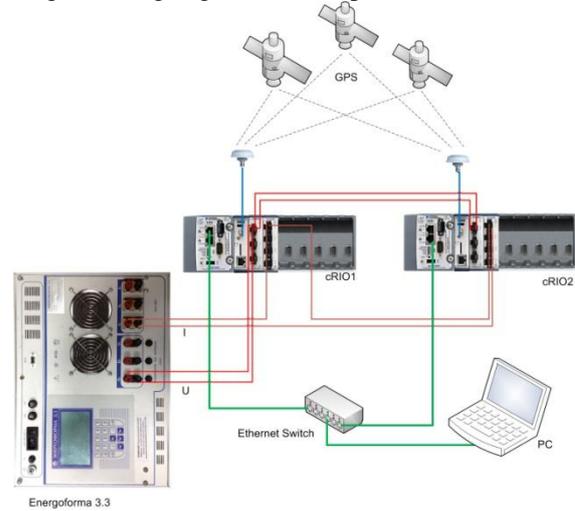


Figure 5. Connection of measuring systems for the experiment

A graph was plotted, representing the difference between the instantaneous voltages for preliminary evaluation of the phase shift between the signals measured by the first and second cRIO systems (Figure 6).

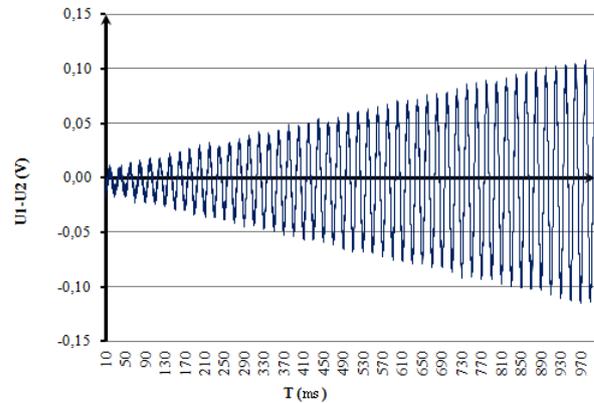


Figure 6. Graph of the differences in signal voltages

Based on analysis of the graph, signal differences vary from the frequency of the measured signal. The amplitude of the signal increases linearly with time. It should be noted that the current values of the stresses calculated by voltage measuring systems cRIO1 and cRIO2 at 20 ms intervals, were almost equal to each other at all 50 measurement periods. This suggests that the cause of the linear magnification in the signal differentiation is the systematic instability of the 200 MHz clock generators of the cRIO systems that were used.

The determination of the relative systematic instability of clocks was performed by comparing the measured

signal at the intersecting points of zero values (Figure 7).

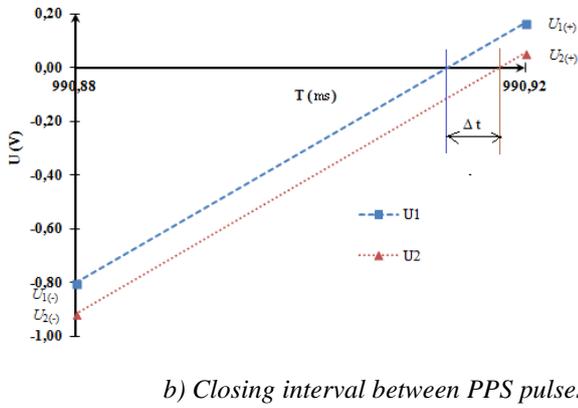
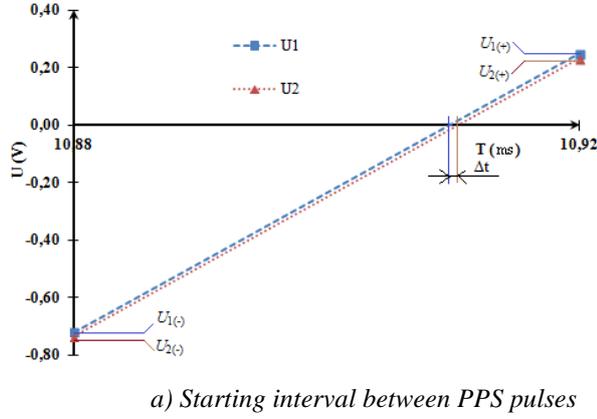


Figure 7. Graphs of voltage signals at the time of zero-crossing

Assuming that the signal is changed linearly at the moment it crosses zero, the value of the time skew difference of the two measured signals may be defined as follows:

$$\Delta t = \left[\frac{U_{1(+)} - U_{1(-)}}{U_{1(+)} - U_{1(-)}} - \frac{U_{2(+)} - U_{2(-)}}{U_{2(+)} - U_{2(-)}} \right] \frac{1}{F_d}, \quad (1)$$

wherein $U_{1(+)}$ and $U_{2(+)}$ are voltage values in the sample after the zero crossing, the first and second measured system, respectively; $U_{1(-)}$ and $U_{2(-)}$ are voltage values in the sample before the zero crossing, the first and second measured system, respectively; F_d is sigma-delta ADC sampling rate.

The calculation results of the time skew difference of the two measured signals in time, are shown in Figure 8.

As shown in Figure 8, the time skew difference in the time domain increases linearly from 0.5 to 4.6 μ s. As noted above, this can be explained by the systematic instability of 200 MHz clock generators at cRIO1 and cRIO2. Since the 12.8 MHz generators use 200 MHz generators as a reference, they also have a similar

systemic instability. This instability is due to the individual characteristics of the crystal generator. Its value for a particular cRIO system can be calculated by counting the number of 200 MHz clock pulses between the two PPS fronts.

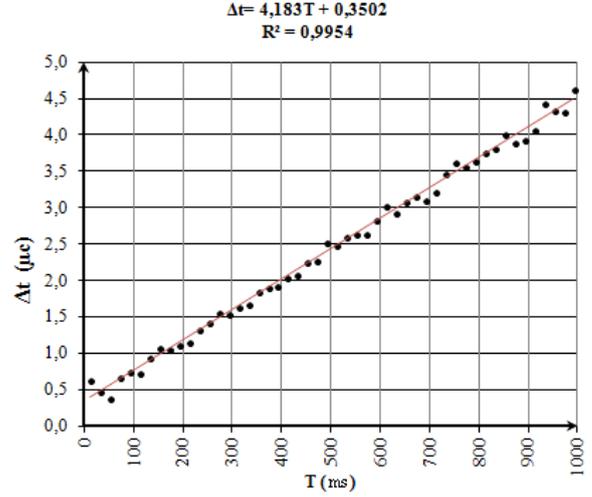


Figure 8. Time skew difference graph of two measured signals

Suppose that the number of pulses is N_p . Then the value of the time skew dT (c) can be determined by the formula:

$$dT = \frac{N_p - 200\,000\,000}{N_p}. \quad (2)$$

Systematic uncertainties may change over time. For example, due to changes in ambient temperature, there is ageing of the quartz and other factors. Changing systematic instability between two adjacent measurement periods with duration of 1 s is not critical for a specific measurement system. However, instability should be considered when determining the time skew dT (c) in accordance with (2) the impact on the result of temporary PPS. The amount of temporary instability of PPS for S.E.A. 9724 modules may reach ± 150 ns. The method proposed in [14] and implementation of a Kalman filter can be used to compensate for this instability.

In this case, the algorithm and 12.8 MHz software generator discussed in Section III can be adjusted to compensate for the time skew. The value of making corrections is reduced in a corresponding increase or decrease in the number of 75 ns periods. If we take the value of the maximum time skew equal to 5 microseconds at second interval, the number of increasing or decreasing 75 ns periods will be equal to 1,000. To implement the compensation value of 100 ns (corresponding to PPS accuracy) the number of increasing or decreasing 75 ns periods will be equal to 20. It should be noted that this approach cRIO internal clock

correction is not performed and the time stamp must be formed in software, assuming that the time interval between samples is strictly determined by the sampling rate of delta-sigma ADC in NI 92XX modules.

After compensating for systematic instability of cRIO 200 MHz clock generators, time skew measurement systems will be determined by PPS accuracy and the random instability of these generators. Figure 9 shows the distribution of the time skew between the two measuring systems after compensating for the systematic instability of cRIO 200 MHz clock generators. Based on the bar graph, jitter does not exceed ± 250 ns.

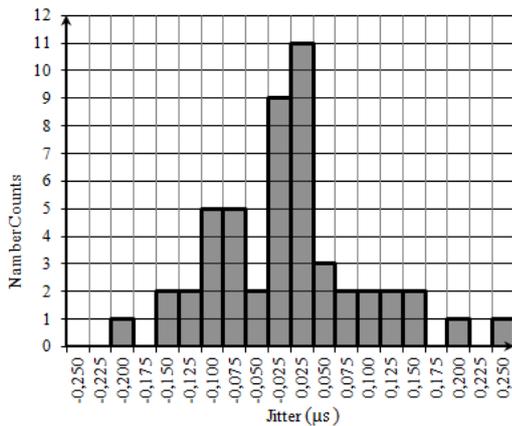


Figure 9. Jitter histogram

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V. CONCLUSIONS

The results of the experiments have shown that the proposed C-series algorithm synchronization modules based on the PPS signal make it possible to measure voltage and current with a time skew of no more than 5 μ s.

To improve the accuracy of synchronization, auto-tuning is suggested for 12.8 MHz generators using PPS. This reduces the amount of time skew to 0.25 μ s.

The developed algorithm is flexible and can be modified for use with C-Series modules that use a clock with frequencies other than 12.8 MHz.

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