20th IMEKO TC4 International Symposium and
18th International Workshop on ADC Modelling and Testing
Research on Electric and Electronic Measurement for the Economic Upturn
Benevento, Italy, September 15-17, 2014

An Automated Digital Testing System for High-Resolution ADC Based on the Feedback Loop Method Using Low-Resolution DAC Signal

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Abstract –**This paper presents an automated digital testing system for high-resolution ADC with low-resolution DAC signal. This system mainly comprises a low-resolution DAC (or signal source), a feedback loop circuit, a bias voltage device and a reference voltage source controlled by a digital potentiometer. By the digital potentiometer constantly fine-tuning the reference voltage and joining bias voltage timely, the output of DAC can completely measure all the codes of high-resolution ADC under test. This system solves the problem that low-resolution DAC signal tests high-resolution ADC inaccurately, which not only greatly reduce the test cost, but also can be applied to a variety of ADC hardware testing environments. The simulation results show that, 10-bit DAC signal in this system can measure each code of 14-bit ADC twice at least. The proposed testing system shows a new feasible solution to high-resolution ADC test.**

I. INTRODUCTION

The ADC (analog-to-digital converter) is considered as one of the most important mixed-signal circuits in the world. As the interface between the digital processing systems and the actual analog world, ADC rapid development promotes the progress of the electronics industry, affecting the development of human life. Every year, many famous semiconductor companies will design a large number of precision ADC chips and products. But the following questions are that how to accurately test the reliability of the mixed-signal systems and efficiently point out the shortage of designs. At present, the test cost has accounted for a big proportion of chip manufacturing costs, and sometimes even is greater than the sum of ADC design and process [1]. The formal testing standard faces more and more challenge, because it needs signal sources be 2-3 bits higher than device under test (DUT) [2]. Thus, request of the hardware test platforms is very harsh, and cannot be fulfilled in some special cases. Therefore, how to accurately test high-precision ADC, and as far as possible to reduce the test cost, have become new research focuses.

There are many excellent researchers interested in this direction. A number of representative works are present here. In [3], the author evaluated the possibility of implementation test standard recommendations,especially for identification of nonlinearity of high-resolution ADC and correction nonlinear component of systematic error. [4] proposed a BIST scheme for high-resolution ADC testing using only digital testing environments, which was capable of characterizing ADC transition levels one by one with small hardware overhead. The authors in [5] described a novel method of estimating the “true” static nonlinearity of an ADC using a low-frequency sine signal, and the ADC under test had to be “fed” with this “linear” portion of the sine wave. In [6], authors presented algorithms that can use any monotonic signal with linearity much lesser than the ADC under test to estimate the static parameters. However, there are few industry applications for high-resolution ADC test. Most of the existing methods specify the ADC architecture or request higher resolution signals. These drawbacks limit the usage of the testing methods on ADCs.

This work introduces an automated digital testing system for high-resolution ADC. It provides an improvement program based on the existing feedback loop method, adding some special circuits. In addition, this paper supports some complimentary content, according to the traditional test standard. Since the signal source owns less resolution, whose interval is much larger than the ADC’s under test (for example 10-bit DAC interval is 16 times of 14-bit ADC). By increasing the number of tests, it can effectively compensate the deficiency. Simulation results show that, a 10-bit DAC signal can effectively test 14-bit ADC.

The rest of the paper is organized as follows. Section II will review the original feedback loop method. The testing system that uses small special circuits and some useful complimentary content will be described in Section III. In section IV, some simulation results demonstrate the working of the proposed methods by using MATLAB simulations. We will evaluate the system and conclude the paper in section V.

ISBN-14: 978-92-990073-2-7

II. REVIEW OF THE ORIGINAL FEEDBACK LOOP TESTING SYSTEM

Feedback loop testing system is widely used test method for determining ADC transition levels [7]. In this method, an input is applied to the ADC firstly, and the converter is triggered secondly. Then the results of the conversion are compared to a desired value. If the ADC output is below the desired value, the input will be raised by a fixed amount. If the ADC output is equal to or above the desired value, the input will be lowered by a fixed amount. This process should be repeated, until the ADC input has settled to a stable, average value. After the loop has settled, the input value can be either measured. Moreover, if the input source is well calibrated, its transfer function can be computed. A block diagram is given in Figure (1).

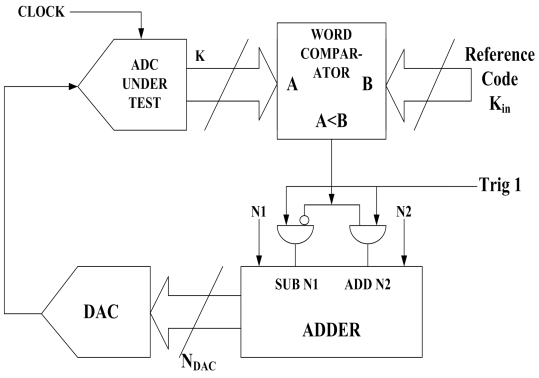


Fig. 1. Feedback loop testing system.

In this diagram, an N-bit DAC (digital-to-analog converter) generates the feedback signal. For clarity, this method will be discussed in terms of a DAC-generated input. N1 and N2 of Figure .1. are equal and assigned the value N_0. According to the result of the comparison between the ADC's actual output code k, and the given reference code kin, the DAC's value is incremented or decremented by N_0 after each conversion cycle. Once the code transition level T[kin] of the ADC has been reached, the feedback loop causes the input signal to cross this transition in steps, which can be chosen to be as small as the DAC resolution. The ADC input level is calculated from the known DAC transfer function.

III. THE AUTOMATED DIGITAL TESTING SYSTEM

This work is proposing an automated digital testing system for high-resolution ADC that utilizes low-resolution DAC signal. It is added by some new and special circuit improvement, on the base of the original feedback loop method. In the actual ADC testing, technical personnel and testing engineers not only pay close attention to the accurate test results, but also hope to reduce test hardware requirement, especially with a less resolution and cost signal source. But in the actual researches, they often encounter many difficulties. For instance, firstly, low-resolution DAC's LSB (Least Significant Bit) is much larger than ADC's under test, which can't be changed by common approaches at present, as shown in the Fig. 2. The origin feedback loop method application is also limited by the resolution of DAC signal. Secondly, it can't directly test all ADC codes, which is the most important. The key point to ADC testing is to measure each code of ADC as far as impossible, before beginning data analyses and other researches. What is more, in the traditional test standard, output range of DAC must exceed input range of ADC under test, to get all the precise digital output codes, which increases the test challenge. In order to overcome the difficulties above, the authors of this paper did many researches and explorations, and found an effective strategy at last.

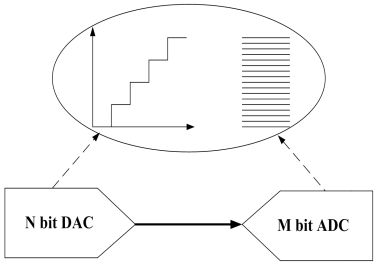


Fig. 2. 2-bit DAC test 4-bit ADC.

A. Hardware improvement

Currently, there are more and more DAC chips that use the design of external reference voltage source V_{REF}, whose output range are also determined by it. What is more important, the DAC can get more complex and widespread applications. According to the feature of linear increasing, and the output range V_{OUT} of a n-bit DAC can be modeled as

$$V_{OUT} = \left(\frac{D}{2^n} \right) \times V_{REF} \quad (1)$$

Where D is the input data of DAC.

The proposed testing system utilizes this feature and connects a variable resistance circuit structure between the external voltage V_{EXT} and DAC chip, which contain a reference resistor R_{REF} and a digital potentiometer resistor R_{SET}, as shown in the Fig. 3. In this stucture, the digital potentiometer can be controlled from the outside, indirectly making the resistance output vary linearly. Through trimming resistor, like the lever principle, digital potentiometer can change external reference source V_{REF} and make the output range V_{OUT} of DAC signal change orderly. This process makes the variation range of DAC signal reach the interval of high-resolution ADC under test, which staggers the fixed codes between signal source and the corresponding ADC. The most significantly, low-resolution DAC signal source can measure each code of high-resolution ADC in theory.

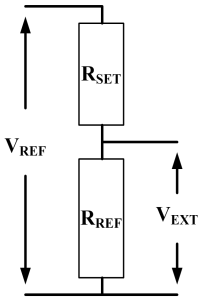


Fig. 3.The variable resistance circuit.

According to the newest survey, the current minimum interval of digital potentiometer step ΔR_{SET} can reach 4 ohms, relative to K or even tens of K ohms of the set reference resistance R_{REF}, which equally "add" several resolutions to the DAC signal source. According to the given n-bit ADC under test, the relationship between reference resistor R_{REF} and the digital potentiometer step ΔR_{SET} is

$$\frac{\Delta R_{SET}}{R_{REF}} = \frac{T_N - T_0}{2^n} \tag{2}$$

Where N is the maximum number of the code; T is the transition level of ADC code.

Based on the above set resistance, the corresponding relationship between output range V_{OUT} and the digital potentiometer resistance R_{SET} is

$$V_{OUT} = \left(\frac{R_{SET} + R_{REF}}{R_{REF}} \right) \times V_{EXT} \tag{3}$$

Because the output of DAC signal source linearly increases equivalent to "stretching", both ends of the ADC digital codes will be completely tested, but the center part may be undetectable at the same time. It needs to take some special technical means. The proposed system places a bias voltage device at the output of signal source, by which making the most dense output range of DAC cover the center codes of ADC. It can solve the problem well.

B.The number of repeating test

The original feedback loop method needs to repeatedly test, in order to reach the stable state. But it does not give an exact number, and just triggers constantly. Differently, the fundamental purpose of this system is to measure all the codes of high-resolution ADC completely. At the same time, the test number should be given in accordance with the number of digital potentiometer changing. Since the system uses the low-resolution signal source, whose interval is much larger than the measured ADC's (for example, 2-bit DAC interval is 4 times of 4-bit ADC). According to this situation, a large enough test number can effectively compensate for the deficiency. From this, the paper found a feasible way for low-resolution signal testing high-resolution ADC. So it is important to make some correction about the traditional standard. In the traditional testing standard, it is ruled strictly as

$$n_E \geq n + 3 \tag{4}$$

And in the proposed system, its new relation is

$$n_E + \log M \geq n + 3 \tag{5}$$

Where n_E is effective bit number of DAC signal source; M is the number of repeating test. Here, take the note that, according to the hardware improvement, half of the number is used before adding bias voltage to the system, and the other is used after that.

C. The complete system

Summing up the above content, the proposed automated digital testing system adds variable resistance circuit structure and some hardware improvemnt to test high-resolution ADC. The complete system is

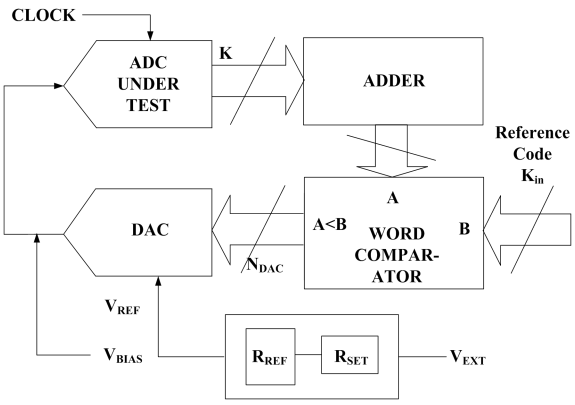


Fig. 4. The complete system.

The proposed automated digital testing system uses low-resolution DAC signal source to test high-resolution ADC accurately. So the test cost can be reduced greatly. This paper also gives following testing steps

1) Choose the reference resistor R_{REF} and the minimum interval of digital potentiometer step ΔR_{SET}, and set the variable resistance circuit structure;

2) Calculate number of repeating test based on the resolution of DAC signal source an ADC under test;

3) Increase the digital potentiometer resistor, and test ADC with the half number;

4) According to the test result, plus a bias voltage and test with the left number;

5) Calculate the tested number of the ADC codes.

What is more important, the system does not limit the ADC architectures and gives enough theoretical analyses. It can be uesd in many experimental environment and easy to implement.

IV. SIMULATION RESULTS

Simulation has been done for the automated digital testing system. A 2.0Vpp 14-bit pipelined ADC and a 10-bit DAC are modeled ideally. This paper pays attention to the ability that output of low-resolution DAC signal source can measure each code of high-resolution ADC. So, there is no need to add any noise and error in DAC or ADC model. Besides them, the input signal a ramp signal which is widely used.

As the minimum interval of digital potentiometer can reach 4 ohms, reference resistance is set to 32K. And on the basis of formula (5), the number of the test is 2^7, in accordance with the number of digital potentiometer changing. In order to verify the system, the simulation will show the test process with 2^4, 2^5, and 2^6 times

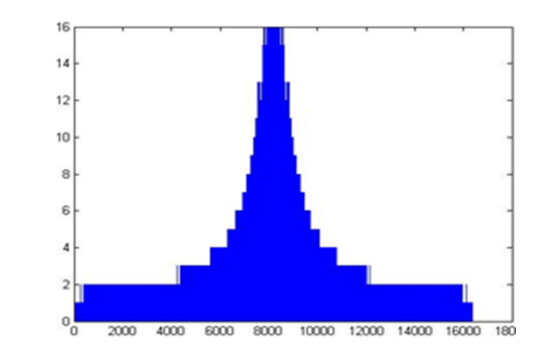


Fig. 5. Test with 2^4 times.

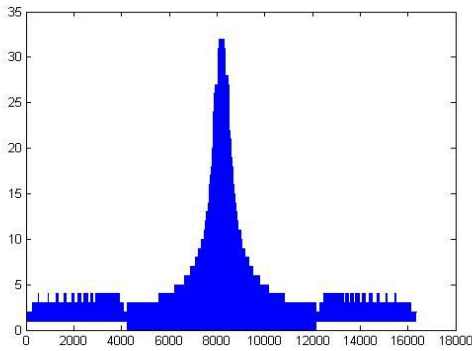
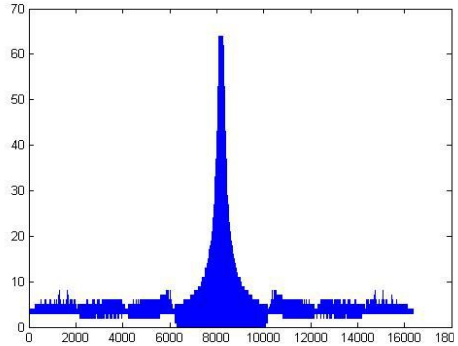


Fig. 6. Test with 2^5 times..



From simulation results above, it is clear that the low-resolution DAC signal source of the system can measure more and more ADC digital codes by increasing the number of repeating test. However, part of the center codes can not be measured, which is consistent with the system expectation. According to the fourth step, it need to add a bias voltage, which is one third of the ADC full scale on the basis of the simulation result. The system should work again with the left 2^6 test number. At the same time, we must calculate the tested number of the ADC codes.

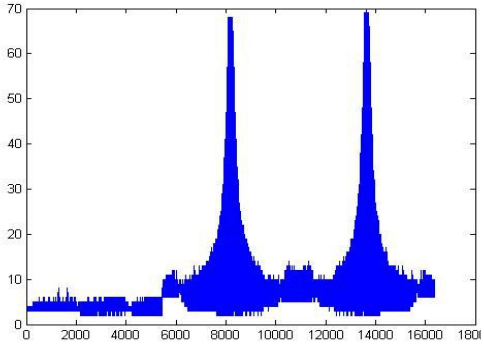


Fig. 8. Test with the left 2^6 times..

From the Fig.8, the general simulation result shows that 10-bit DAC signal source of this system can measure each code of 14-bit ADC twice at least, and most of the codes are even measured by over 10 times. All the improvement and steps fit regulations of the proposed automated digital testing system.

V. CONCLUSIONS

An automated digital testing system for high-resolution ADC using low-resolution DAC signal source is discussed in this work. The system preserves the beneficiary characteristic of the original feedback loop testing system that utilizes easy-to-generate signals in ADC test, and add some complimentary parts, especially a reference voltage source controlled by a variable resistance circuit structure and the certain number of repeating test based on theoretical reduction. Details of the proposed testing system are discussed in the paper and the performance of the testing system is validated in simulation part. The simulation results show that by the digital potentiometer constantly fine-tuning the reference voltage and joining a bias voltage timely, the 10-bit DAC signal source owns the ability to measure each code of 14-bit ADC twice at least, which is equivalent to increasing the resolution of DAC. And there are no limits to ADC of architectures. Since the hardware design and computational complexity of the system is not very hard, it can be applied in many experimental environment, which greatly reduce the testing costs.

VI. ACKNOWLEDGMENT

This work was supported by National Science and Technology Major Project (No. 2013ZX03001011-003).

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