20th IMEKO TC4 International Symposium and
18th International Workshop on ADC Modelling and Testing
Research on Electric and Electronic Measurement for the Economic Upturn
Benevento, Italy, September 15-17, 2014

Advanced experimental setup for reliability and current consumption measurements of Flash non-volatile memories

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***Abstract* – In this paper we present a new experimental setup that enables static, dynamic and high voltage electrical characterization for the Flash memory cell. Using an Agilent B1500 parameter analyzer and its embedded modules we minimized the effects of the parasitic connection between different instruments. The current consumption of a memory cell is generally measured using a current/voltage converter or the Floating Gate technique. Our setup is able to measure dynamically the current consumption with a sampling time of several nanoseconds during a hot carrier injection. Moreover we can evaluate the degradation of memory cell performances including endurance test, and its impact on the cell memory consumption. Our method is implemented to test 90nm technology node Flash memories, but it can also be used for future ultra-scaled technologies. Moreover we propose to use our technique to demonstrate the dependence of drain current consumption on the defects generation due to the endurance degradation. In conclusion we implemented this original and flexible method to better understand the Flash memory behavior for advanced embedded and low energy applications.**

I. INTRODUCTION

Today the market of Flash non-volatile memories is expanding due to the increasing number of portable devices and SoC applications. All these applications demand higher performances such as: high density, low power consumption, short access time, low costs, and so on [1, 2]. In this paper we focus on the current consumption characterization of Flash floating gate NOR memory [3, 4]. The nonvolatile memory devices based on this technology require high voltage (4V up to 10V) to operate due to the fundamental nature of cells and the physics of charge storage mechanisms. These are overvoltage requirements considering that the transistors in the logic block need substantially lower voltages. In [3] a study on the importance of single cell energy consumption is presented. The program and the erase operations, of floating gate cells, are directed by the physic mechanisms that dictate the voltage, current, and speed operations. Moreover many special operational blocks are required to deliver the operating conditions including high-voltage charge pumps, decoders and sense amplifiers that contribute to overall power and energy dissipation during operation of the device. Typically, for flash memory designs, high-voltage and high current pumps achieve an efficiency of about 33%; while high-voltage and low current pumps achieve an efficiency of about 66% [3].

In general the drain current consumption of a Flash floating gate memory cell is estimated using a complex experimental setup (current/voltage converter) [5-7] or with the Floating Gate (F.G.) technique [8-10]. In this way it is not possible to understand the dynamic cell behavior and to measure the cell performances in a NOR architecture for a programming pulse of several microseconds. Moreover, the F.G. method, is difficult to implement for the discrete charge trapping memories (silicon nanocrystal, SONOS, TANOS). In this context we developed a new experimental setup in order to measure the current consumption during a channel hot electron programming operation, switching between static, dynamic and endurance experiments. These measurements are combined with the data retention experiments. Some experimental results, published in literature, confirming the validity of the technique, are reported for the 1T Flash Floating Gate [4], 1T silicon nanocrystal [11], and 1.5 Split Gate memories [12]. The method is thus general and independent on the cell architecture and size. To our knowledge no results exist in literature concerning the cell energy consumption after 1M program/erase operations, and its degradation during the cycling. Furthermore we propose to use the dynamic measurement to relate the charge trapping/detrapping to the cell current consumption. This study enables a control of memory cell parameters degradation during the aging. As a consequence, it will be possible to implement specific algorithms for SoC applications, in order to improve the memory cell performances and to reduce the energy consumption, waiting for the future emerging nonvolatile memories.

ISBN-14: 978-92-990073-2-7

II. TECHNICAL DETAILS

A. Sample description

The samples used in this work are Flash floating gate memory cells integrated on 200mm wafers (90nm technology node). The length of the cells is 190nm and the width is 80nm, while the SiO_2 tunnel oxide thickness is 10nm, and it is grown on a Si p-type substrate. In figure 1a we reported a cross section TEM (Transmission Electron Microscopy) picture of width dimension, and in figure 1b a schematic of a tested cell. The devices have been realized by STMicroelectronics (Rousset, France).

B. State of the art of current consumption measurements

Today one of the most important challenges for embedded Flash floating gate memories in view of low power applications is to minimize the current consumption during the Channel Hot Electron (CHE) programming operation. A specific current consumption characterization technique is presented in the literature, but requires a complex measurement setup, limited by circuit time constants [5, 13]. The development of the system cited in [5] introduces some errors on measured results due to the variability of IV converter and the coupling between the latter and the scope. In order to measure the current absorption using ramped gate programming, the setup was improved in [13] but the complexity of the system limits the current measurement sensibility and the programming pulse duration. Today the memories for embedded NOR architectures consume a current magnitude of the order of 100 microamperes for shorter time periods (several microseconds).

As an alternative to the direct measurement on floating gate cell, it is possible to calculate the static current consumption during the programming operation starting from the drain current measurement on the equivalent transistor (called dummy cell) [8, 14, 15]. This technique enables the consumption to be calculated, regardless of the programming time, by using a commercial electrical parameter analyzer, while the current is considered to be constant during the programming. This procedure introduces a significant error due to the spread of dummy cell parameters; moreover the energy consumption is overestimated with respect to the real conditions.

C. New experimental setup

Considering the other methods for the current consumption estimation, we propose a new experimental technique in order to measure the drain current during the CHE programming operation by using pulses of 1µs with a sampling time of 10ns. The schematic of our setup is shown in figure 2, where we represent the Agilent B1500 equipped by 3 WGFMUs (Waveform Generator Fast Measurement Unit, Agilent B1530A), 2 SPGUs (Semiconductor Pulse Generator Unit) and 4 SMUs (Source Monitor Unit).

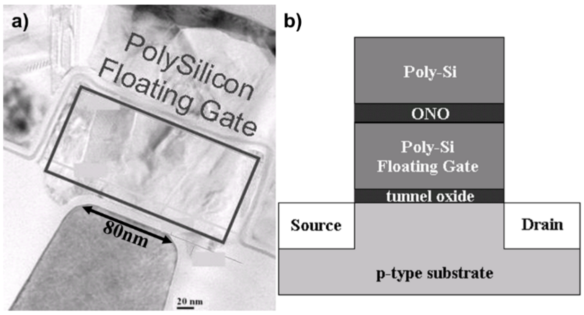

Fig. 1. a) TEM (Transmission Electron Microscopy) picture of Flash floating gate (width cross section). b) Schematic of tested cell.

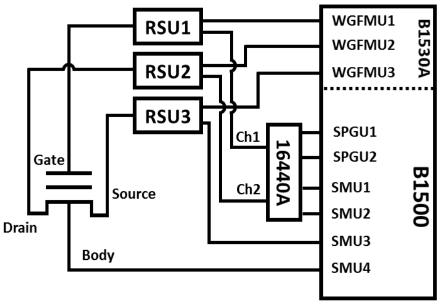

Fig. 2. Schematic of complete experimental setup

Thanks to the 16440A selector the switching between SMUs and SPGUs is thus possible without using a standard switching matrix that, with the connections and cables, can introduce parasitic elements. In series, we connected the RSU (Remote-sense and Switch Unit) modules that enable the link with the probes and the DUT (Device Under Test), because they are normally on SMU position. In the case of current consumption measurements they switch in WGFMU position enabling the fast pulse generation. A detailed description of this switching module is presented in [16]. This module activates the path for signals coming from SMU or SPGU, and in alternative the dynamic measurements performed by the WGFMU modules. In this last case the connection between the B1530 and the DUT is fully adapted and no parasitic connections are present.

In figure 3 we show the connection of the RSU modules with the probes made with the SMA-SSMC cables that enable the shortest connection path to be obtained and thus the minimum parasitic effect [17]. In the case of current consumption measurements it is possible to measure currents with a minimum range of 1µA and a sampling time of 10ns. This makes it possible to study in particular the memory dynamic behavior, thus the current and then the energy consumption during the CHE programming operation. In this paper we present the experimental protocol to perform: Id-Vg (drain current-gate voltage) static characterization to read the memory programmed/erased threshold voltages (Vt_{PR}/Vt_{ER}), programming kinetics, current consumption and reliability experiments (endurance and data retention).

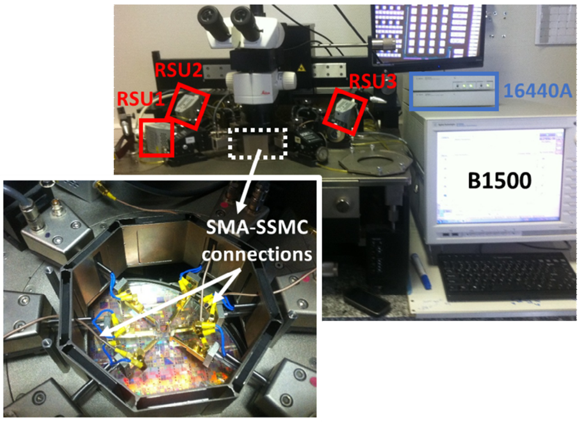

Fig. 3. Picture of experimental setup and its connections

D. Experimental protocol

In figure 4 we represent the test sequence used to characterize the dependence of drain current consumption on endurance degradation. Furthermore we repeat the experiments after a bake period at 150°C to show the cell behavior after the charge detrapping. The memory cell was programmed with different modules, but always by channel hot electron and under the same conditions: gate voltage (Vg) of 9V; drain voltage (Vd) of 4.2V and a programming time (tp) of 1µs. While the erase operation was performed by Fowler-Nordheim using: Vg=-18.5V and te=300µs (erase time) during the cycling.

Also an intelligent erase technique was used to reach a defined Vt_{ER} depending on the type of test. At the beginning of cycling we measured a Vt_{PR}=8V and a Vt_{ER}=2.3V, that correspond to a programming window (ΔVt) of 5.7V. The threshold voltage (Vt) of the memory cell was extracted from Id-Vg characteristics for a fixed drain current, Id=10µA.

III. EXPERIMENTAL RESULTS

In figure 5 we plot the endurance characteristic of a tested cell using the program/erase pulses described above. We cycled the device up to 1Mcycles in order to show the programming window degradation that is 5.7V at the beginning of the test and decreases down to 1.4V at the end. We stopped the endurance test after 1,10k, 100k and 1M cycles in order to characterize the DUT. In figure 6a the programming window kinetics are represented. One can note the degradation of the programming window, thus the programming efficiency. This is due to the electron parasitic charge trapping in the tunnel oxide; these charges increase the tunneling barrier, in particular on the drain zone where the hot electrons are generated to be injected in the floating gate.

We measured the drain current consumption during the channel hot electron operation (figure 6b), by using the WGFMU module, after degradation. These results are published for the first time to our knowledge, showing how the consumption increases during the cycling.

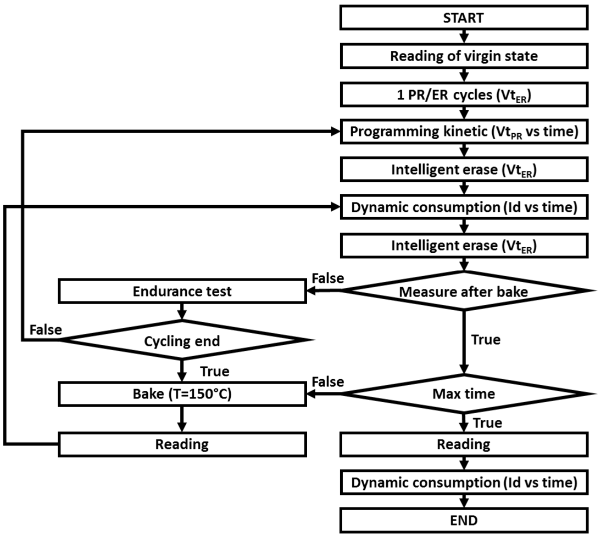

Fig. 4. Flowchart of experimental sequence

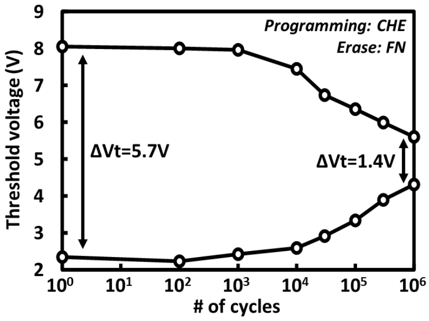

Fig. 5. Endurance characteristic of tested cell. CHE programming (Vg=9V; Vd=4.2V; tp=1µs), FN erase (Vg=-18.5V; te=300µs).

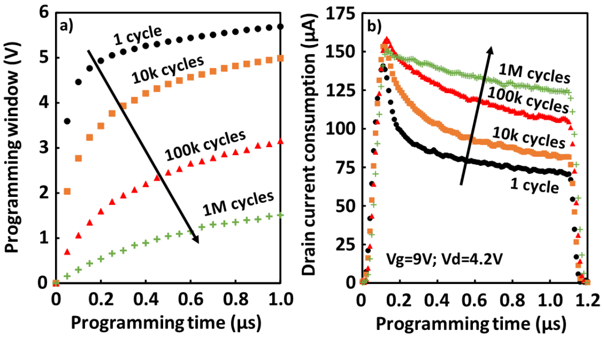

Fig. 6. a) Programming kinetic and b) current consumption characteristics evolution during the cycling.

The drain current gradually decreases, during the programming pulse, when the cell degradation is increased. This is due to the decreased programming efficiency and thus to the slow floating gate potential variation during the hot carrier operation. In order to demonstrate the dependence of current consumption increase, on the presence of parasitic charge trapping in the tunnel oxide, we performed a data retention test after cycling at 150°C.

The Id-Vg characteristics were carried out at room temperature to extrapolate the threshold voltage evolution over time; we reported the results in figure 7a. A sudden charge loss is present; this is due to the variation of the Id-Vg subthreshold slope and the interfacial defects relaxation after 1h in the bake (figure 7b). After this initial effect a rigid shift of the Id-Vg characteristic was measured as a consequence of a deep charge loss present in the tunnel oxide or at the interfaces.

The parasitic charge trapping close to the drain, produces a decrease in injection efficiency by increasing the tunnel barrier, hence dynamically, the floating gate potential weakly decreases during the programming, increasing the current consumption and thus the energy. The energy consumption (Ec) during a channel hot electron programming operation can be calculated as follows:

$$Ec = \int_{0}^{t_p} Vd \cdot Id \cdot dt \qquad (1)$$

In figure 8a we represent the consumed energy before and after cycling experiments, and also after a bake of 68h and 118h at 150°C. We note that the energy consumption decreases as the threshold voltage shifts during the data retention test. The dynamic measurements were performed after the current voltage characteristics of figure 7b. The dependence of energy consumption on the parasitic charge trapping is finally experimentally demonstrated in figure 8b. Here we represent the increase in the current consumption after 1M program/erase cycles, caused by the charge trapping in the drain region. Moreover we show that after a bake period at 150°C the consumption decreases as the threshold voltage shifts. The charge loss activated by the high temperature enables a drain current reduction toward the initial state of fresh cell. Further measurements at different temperatures enable the extrapolation of the consumption recovering activation energy.

IV. CONCLUSIONS

In this paper we presented a new experimental setup to perform advanced electrical characterizations on Flash nonvolatile memories. We propose a new technique in order to measure the dynamic drain current during the CHE programming operation by using pulses of 1µs with a sampling time of 10ns. Thanks to the Agilent B1500 equipment the effects due to the interconnection were reduced. This kind of measure has been integrated in a specific protocol to switch between static, dynamic and endurance tests. The versatility of our system will enable the characterization of the future ultra-scaled technology nodes. Moreover we present here the results of current consumption increase depending on the number of program/erase cycles. We demonstrate that the parasitic charge trapping enables a decrease in injection efficiency by increasing the tunnel barrier.

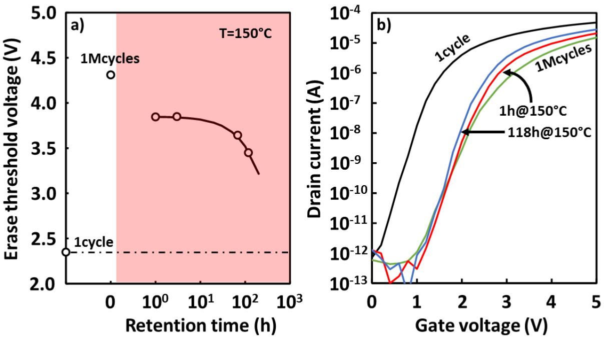

Fig. 7. a) Erase threshold voltage evolution at 150°C after cycling and b) Id-Vg characteristics used for the Vt_{ER} extraction at Id=10µA.

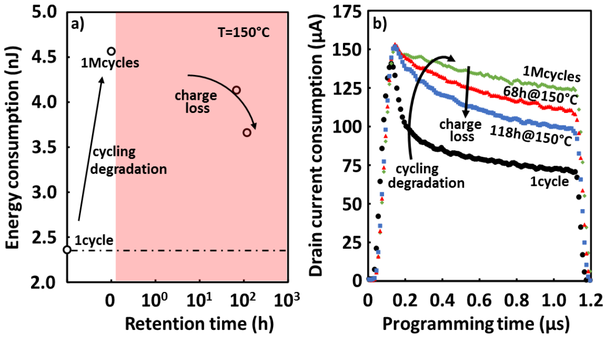

Fig. 8. a) Energy consumption evolution during the bake period, after cycling and b) drain current dependence on endurance and charge loss.

Hence, dynamically, the floating gate potential slightly increases during the programming operation by increasing the energy consumption. Finally for the first time to our knowledge we present the impact of cycling and the charge trapping/detrapping on the dynamic drain current and thus the energy consumption. After the endurance stress, the Flash floating gate memory has a tendency to return to the initial energy consumption condition, because of the defects relaxation at 150°C. When performing the same tests at different temperatures it will be possible to extrapolate the activation energy of this effect and associate it with the threshold voltage shift at high temperature, thus the charge trapping in the tunnel oxide.

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