20th IMEKO TC4 International Symposium and
18th International Workshop on ADC Modelling and Testing
Research on Electric and Electronic Measurement for the Economic Upturn
Benevento, Italy, September 15-17, 2014

Performance and Information Characteristics of Optimized Flash and Adaptive Cyclic A/D Converters

Anatoliy Platonov, Konrad Jędrzejewski

Institute of Electronic Systems,
Faculty of Electronics and Information Technology,
Warsaw University of Technology,
15/19 Nowowiejska Street, 00-665 Warsaw, Poland,
e-mails: plat@ise,pw.edu.pl; Konrad.Jedrzejewski@ise.pw.edu.pl

***Abstract* – The paper presents the results of studies on the performance of flash analog-to-digital converters (ADC) and adaptive cyclic ADC (AC ADC), their information characteristics and probability of saturation. Currently, these parameters are not used as the performance criteria in A/D conversion theory and applications, and their introduction would extend possibilities of designing both ADCs and utilizing them systems. There is also presented original approach to the improvement of ADCs performance under additional condition guaranteeing that probability of their saturation does not exceed a given confidence level.**

I. INTRODUCTION

The first signal processing units of every modern communication system (CS) transmitting the signals from the analog sources are ADCs. The provided by them speed of conversion, resolution and level of conversion errors determine the upper boundaries of performance of digital CS and other digital systems processing analog signals. This makes ADCs the core element of high quality analog-digital systems and the subject of active search of new concepts, technical and technological solutions improving ADC performance. The result is appearance of quickly growing number of different versions of the converters, and growing number of the parameters describing their performance [1], [2].

Nowadays, the set of these parameters does not include information characteristics of ADC. However, information rate [bit/s] at the ADC output is an important parameter in design of many systems, especially, of CS transmitting the analog signals. It is evident that amount of information delivered by CS to addressee per second [bit/s] cannot be greater than amount of information generated per second by ADC. This means that information rate of ADC determines the capacity of communication channels necessary for the accurate and reliable transmission of the signal codes. Known information rate of ADC also permits to transmit the signals using less complex channels or optimally utilizing resources of high speed channels.

In the paper, information and accuracy characteristics of the flash ADCs and AC ADCs are considered. The research develops the results of earlier works [3]-[6] in optimization of AC ADCs where information characteristics of the converters were also studied. The particularity of the research is consideration of possible saturation of the converters. In this aim, we employ the developed in [7], [8] general approach to optimization of the adaptive estimation, measurement and communication systems with feedback [8]-[10]. Optimization is carried out under additional condition that the parameters of their input analog units have the values excluding saturation errors at the given confidence level.

The paper shows practical methods of saturation exclusion and correct analytical optimization of the converters approaching their performance and information rate to the theoretical bounds. In Sect. II, this task is solved for the flash ADC. In Sect. III, we describe the complex of conditions permitting to solve this task for AC ADC and creating the effects unachievable in conventional cyclic ADC (CADC). Final discussion is given in Sect. IV.

II. INFORMATION RATE, MSE OF CONVERSION, AND CAPACITY OF FLASH ADC

Below, we assume that the signal V_t at the input of the ideal *N*-bit flash ADC is stationary Gaussian process with the zero mean and variance σ_V^2, and its realization can be presented by the sequence of samples $V^{(m)} = V(mT)$, $(m = 1, 2, ...)$ where $T = 1/2F$ is the sampling period, and F is the baseband of the input signal. It is assumed that each sample $V^{(m)}$ is converted independently. In this case, analysis of ADC functioning can be reduced to the

ISBN-14: 978-92-990073-2-7

analysis of a single sample conversion that permits to omit indexing of the samples in the further analysis. The samples are routed to the quantizer (block of comparators with quantization levels uniformly spread in the interval of voltages $[-D, D]$) and dividing it into 2^N quantization levels Δ, each of the length

$$\Delta = \frac{2D}{2^N} = D \cdot 2^{-(N-1)} \ . \quad (1)$$

The *N*-bit flash ADC converts the samples V of the input signal into the corresponding *N*-bit codes $S^{(i)}$. The set $\Omega_V = [-D, D]$ of input signals is continuous, and the set Ω_S of 2^N code words (code bins) $S^{(i)}$ is discrete. We assume that, under given full scale range (FSR) $[-D, D]$ of the quantizer, each code $S^{(i)}$ permits to recover (e.g. using D/A converter) its analog equivalent $\hat{V}^{(i)} \in \Omega_{\hat{V}}$ where $\Omega_{\hat{V}}$ is the discrete subset of the set $\Omega_V = [-D, D]$. Distances between the adjacent points $\hat{V}^{(i)}$ are constant and equal to Δ. This permits to express the conversion errors in the variables belonging to the same set Ω_s:

$$\xi^{(i)} = V - \hat{V}^{(i)} \ \text{ and } \ V = \hat{V}^{(i)} + \xi^{(i)} . \quad (2)$$

Formula (2) enables analytically correct formulation of the mean square error (MSE) of conversion:

$$P = E\{[V - \hat{V}^{(i)}]^2\} = E[(\xi^{(i)})^2] \ . \quad (3)$$

For ADC (quantizer) with sufficiently large number of comparators 2^N, Δ is small. In this case, conversion errors $\xi^{(i)}$ can be considered [2],[11] as random values uniformly distributed in the interval $[-\Delta/2, \Delta/2]$ independently from the number of quant. Then, the power of quantization noise (MSE of conversion) takes the value:

$$P = E[(\xi^{(i)})^2] = \frac{\Delta^2}{12} = \frac{D^2}{3} \cdot 2^{-2N} \ . \quad (4)$$

A. Optimal exclusion of flash ADC saturation

The step-wise characteristic of quantizer is not a single source of the conversion errors. The other and much less investigated source of errors is always limited FSR of ADCs – the source of their possible saturation. Each case of ADC saturation causes a full loss of information about the value of the input sample. Even if saturation appears rarely, e.g. with a probability $\mu < 10^{-4}$ per sample, it causes appearance, in average, of μ percent of erroneous codes $S^{(i)}$ (word error rate - WER) in the sequences of codes formed by the converter. On the other hand, WER μ is numerically equal to the percent of erroneous bits in these sequences. Thus, saturation causes the errors similar to the bit error rate (BER) – one of the basic measures of digital CS (DCS) performance. These errors may substantially increase BER of DCSs and should be counted in evaluations of their real performance. Importance of the problem was stressed by many authors, (e.g. [11], p. 13.2.3: "saturation noise is more dangerous than quantization noise").

Nowadays, input range [-*D*, *D*] of ADC is established by the standards or manufacturers regardless of distribution of the converted signals. To exclude saturation, users assess the mean value and variance σ_V^2 of the input signals and choose corresponding ADC "with a reserve", i.e. with FSR wider than necessary. However, such a choice decreases the number of comparators directly participating in the conversion and, as the result, increases MSE and decreases the real (effective) resolution of ADC. We did not find in the literature analytical recommendations for optimal utilization of FSR and below we employ the original approach based on the approach proposed in [7],[8]. One should stress that solution of this task is possible only if the prior distribution $p(V)$ of the signal values can be assessed.

Let us place, before the quantizer with FSR $[-D, D]$, a linear pre-amplifier with the gain G. Then, the signal routed to the comparators has the value $y = GV$, and ADC will be saturated, if $|y| > D$. Under known distribution $p(V)$ of the samples values one can easily assess a probability of this event:

$$\mathrm{P}^{sat} = \Pr(|y| \geq D) = 1 - \int_{-D/G}^{D/G} p(V) dV = \\ = 1 - \frac{1}{\sigma_V \sqrt{2\pi}} \int_{-D/G}^{D/G} \exp\left\{-\frac{V^2}{2\sigma_V^2}\right\} dV . \quad (5)$$

Saturation of ADC (of the quantizer) will be excluded at the confidence level 1-μ, if the gain *G* has the "permissible" value guaranteeing that probability of the sample saturation will be less than a given small value μ: $\mathrm{P}^{sat} < \mu$, (in applications $\mu \leq 10^{-4}$). Using in (5) a new variable $z = \sigma_V V$, this condition ("statistical fitting condition" [7], [8]), can be written in the form:

$$1 - \frac{2}{\sqrt{2\pi}} \int_0^{\alpha} \exp\left\{-\frac{z^2}{2}\right\} dz = 1 - 2\Phi(\alpha) < \mu , \quad (6)$$

where $\Phi(\alpha)$ is tabular Gaussian function, and saturation factor $\alpha = D / G\sigma_V$. Inequality (6) determines the set $\Omega_\alpha = [\alpha_\mu, \infty)$ of permissible values α which guarantee elimination of saturation at the confidence level not smaller than $1 - \mu$. The set of permissible values α has the low boundary: $\Omega_\alpha = [\alpha_\mu, \infty)$, where α_μ is solution of the equation $\Phi(a) = (1 - \mu) / 2$.

Dependence $\alpha = D / G\sigma_V$ and inequality $\alpha \geq \alpha_\mu$ determine the set of permissible gains of preamplifier Ω_G:

$$G \leq G_\mu = \frac{D}{\alpha_\mu \sigma_V} . \quad (7)$$

Pre-amplifier transforms the initial FSR of ADC to the permissible one determined by formulas $y = GV$ and (7)

$$[-D_1, D_1] = [-D/G, D/G] = [-\alpha\sigma_V, \alpha\sigma_V] . \quad (8)$$

B. Minimal MSE of conversion

For the gains (7) and FSR (8), MSE of conversion is determined by formula (4) where FSR 2*D* is replaced by $2D_1 = 2\alpha\sigma_V$. According to (4), the smaller FSR, the smaller MSE. Taking into account that $\alpha \geq \alpha_\mu$, minimal MSE (MMSE) of conversion P_μ for ADC with pre-amplifier fitted to the signal attains the value:

$$P_\mu = \frac{D_\mu^2}{3} \cdot 2^{-2N} = \frac{\alpha_\mu^2 \sigma_V^2}{3} \cdot 2^{-2N}, \quad (9)$$

where optimal FSR of ADC and the gain of pre-amplifier have the values:

$$FSR_\mu = 2D_\mu = 2\alpha_\mu \sigma_V \ , \ G_\mu = D/\alpha_\mu \sigma_V . \quad (10)$$

Further, ADCs satisfying these conditions are called *optimally fitted to the signals with the given variance* σ_V^2 or, briefly, optimally fitted ADCs.

All the samples $\tilde{V}$ of the signals with the variance $\sigma_{\tilde{V}}^2 < \sigma_V^2$ will be converted by the optimally fitted ADCs without saturation at the granted confidence level $1-\mu$ per sample. However, these signals will activate only comparators with switching voltages placed within interval $[-\alpha\sigma_{\tilde{V}}, \alpha\sigma_{\tilde{V}}]$. All the other comparators will be excluded from the conversion with a probability not less than $1-\mu$. This means practical reduction of the number of active comparators and ADC resolution by $\gamma = \sigma_{\tilde{V}} / \sigma_V$ times. In turn, conversion of the signals more powerful than σ_V increases WER up to the values greater than the permissible level μ. It permits to conclude:

Claim 1. Under given μ and *D*, full utilization of the resources of optimally fitted ADC can be achieved only if the parameter σ_V determining the gain of pre-amplifier is equal to the standard deviation of the input signal.

In practice, this can be done using pre-amplifiers with the gain $G_\mu = D/\alpha_\mu \sigma_V$ adjusted using the preliminary measured values σ_V or using automatic gain control. The adaptive adjusting can be used also.

Remark 1. Direct comparison of MSE (4) and (9) is not correct: formula (4) is derived under implicit assumption that the converted signals never cross the boundaries [-*D*, *D*], while (9) takes into account distribution of the input signals and possible saturation of ADC (see also p. II.C).

C. *Information rate of optimally fitted flash ADC*

Let ADC is optimally fitted to the Gaussian signals with the variance σ_V^2, FSR ADC is $2D_\mu = 2\alpha_\mu \sigma_V$ and $G_\mu = D/\alpha_\mu \sigma_V$. The mean amount of information $I(V,\hat{V})$ in the codes $\hat{V}^{(k)}$ of the samples about their values V can be evaluated in different ways. The simplest one is a computation of $I(V,\hat{V})$ using the relationship:

$$I(V,\hat{V}) = H(V) - H(V \mid \hat{V}), \quad (11)$$

where $H(V)$, $H(V \mid \hat{V})$ are the prior and posterior entropies (one should stress that entropies are the functionals of distributions $p(V \mid \hat{V}^{(i)})$, $p(\hat{V}^{(i)})$, and values V, $\hat{V}$ in (11) are not the arguments but only indicators of the sets Ω_V, $\Omega_{\hat{V}}$). The particularity of $I(V,\hat{V})$ (11) is that, unlike the continuous set $\Omega_V = [-D_\mu, D_\mu]$, set $\Omega_{\hat{V}}$ is discrete, and expression for the posterior entropy $H(\hat{V} \mid V)$ is to be written in the form:

$$H(V \mid \hat{V}) = -\int_{-D_\mu}^{D_\mu} \sum_{i=1}^{2^N} p(V,\hat{V}^{(i)}) \log_2 p(V \mid \hat{V}^{(i)}) \, dV. \quad (12)$$

Taking into account the uniform distribution of quantization noise and formula (2), one may conclude that

$$p(V \mid \hat{V}^{(i)}) = p(\xi^{(i)}) = \\ = \frac{1}{\Delta_\mu} \begin{cases} 1 & \text{for } |V - \hat{V}^{(i)}| \leq \Delta_\mu/2 \\ 0 & \text{for } |V - \hat{V}^{(i)}| > \Delta_\mu/2 \end{cases} \quad (13)$$

where $\Delta_\mu = 2D_\mu 2^{-N}$. Substitution of (13) to (12) gives:

$$H(V \mid \hat{V}) = -\sum_{i=1}^{2^N} p(\hat{V}^{(i)}) \int_{-D_\mu}^{D_\mu} p(V \mid \hat{V}^{(i)}) \log_2 p(V \mid \hat{V}^{(i)}) dV = \\ = \frac{1}{\Delta_\mu} \sum_{i=1}^{2^N} p(\hat{V}^{(i)}) \int_{\hat{V}^{(i)}-\Delta_\mu/2}^{\hat{V}^{(i)}+\Delta_\mu/2} \log_2 \Delta_\mu dV = \log_2 \Delta_\mu . \quad (14)$$

In turn, the prior entropy $H(V)$ of the converted signals is to be computed on the finite set $V \in \Omega_V^{fin} = [-D_\mu, D_\mu]$. According to the results of point II.A, extension of the input range of the statistically fitted ADCs to $[-\infty, \infty]$ may increase a probability of saturation to the values not greater of μ. In this case, prior entropy is determined by known formula [12]:

$$H(V) = 1/2 \cdot \log_2(2\pi e \sigma_V^2) \quad (15)$$

This value may differ from the entropy computed on the interval $[-D_\mu, D_\mu]$ by the negligibly small terms of $O(\mu)$ order. Substitution of (14),(15) to (11) gives the following relationship:

$$I(V,\hat{V}) = \frac{1}{2} \log_2 \left(\frac{2\pi e \sigma_V^2}{\Delta_\mu^2} \right) = N^{eff} \text{ [bit/sample]}, \quad (16)$$

which determines the effective (real) resolution N^{eff} of the converter. Then, information rate at the ADC output $R = 2FI(V,\hat{V})$ [bit/s] is determined by the formula:

$$R = F \log_2 \left(\frac{2\pi e \sigma_V^2}{\Delta_\mu^2} \right) = 2F \left[N + \frac{1}{2} \log_2 \left(\frac{\pi e \sigma_V^2}{2D_\mu^2} \right) \right] = \\ = 2F \left[N + \frac{1}{2} \log_2 \left(\frac{\pi e}{2\alpha_\mu^2} \right) \right] = 2FN^{eff} . \quad (17)$$

Formulas (16), (17) determine maximal effective resolution and information rate for flash ADCs optimally fitted to the Gaussian signals with the variance σ_V^2, and saturation eliminated at the confidence level $1-\mu$.

D. *Capacity of flash ADC*

In [3], [8], also in [13], it is noted that every ADC can be considered as a special case of communication channel with the capacity determined by the relationship:

$$C = \frac{1}{T} \max_{p(x)} I(V,\hat{V}) = 2F \max_{p(x)} [H(V) - H(V \mid \hat{V})] = \\ = 2F [\max_{p(x)} H(V) - \log_2 \Delta]. \quad (18)$$

As it was mentioned above, technical documentation for ADCs determines their (comparators') FSR $[-D, D]$ without any connection with distribution of the input signals. It is known [12] that, if no other information is given, distribution maximizing the entropy $H(V)$ at the interval $[-D, D]$ is uniform and $H_{\max}(V) = \log_2(2D)$. This and formula (18) allow us to formulate the claim:

Claim 2. If only FSR $[-D, D]$ of the flash ADC is known, maximal amount of information in the codes $S^{(i)}$ of the samples about their values V, and capacity of ADC are determined, respectively, by the relationships:

$$I_{\max}(V, \hat{V}) = \log_2 \frac{2D}{\Delta} = N \text{ [bit/sample]}, \qquad (19)$$

$$C = 2FN \text{ [bit/s]}. \qquad (20)$$

Remark 2. None real signal has uniform distribution. For this cause, users evaluate the mean value and variance of the input signals. However, if these parameters are known, distribution of the signals which maximizes entropy $H(V)$ is Gaussian [12]. This proves that (16), (17) determine upper boundaries of the effective resolution and information rate of the statistically fitted ADC. Nevertheless, these values are always smaller than (19), (20).

III. INFORMATION CHARACTERISTICS OF AC ADC

The block diagram of adaptive cyclic (AC) ADC is presented in Fig.1. As in Sect. II, input signals are Gaussian with the zero mean and variance σ_V^2. Each sample V is formed by the sample and hold (S&H) unit and held at the input of a subtractor Σ during the time $T = 1/2F$ sufficient for realization of *n c*ycles of conversion, each of duration $\Delta t_0 = T/n$. In the sequential cycles, all the adjusted parameters of AC ADC are set to the new values.

A. General scheme of AC ADC functioning

Unlike known cyclic ADC (CADC), digital part of AC ADC is realized as the application-specific digital circuit. This unit computes estimates $\hat{V}_k$ of the sample ($k = 1, \dots, n$) in the form of N_S - bit words, and N_S is by 3-5 bits greater than the expected resolution of the converter. The digital circuit includes the store unit (ROM in Fig. 1) which stores, during the time Δt_0, the code $\hat{V}_{k-1}$ of the previous estimate cyclically replaced by the next computed estimate. It also stores the set of independently computed values G_k, L_k used for setting the parameters of pre-amplifier A and digital multiplier M. This unit computes the product $L_k \tilde{y}_k$ of N_S - bit coefficient L_k and digital signal $\tilde{y}_k$ formed by coarse ($N_{ADC} \sim 4 \div 6$ bit) A/D converter ADC$_{\text{In}}$ at the output of the analog part. In each cycle, estimate $\hat{V}_k$ is computed in the adder (Ad in Fig. 1) according to the equation [3]-[6]:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k \qquad (k = 1, \dots, n). \qquad (21)$$

Each *k*-th cycle of conversion begins from the setting the gains of pre-amplifier A and multiplier M to the values

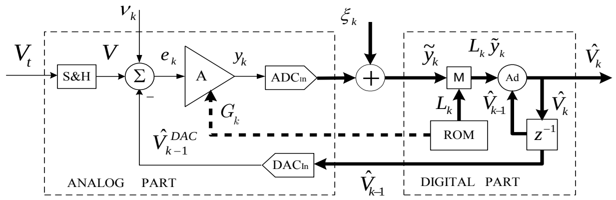

Fig. 1. The block diagram of AC ADC.

G_k, L_k. Next, the subtractor Σ forms the difference signal $e_k = V - \hat{V}_{k-1}^{DAC}$ amplified by the pre-amplifier A, where $\hat{V}_{k-1}^{DAC}$ is an analog equivalent of the estimate $\hat{V}_{k-1}$ formed by the high quality feedback converter DAC$_{\text{In}}$ ($N_{DAC} \geq 10$ bit). The amplified signal $y_k = G_k e_k$ is routed to the input of the coarse ADC$_{\text{In}}$ with the input range $[-D, D]$. The converted value $\tilde{y}_k$ is processed in the digital part according to (21), new estimate $\hat{V}_k$ is routed to the store unit ROM and to the input of DAC$_{\text{In}}$. The formed by DAC$_{\text{In}}$ new value $\hat{V}_k^{DAC}$ is routed to the second input of the subtractor Σ. Simultaneously, a synchronizing unit sets the gains L_k, G_k to the values L_{k+1}, G_{k+1}, and the next cycle of conversion begins.

B. Qualitative differences between AC ADC and CADC

Transition to computation of estimates $\hat{V}_k$ in the form of long-bit ($N_S \sim 20 \div 24$ bit) digital words allows their description, with high accuracy, by the continuous variables. This permits to analyze AC ADCs using conventional tools of continuous mathematics and to optimize them using methods of optimal estimation theory. Similarly to Sect. II, errors ν_k at the output of DAC$_{\text{In}}$ are considered as the analog noise added to the analog equivalent of digital estimates $\hat{V}_k$ routed to the input of DAC$_{\text{In}}$:

$$\hat{V}_k^{DAC} = \hat{V}_k + \nu_k, \quad (k = 1, \dots, n). \qquad (22)$$

The variance σ_ν^2 of the feedback errors ν_k depends on the truncation (round-off) errors of DAC$_{\text{In}}$, EM noises of other elements and on the external noises. Formula (22) permits us to write the difference signal e_k in the form:

$$e_k = V - \hat{V}_{k-1}^{DAC} = V - \hat{V}_{k-1} + \nu_k. \qquad (23)$$

The amplified signal $y_k = G_k e_k$ is routed to ADC$_{\text{In}}$, and the signal $\tilde{y}_k$ at its output can be presented in the form:

$$\tilde{y}_k = G_k e_k + \xi_k = G_k (V - \hat{V}_{k-1} + \nu_k) + \xi_k, \qquad (24)$$

where ξ_k is the quantization noise of ADC$_{\text{In}}$. Formulas (21), (22)-(24) potentially enable analysis of AC ADC functioning during all cycles of the sample conversion.

Similar relationships can be formally written for the conventional cyclic ADCs (CADCs). However, all CADCs form the estimates $\hat{V}_k$ by shifting and adding the low-bit code words $\tilde{y}_k$ formed by ADC$_{\text{In}}$ [2]. Therefore, the length of the codes $\hat{V}_k$ (in bits) grows in sequential cycles $k = 1, \dots, n$. Moreover, in CADC, gains L_k, G_k have always discrete values proportional to $2^{kN_{ADC}}$. Thus, for CADC, formulas (21)-(24) have only illustrative value and cannot be used for derivation of analytical results.

Transition to computation of estimates in the form of long-bit words removes these constraints. The only difficulty in AC ADC analysis is the non-Gaussian distribution of the noises ξ_k, ν_k.

C. Optimization of AC ADC

Relationships (21)-(24) permit to formulate MSE $P_k = E[(V-\hat{V}_k)^2]$ as the function of continuous parameters L_k, G_k. The latter permits us to find values L_k, G_k which minimize MSE P_k for each cycle $k=1,...,n$.

Similar task, employing similar models, had been studied in the cycle of researches of the 1950-1979s devoted to optimization of the analog feedback communication systems (AFCS) designated to iterative transmission of the analog signals. These researches were ceased in the midst of 70s - omission of saturation effects in the forward transmitters made excellent analytical results inapplicable (see also [10]).

In our research in AFCS optimization ([10] and earlier works), this problem was removed by application of the similar to (5) statistical fitting condition considered as the additional condition in solution of the optimization task. The obtained solution determines the parameters of the analog (transmitting) and digital (receiving) parts of AFCS minimizing MSE P_k for each cycle of transmission and eliminated saturation. The research also showed that optimal AFCSs transmit the signals with the bit-(information-) rate equal to the capacity of the systems.

Comparison of the architecture and mathematical models of AFCS and AC ADC showed their identity except of non-Gaussian distributions of quantization noises ν_k, ξ_k [8]. However, it was evident that increase of resolution of $\mathrm{ADC_{In}}$ and $\mathrm{DAC_{In}}$ approaches the model of AC ADC to the model of AFCS. This had allowed us to suggest that application of optimal algorithms derived for AFCS to AC ADC will make them not ("sub-") optimal but they can be used as the basis for the further systematic optimization of AC ADC. Research [14] and later ones confirmed of this suggestion.

D. Sub-optimal Gaussian conversion algorithm

Optimal for AFCS, and sub-optimal for AC ADC algorithms were obtained under similar to (5) statistical fitting condition [3]-[8]: for each $k=1,...,n$,

$$\Pr_k^{sat} = \Pr(\ |y_k| = G_k\,|e_k|\ > D \,\big|\, \tilde{y}_1^{k-1}) < \mu, \quad (25)$$

where $\tilde{y}_i^{k-1} = (\tilde{y}_1,...,\tilde{y}_{k-1})$ denotes the sequence of low-bit codes $\tilde{y}_i$ delivered to the digital unit of the converters in previous cycles of conversion.

Digital unit (ASIC) of AC ADC computes the codes of estimates according to equation (21) with the gains L_k, G_k set, for each $k=1,...,n$, to the values:

$$G_k = \frac{D}{\alpha\sqrt{\sigma_\nu^2 + P_{k-1}}}\ ;\quad L_k = \frac{1}{G_k}(1 - P_k P_{k-1}^{-1}), \quad (26)$$

where

$$P_k = \begin{cases} \sigma_0^2(1+Q^2)^{-k} & \text{for } 1 \le k \le n^* \\ \sigma_\nu^2(k-n^*+1)^{-1} & \text{for } k > n^* \end{cases} \quad (27)$$

is the MSE of the estimate $\hat{V}_k$ after *k* cycles of conversion. Parameter Q^2 is SNR at the $\mathrm{ADC_{In}}$ output and has the values [3]-[6]:

$$Q^2 = \frac{G_k^2 E[(e_k)^2]}{\sigma_\xi^2} = \left(\frac{D}{\alpha\sigma_\xi}\right)^2 = SNR_{out}^{ADC}. \quad (28)$$

The "threshold cycle" n^* in (27) corresponds to the cycle, for which MSE P_n attains the value σ_ν^2, i.e. is the solution of the equation $P_n = \sigma_\nu^2$ and has the form:

$$n^* = \frac{1}{\log_2(1+Q^2)}\ \log_2\left(\frac{\sigma_0^2}{\sigma_\nu^2}\right) = \frac{\log_2 SNR_{inp}^{ADCin}}{\log_2(1+SNR_{out}^{ADCin})}. \quad (29)$$

Beginning from n^*, MSE diminishes hyperbolically. Initial conditions for (21),(26),(27): $\hat{V}_0 = 0$; $P_0 = \sigma_V^2$; $G_1 = D/\alpha_\mu\sigma_V$. Parameter α_μ, like in Sect. II, is determined by the equation $\Phi(a) = (1-\mu)/2$.

The first step in application of the basis algorithm (21), (26)-(29) to AC ADC optimization was a replacement of the variances σ_ξ^2, σ_ν^2 of Gaussian noises by the variances of quantization noise (4) computed independently for $\mathrm{ADC_{In}}$ and $\mathrm{DAC_{In}}$. Amount of information $I^{AC}(V,\hat{V}_n)$ in the final codes $\hat{V}_n$ formed by AC ADC determines the number of bits necessary for digital presentation of the samples V value that is real resolution of the converter, frequently called "effective number of bits" ($ENOB_n^{AC}$). According to [7],[8], in the Gaussian case:

$$I^{AC}(V,\hat{V}_n) = \frac{1}{2}\log_2\left(\frac{\sigma_0^2}{P_n}\right) = ENOB_n^{AC} = $$

$$= \begin{cases} \dfrac{n}{2}\log_2(1+Q^2) & \text{for } 1 \le n \le n^* \\ \log\dfrac{\sigma_0^2}{\sigma_\nu^2}(n-n^*+1) & \text{for } n > n^* \end{cases} \quad (30)$$

Corresponding mean bit rate at the AC ADC output is determined by the relationship $R_n^{AC} = 2FI^{AC}(V,\hat{V}_n)$.

E. Additional improvement of AC ADC characteristics

The research showed that AC ADC performance can be improved applying complex of methods developed in [3]-[6] and other works. Most of them is half-heuristic but all of them are based on the analysis of algorithm (21), (26)-(29). In particular, the first formulas in (26), (30) show that the increase of G_k decreases MSE P_k, increases $ENOB_n^{AC}$ and information rate R_n^{AC}. This determined the first direction of the research and allowed us to develop model-based methods for simulation analysis of AC ADC [5], [6] defining the maximal permissible values G_k. Joint theoretic and simulation studies allowed for the derivation of high efficient approximate formulas for the optimal gains [15]:

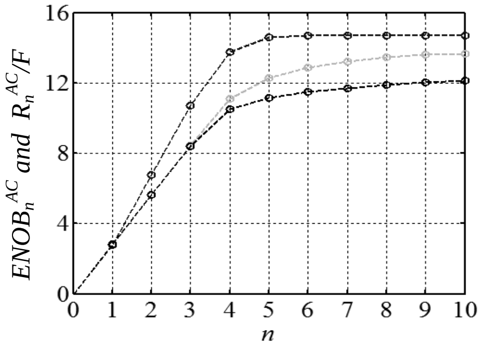

Fig. 2. Dependencies of ENOB and R_n^{AC} / F on the number of conversion cycles for: a) basic algorithm (lower line); b) algorithm with residual errors correction (gray line); c) algorithm with gains (31) (upper line).

$$G_{k+1} = \frac{D}{\Delta_{ADC} /(2 \cdot G_k) + \Delta_{DAC} / 2 + \alpha \sqrt{2} \sigma_{\nu}^{an}}, \qquad (31)$$
$$L_k = G_k^{-1} \ ; \quad (D = \alpha \sigma_0 ; \ G_1 = 1) \ .$$

Significant improvement was achieved also by correction of the conversion algorithm using truncated parts of the residual errors e_k [16]. The improving effects of the corrections illustrated in Fig. 2 were also confirmed experimentally [17].

IV. CONCLUSIONS

The results of research show that optimal fitting of the converters enables elimination of the saturation errors and approaching the flash ADCs and AC ADCs performance to the limit values. It is also shown that measurement of the mean value and variance of the signals is sufficient for definition of the limit efficient resolution and information rate of the flash ADC. It is shown that flash ADCs with uniform quantizers convert the real signals with information rate always smaller than for the signals with uniform distribution.

In turn, optimization of AC ADCs on the basis of the results of AFCS optimization allows for the development of efficient sub-optimal algorithms of conversion approaching ENOB and information rate of AC ADC to the theoretical limits. Additional advantage of AC ADC is a continuation of the growth of resolution at the cycles, where resolution of CADC ceases to grow. This permits to adjust resolution of AC ADC depending on application.

REFERENCES

[1] S.Rapuano, P.Daponte, E.Balestrini, L.De Vito, S.J.Tilden, S.Max, J.Blair, "ADC parameters and characteristics", IEEE Instr. & Measurm. Magazine, vol. 8, no. 5, 2005, pp. 44-54.

[2] W.Kester, Analog-Digital Conversion, AD Inc., 2004.

[3] A.Platonov, "Information properties of sub-optimal cyclic ADC with algorithmic estimates forming", Proc. Polish-Czech-Hungarian Workshop on Circuit Theory and Applic., Warsaw, 2002, pp. 89-94.

[4] Ł.Małkiewicz, A.Platonov, "Analytic design of cyclic low energy ADC with sub-optimal estimates calculation", Proc. of XVII-th IMEKO World Congr. Dubrovnik, Croatia, 2003, pp. 141-146.

[5] A.Platonov, K.Jędrzejewski, J.Jasnos, "Design and analysis of algorithmic multi-pass A/D converters with theoretically highest resolution and rate of conversion", Measurement, vol. 30, no. 3, 2004, pp. 267-278.

[6] A.Platonov, K.Jędrzejewski, Ł.Małkiewicz, "Principles of optimisation, modeling and testing of intelligent cyclic A/D converters", Measurement, vol. 39, no. 3, 2006, pp. 213-231.

[7] A.Platonov, "Optimal identification of regression-type processes under adaptively controlled observations", IEEE Trans. on Sign. Proc., vol. 42, no. 9, 1994, pp. 2280-2291.

[8] A.Platonov, Analytical methods in analog-digital adaptive estimation systems design, Publ. House of Warsaw Univ. of Technology, s. "Electronics", vol. 154, 2006 (in Polish).

[9] A.Platonov, J.Szabatin, "Analog-digital systems for adaptive measurements and parameter estimation of noisy processes", IEEE Trans. on Instr. and Measur., vol. 45, no. 1, 1996, pp. 60-69.

[10] A.Platonov, "Capacity and power-bandwidth efficiency of wireless adaptive feedback communication systems", IEEE Comm. Letters, vol. 16, no. 5, 2012, pp. 573-576.

[11] B.Sclar, Digital Communications: Fundamentals and Applications, 2nd edition, Prentice Hall, 2001.

[12] R.G.Gallager, Information Theory and Reliable Communication, J. Wiley, NY, 1968.

[13] Ignjatovic Z., Sterling M., "Information-Theoretic Approach to AD Conversion", IEEE Trans. CAS-I, 2013, no. 9, pp. 2249-2262.

[14] K.Jędrzejewski, A.Platonov, "A new approach to optimization of adaptive ADC with multi-pass residual compensation", Proc. of Polish-Czech-Hungarian Workshop on Circ. Theory, Sign. Proc. and Telecom. Netw., Budapest, Hungary, 2001, pp. 11-18.

[15] J.Jasnos, "Analysis and application of modified sub-optimal algorithms to ICADC design", 14th IMEKO Int. Symp. on New Technol. in Meas. and Instrum., and 10th Workshop on ADC Modeling and Testing, Gdynia-Jurata, Poland, 2005, pp. 564-567.

[16] Ł.Małkiewicz, A.Platonov, Method of additional improvement of intelligent cyclic ADC performance", Proc. IEEE Int. Conf. on Instr.& Meas. Technology, IMTC-2007, 2007, Warsaw, Poland, IEEE Xplore.

[17] A.Platonov, J.Jasnos, K.Jędrzejewski, Ł.Małkiewicz, Z.Jaworski, E.Piwowarska, P.Studziński, "Particularities of cyclic intelligent ADC design, implementation and adjusting", Int. Conf. on Sign.& Electronic Syst., ICSES'08, Kraków, Poland, 2008, pp. 43-46.