20th IMEKO TC4 International Symposium and
18th International Workshop on ADC Modelling and Testing
Research on Electric and Electronic Measurement for the Economic Upturn
Benevento, Italy, September 15-17, 2014

UTokyo VDEC's CMOS-MEMS Technology via Nanotechnology Platform for Prospective Integrated Magnetic Sensor

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***Abstract* – The paper summarizes CMOS-MEMS multi-project activities among the "Ultrafine Lithography and Nano Measurement Center" of Japanese Government of Education (MEXT)'s Nanotechnology Platform Program, participated by VLSI Design and Education Center of the University of Tokyo. The best mix and match of (1) CMOS LSI fabrication on user-defined Silicon on Insulator (SOI) wafer through VDEC's multi-chip foundry service and (2) MEMS post-processing in cutting-edge micro/nano fabrication apparatuses installed in Federal Class 1 Supercleanroom of VDEC in Takeda Sentanchi Building provides powerful realization tool for brand-new microdevices research. The presentation includes introduction to the activities together with CMOS-MEMS microdevice examples and prospectives.**

I. INTRODUCTION

Based on successful research and industrialization in CMOS Large Scale Integration (CMOS-LSI) devices from 1950s (for information processing), and in Micro Electro Mechanical Systems (MEMS) devices from 1980s (for sensing and actuation), one of the "must proceed to" research fields in 21st century is *integrated microdevices*, or CMOS-MEMS, as summarized in Fig. 1. Careful device and circuit co-design can provide in-situ information processing sensing systems with (1) new functionality, (2) high performance, and (3) compact and/or massively large-scalability. To perform research on such devices, the researcher must have access to both CMOS LSI and MEMS fabrication facilities ("fab"), which are in general bulky and costly. Therefore research activities of CMOS-MEMS were limited to the established big universities, research institutes, and companies that have in-house "fab"s. Making the "fab"s accessible to broader community will drastically accelerate research activities. In the LSI field, as early as 1980s many researchers moved from "in-house fabrication" to "multi-chip foundry" scheme; designers just submit LSI design, and the chips are made at fabs in industry. The major academic foundry players are for example MOSIS(USA, 1981), CMP(France, 1981), and

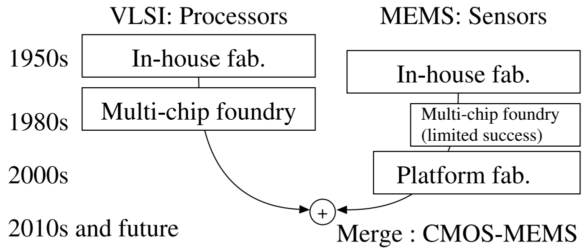

Figure 1. LSI and MEMS R&D evolution

Figure 2. Class 1 Takeda SuperCleanroom Class and Electron Beam Writer F5112+VD01

VDEC/UTokyo(Japan, 1996). This scheme drastically made the VLSI research easier, but in return dedicated tuning of the fabrication process became no more possible.

In the MEMS field, despite pioneering and continuous works of pioneering foundry services such as MUMPs (USA), foundry scheme of MEMS is by ages behind to that of LSI due to the nature that standardization is not that much possible like LSIs. Instead, from around the year 2000, "fab-lab" style multi-use open cleanroom facility infrastructure scheme has grown up. To the authors' knowledge, there are at least three "network-type" nationwide infrastructure projects: National Nanotechnology Infrastructure Netwok (NNIN, USA), Recherche Technologique de Base (RTB, France), and our Nanotechnology Platform

ISBN-14: 978-92-990073-2-7

(Japan). For future, by natural extension of these two activities, a brand-new fabrication scheme is starting: The VDEC users can therefore obtain the reliable LSI wafers made in Japanese company, and can make MEMS processing in the VDEC's cleanroom. In this paper, the VDEC's Nanotechnology Platform site and VDEC's multichip foundry for MEMS post processing are presented together with successful device examples.

II. NANOTECHNOLOGY PLATFORM UTOKYO SITE

Japan's Nanotechnology Platform is the 3^{rd} generation of such national infrastructure project, granted for ten years (2012-2021) by the Ministry of Education, Culture, Sports, Science and Technology (MEXT). The project networks 35 individual research institutes widely spread over Japan. Three technological domains are covered: (1) micro and nano fabrication, (2) atomic level observation, and (3) molecular syntheses. The Nanofab platform is composed of 16 institutes of Japan. These institutes are selected to serve both for local "quick access" fabrication center and key specific technology provider. The University of Tokyo is participating in two layers of Nanofabrication and Nanoobservation. That of Nanofab, called "Ultrafine Lithography and Nano Measurement Center", is operated by the VDEC. The unique features of the VDEC are (1)High-throughput direct E-Beam drawing facility, and (2)simultaneous accessibility to both VLSI and MEMS.

A. *Cutting-edge machines of VDEC in Takeda Cleanroom*

Since 1996, VDEC has put his industrial-grade direct E-Beam machines to the open access from university members. In the year 2014, two E-Beam machines are under open access: ADVANTEST F5112+VD01 (Fig.2) that is 2^{nd} generation machine with finest resolution of 50nm, and ADVANTEST F7000S-VD01 that is 3^{rd} generation machine with finest resolution of 1Xnm. Both machines can draw on entire 8-inch wafer. Typical exposure time over entire 4-inch is half an hour, which is surprisingly rapid as compared to the common sense of EBeam machine. Also, the opeation team is successful in negotiating with Tokyo Oka Corporation (Tok) to acquire special EBeam resist. The resist (OEBR-CAP112) is very thick (1 to 2 μm) as compared to the common thickness (typically 0.1 to 0.5μm), ensuring long micro and nano process. Typical use of the thick resist is direct (maskless) pattern drawing for SOI MEMS; on an SOI wafer the MEMS pattern is directly drawn, and the wafer is readily put into the Silicon Deep Reactive Ion Etching (Deep-RIE) machine. Maximum etching depth with that resist is typically 130μm so that the direct writing can cover most of the MEMS fabrication. By that way, such 1-layer SOI MEMS can be made within one day by the skillful students and or engineers. This drastically short turn-around-time (TAT) is the key feature of MEMS fabrication in Takeda Cleanroom.

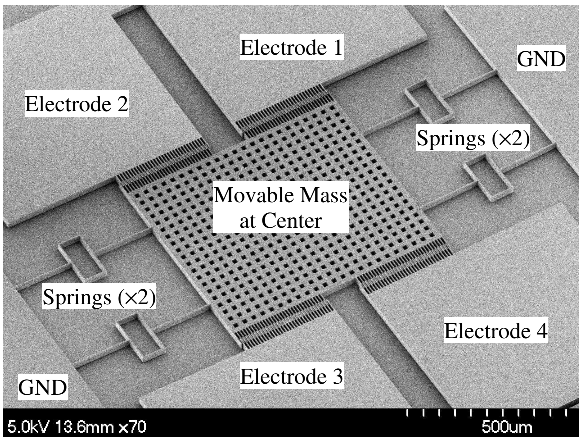

Figure 3. SEM photo of Movable MEMS resonator

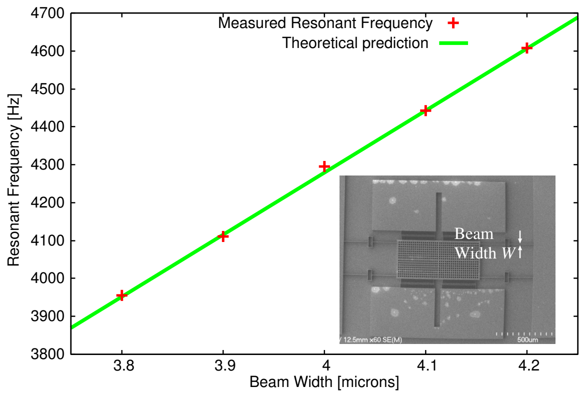

Figure 4. Clear dependence of resonant frequency on beam width was measured

Figure 3is an example of MEMS resonator designed and fabricated by the students of Experimental Course[1]. Through 5-days' intensive course, the students can have real experience of moving silicon device that they have designed by themselves. Due to the ultra-high drawing resolution and accuracy (for F5112+VD01 EBeam writer, data resolution grid is 2nm, and 3-sigma field connection and distortion uniformities are guaranteed below 50nm), it is possible to quantitatively analyse the MEMS devices, by batch-fabricating many devices having slightly perturbate geometries. The plot in the Fig. 4 shows measured and theoretically analyzed resonant frequency dependency on the spring beam width W. Five identical devices were batch fabricated, in varying the design beam width by 100nm from 3.9μm to 4.3μm. As shown in the solid line, the frequency dependence clearly follows the well-known resonant frequency equation:

$$\omega_0 = \sqrt{\frac{k}{m}} = \sqrt{\frac{EtW^3}{2mL^3}} \quad (1)$$

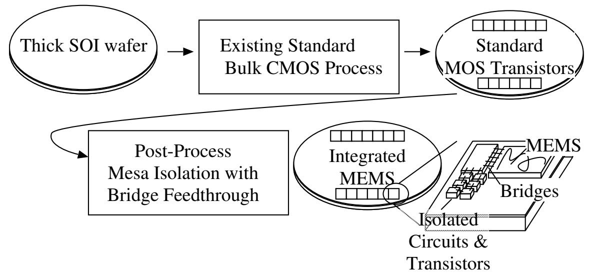

Figure 5. CMOS Post-Process Scheme with User-Defined SOI Wafer

where m and k are equivalent mass and equivalent spring constant respectively. The equivalent spring constant k is defined by Young's modulus E, SOI thickness t, length L and width W of each beam. The equation shows resonant frequency depends on $W^{3/2}$. Such capability of precise (below 100nm) geometry control of microns-size MEMS pattern over large (millimeter to centimeters), is unique to the VDEC EBeam writer, showing his high potential as a powerful tool of MEMS device development.

In recent years, The user count of Takeda Cleanroom is over 600, including over 200 newcomers, coming from around 100 individual research groups coming from industry, academic, and public research entities. Every year the office receives over 150 technological reports, which is more than twice of average report count of the Nanofab sites (As ensemble of 16 sites, Nanofab has over 1,100 reports per year).

B. *"One-stop" simultaneous accessibility to both VLSI and MEMS.*

The high capability on nanofabiracation of UTokyo VDEC site is suitable for quick and efficient R&D of MEMS devices; however it cannot provide millions of transistor devices with industrial quality and technology node. Toward integrated CMOS-MEMS device, VDEC proposes to out-source VLSI fabrication, then perform processing in VDEC Takeda Cleanroom. One of the partner companies of VDEC is Phenitec Semiconductor, Okayama Japan. The company provides standard 0.6μm 5-V 1poly-2(or 3)Metal CMOS process of 6-inch silicon wafer. The scheme is to fabricate VLSI first and then make additional MEMS process (Fig.5), which is widely known as CMOS post-process. One of the unique features of VDEC's post-process schemes is and flexibility on substrate choice. Different from most of the foundry service companies, that of VDEC accepts LSI fabrication on the user-defined silicon substrates. The tested wafer types in addition to standard bulk Si wafer are 9μm, 25μm, and 50μm SOI. Typical usages of SOI substrate are for example (1) in-plane moving MEMS structure, (2) microfluidics integrated LSI (Fig. 7[2]), and (3) electrical device substrate isolation.

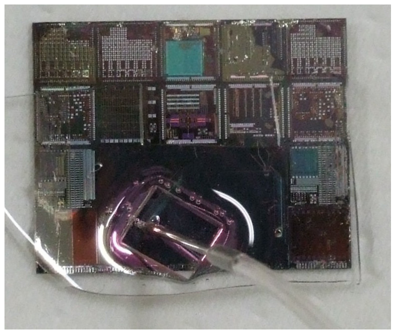

Figure 6. Post-Processed fluidic-integrated LSI device with external connection

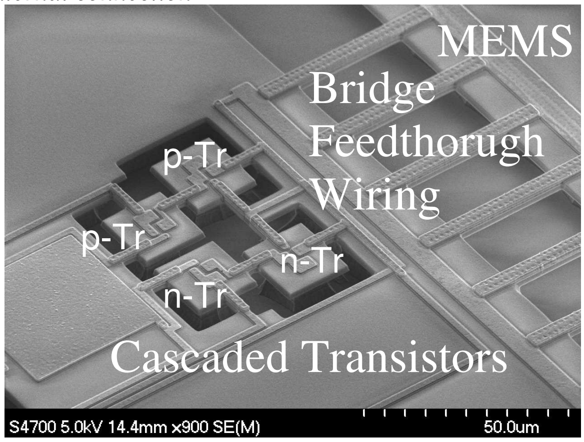

Figure 7. CMOS post-processed CMOS circuit and bridge feedthrough to MEMS

Delivered 6-inch wafer can of course be processed directly, but to increase the chance to success the wafer is in most of cases diced into 15mm square, which is the size of one reticle shot. Fifteen millimeters chip is large enough to hold entire post-process, including EBeam alignment lithography, Plasma RIE, Deep RIE, cleaning and annealing.

Figure 7 shows an SEM micrograph of cascaded CMOS transistors inverter circuit and bridge electrical feedthrough[3]. The circuit is an inverting buffer, composed by two n-type transistors and two p-type transistors connected in cascade. Potential of each transistor's substrate is tied to its source node. The idea is to hold double voltage of $V_{\rm DD}$ by two series-connected transistors. By increasing the number of cascading transistors, the holding voltage was measured to be as high as 160 $V_{\rm DD}$ (800V [4]). The measurement result also shows high flexibility in circuit design.

III. CONSIDERATION FOR INTEGRATED MAGNETIC SENSOR

By taking full advantage of the VDEC's multi-chip foundry and post-process nanotechnolgoy platform, many types of novel integrated sensors will be available. For

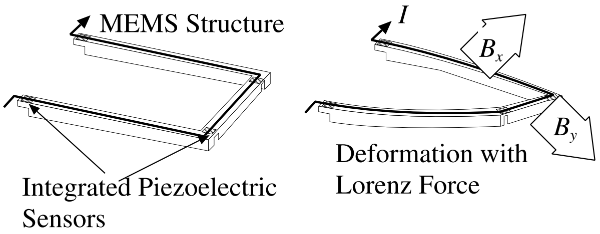

Figure 8. Integrated Lorentz Force Sensor Exaemple

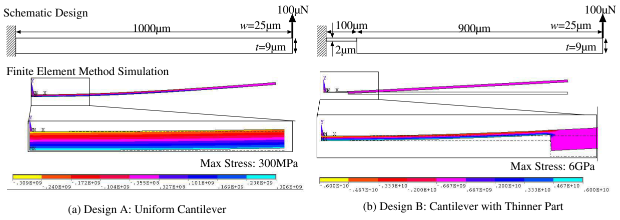

Figure 9. Finite Element Simulation Indicates Possibility to Enhance Sensitivity

example, it is possible to realize Lorentz force sensors such as presented in [5] and [6], by integration of post-processed free-standing MEMS structure and CMOS-processed piezoelectric stress sensing device. A free-standing MEMS structure such as shown in Fig. 8 is realizable by post-processing. As added value of MEMS process, it is possible to intentionally put difference in device thickness. Figure 9 shows an Finite Element Method (FEM) simulation of cantilevers deformation in (a) 1000μm-long 9μm-thick, and 25μm-wide, and (b) the same length and width, except thickness of 2μm instead of 9μm at the root of cantilever for in100μm-long. Major bending occurs at the pinched (thinner) part. Maximum stress in pinched device is 20 times as important as simple cantilever one, thus ensuring better sensitivity.

IV. CONCLUSION AND PERSPECTIVES

VDEC is trying to provide more opportunity of CMOS-MEMS devices to broader research communities. For MEMS fab-lab, Takeda Sentanchi Cleanroom is in continuous operation since the year 2003. For CMOS-MEMS foundry, collaboration with Phenitec Semiconductor started in 2009 and each year at least one multi-chip project fab was launched. These two activities are ensured by MEXT nanotechnology platform from year 2012 to 2021, so the researchers can rely on the stable existence of the process. The system is open to the world; in Europe, NDAs have been issued between four CNRS laboratories in France: GREYC/ENSI de Caen, LIP6/Paris, FEMTO-ST/Besançon, CNFM-LIRMM/Montpelier, and IEMN/Lille, and already a couple of VLSI chips and post-processing have been made. By collaboration with such universities laboratories and or directly to VDEC, researchers can take advantage of the technology in a short turn-around time.

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