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Self-calibratable Adaptive Sub-ranging ADC Insensitive to Amplifiers Gain Errors

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***Abstract* – The paper proposes a variant of adaptive sub-ranging ADC capable of self-calibration in presence of the internal amplifiers gains deviations due to technological imperfections. The changes needed to be implemented to make the adaptive ADC insensitive to gains errors, and the procedure of self-calibration that uses the internal DAC as calibration signal source, are proposed. Capabilities of the approach are discussed on the basis of results of computer simulations.**

***Keywords* – sub-ranging ADC, adaptive ADC, self-calibration, auto-calibration, gain errors**

I. INTRODUCTION

Iterative sub-ranging A/D converters (ADCs) [1],[2] achieve high resolution using in each iteration a low resolution A/D converter (sub-ADC or SADC) or a series of low resolution SADCs in the pipeline architecture, to convert the residue signal which diminishes in subsequent iterations. In order to take full advantage of the SADC's input range, the residue signal needs to be amplified using an amplifier before SADC. The block consisting of an amplifier and SADC can be considered as SADC with input range narrowing in subsequent iterations. Hence the name of this method of A/D conversion. However, presence of the amplifiers in the architecture of the sub-ranging ADC introduces a source of critical errors. Many works (e.g. [1],[2]) pay attention to high sensitivity of the resolution of the sub-ranging ADCs to technologically conditioned deviations of amplifiers gains from the nominal values assumed during their design. This leads to very strict requirements regarding parameters of the amplifiers, which increases complexity, size and power consumption of the ADCs. On the other hand, since these errors are unavoidable, some of the bits at SADC output are not fully reliable, which worsens performance of the sub-ranging ADCs.

These problems are nowadays solved using methods which are not fully efficient for the reasons discussed in Sect. II. Our researches show that transition to adaptive version of the sub-ranging ADC [3]-[10] creates possibilities of a more efficient tackling of the problem. This paper proposes a high performance variant of the adaptive sub-ranging ADC robustified against amplifiers gain errors.

A. Principle of functioning of adaptive sub-ranging ADC

The block diagram of the adaptive sub-ranging ADC discussed in the paper is presented in Fig. 1. The analog part, besides presence of the switch SW, is the same as in conventional sub-ranging ADCs, e.g. [13]. During normal work of the adaptive ADC, the switch SW is in the upper position, as shown in Fig. 1 (the role of the switch SW is described in Sect. III). Sampling of the input signal $V(t)$ is performed by the sample-and-hold unit (S/H). The captured input voltage V is held at the S/H output during K cycles (iterations) of conversion. In each k-th cycle, the compensation signal $\hat{V}_{k-1}^{SDAC}$ is subtracted from the input sample V by means of the subtraction unit (Σ) that forms the residue signal e_k. The compensation signal $\hat{V}_{k-1}^{SDAC}$ is the analog equivalent of the estimate $\hat{V}_{k-1}$ of the input voltage V, computed in the previous cycle of conversion and formed by the internal D/A sub-converter (SDAC) with N_{SDAC}-bit input. The residue signal e_k is amplified by the appropriate, depending on the cycle number, internal amplifier with gain C_k (value C_k increases in subsequent cycles) selected from a bank of amplifiers, and quantized by the coarse flash A/D sub-converter (SADC) with N_{SADC}-bit (2-6 bits) output code $\tilde{y}_k^{SADC}$. The sub-code $\tilde{y}_k^{SADC}$ of the amplified residue signal $C_k e_k$ is used in the digital part of the converter to form the code (estimate) of the input sample according to the following relationship:

$$\hat{V}_k = \hat{V}_{k-1}^{SDAC} + L_k \tilde{y}_k^{SADC}, \tag{1}$$

where L_k is a digital coefficient whose value corresponds to the value of the gain C_k. The final estimate $\hat{V}_K$ (the result of A/D conversion) of the input sample V is obtained after K cycles of conversion. In conventional sub-ranging ADCs the output codes are formed using components performing simple bit operations, whereas in the adaptive sub-ranging ADC, the codes $\hat{V}_k$ are actually calculated in each cycle of conversion in a simple computing unit (Digital Processing Unit in Fig. 1).

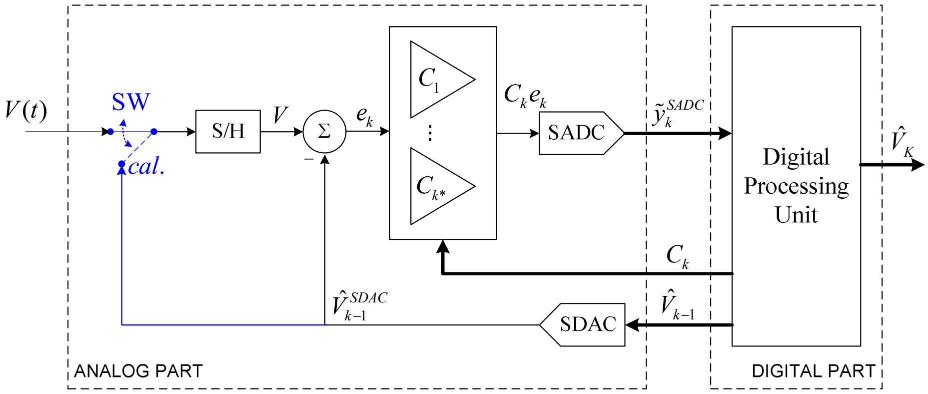


Fig. 1. Block diagram of self-calibratable adaptive ADC

B. Choice of adaptive ADC parameters C_k , L_k

Main effort in previous researches on the adaptive sub-ranging ADCs was focused on development of the methods of determining optimal values of the amplifiers gain coefficients C_k and the corresponding coefficients L_k in (1) that minimize MSE of conversion, or equivalently maximize ENOB (Effective umber of bits [14]) in each cycle of conversion. The optimal values of C_k , L_k in case of absence of analog technological imperfections are determined as follows (see [10] and other works).

In the threshold interval of cycles of conversion $(k \le k^*)$, in which ENOB grows linearly, they should be set to the values:

$$C_k = \frac{D}{\Delta_{SADC}/(2\cdot C_{k-1}) + \Delta_{SDAC}/2 + \alpha\sqrt{2}\sigma_a}\,, \quad L_k = C_k^{-1}\,, \quad (2)$$

where D is a half of the input range of SADC $[-D, D]$, $\Delta_{SADC} = D\cdot 2^{-(N_{SADC}-1)}$ and $\Delta_{SDAC} = D\cdot 2^{-(N_{SDAC}-1)}$ are the quantization intervals of SADC and SDAC, respectively, σ_a^2 is the variance of internal analog noises, α denotes the saturation factor dependent on the assumed permissible probability μ of saturation of SADC ($\mu \ll 1$). In the first cycle the gain $C_1 = D/(D + \Delta_{SDAC}/2 + \alpha\sigma_a)$.

The threshold number of cycles k^* can be assessed as the minimal value of k for which:

$$\Delta_{SADC}/(2\cdot C_{k-1}) < \alpha\sqrt{2}\sigma_a + \Delta_{SDAC}/2\,. \quad (3)$$

In the post-threshold interval of cycles of conversion $(k > k^*)$, in which ENOB grows more slowly – logarithmically, the gains C_k can be fixed, but the coefficients L_k should be adjusted continually as follows:

$$C_k = C_{k^*} = \frac{D}{\alpha\sqrt{2\sigma_a^2 + \Delta_{SDAC}^2/12}}\,, \qquad L_k = C_k^{-1}\left(1 - \frac{P_k}{P_{k-1}}\right),$$

$$P_k = P_{k-1} - \frac{C_k^2 P_{k-1}}{\sigma_\xi^2 + C_k^2(\Delta_{SDAC}^2/12 + \sigma_a^2 + P_{k-1})}\,, \quad (4)$$

where σ_ξ^2 denotes the variance of the SADC quantization noise (usually, it can be assumed that $\sigma_\xi^2 = \Delta_{SADC}^2/12$). Initial condition for (4) is $P_{k^*} = \Delta_{SDAC}^2/12 + 2\sigma_a^2$.

According to the results of previous researches (see e.g. [6]), formula (1) should be corrected as follows:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k^{SADC} - L_k C_k (\hat{V}_{k-1} - \hat{V}_{k-1}^{SDAC})\,, \quad (5)$$

to include an additional component related to the correction of the truncation error $\hat{V}_{k-1} - \hat{V}_{k-1}^{SDAC}$ appearing when the analog equivalent $\hat{V}_{k-1}^{DAC}$ of the estimate $\hat{V}_{k-1}$ is formed by means of SDAC with limited precision N_{SDAC} -bit, lower than the precision N_{comp} of calculation of the estimates $\hat{V}_{k-1}$ in the digital part of the adaptive ADC.

A sub-ranging adaptive ADC designed according to algorithm (2)-(5) is optimal but very sensitive to imperfections of its analog components, in particular to gains errors.

II. RELATED RESULTS IN THE LITERATURE

The paper extends the results of works [3]-[10] and others, concerning development of the methods of design and optimization of adaptive sub-ranging ADCs. It addresses the issue of strong influence of amplifiers gains errors on performance of sub-ranging ADCs, and proposes a solution allowing reduction of the influence of these errors much more efficiently than methods used in conventional sub-ranging ADCs. The solution involves a modification of the design as well as a calibration procedure differing from the today used (see e.g. [11],[12]).

The errors of the amplifier gains in a given cycle k of conversion increase the residue signal in the following cycle, which in turn increases the probability of saturation of the internal converter SDAC, i.e. the probability of appearance of large error in the final estimate $\hat{V}_K$. To keep the probability of abnormal errors below the permissible value, the nominal gains C_k have to be decreased. In known sub-ranging ADCs, for this purpose the gains of the amplifiers in particular cycles are reduced by half [1],[2], which decrements the speed of conversion by 1 bit per cycle. This decrement by half is excessive, but is necessitated by the principle of forming of output codes used in conventional sub-ranging ADCs. Building the output word as a juxtaposition of codes of successive observations $\tilde{y}_k^{SADC}$ imposes a constraint on possible nominal gains values – they have to be exact integer powers of two (as shifting a binary code by several positions is equivalent to multiplying the number it represents, by an integer power of two).

In sub-ranging adaptive ADCs, thanks to a different method of codes forming – actual computing estimates $\hat{V}_k$ in each cycle of conversion in a computing unit, the constraint on possible gains values limiting them to integer powers of two is removed and they can be assigned arbitrary values. This creates the possibility to set the gains C_k to the values not lower than exactly sufficient for elimination of saturations, and was employed in [9] as well as is the basis to development of the self-calibration method in this work.

III. DESCRIPTION OF THE METHOD

Implementation of the capability of self-calibration in the adaptive ADC with amplifiers gains errors requires that before its manufacturing, the nominal gains values be reduced using the method described in [9],[15], taking into account the expected maximal technological deviations of the amplifiers gains, modeled as follows:

$$C_k^{(act)} = C_k(1+\varepsilon_k), \quad k = 1,..,k^*, \tag{6}$$

where $C_k^{(act)}, C_k$ are the actual and nominal amplifier gain values in cycle k, respectively. The variable ε_k is a relative gain error assumed to be a random value with zero mean, limited to the interval $[-\delta_C, \delta_C]$. The method of determination of "safe", adequately diminished to exclude saturation, gain values $C_k^{(safe)}$ for subsequent cycles, consists in correction of the nominal gains C_k obtained using algorithm (2)-(5), taking into account the expected limit values of gain errors δ_C. The largest safe values $C_k^{(safe)}$ are then to be determined as follows:

$$C_1^{(safe)} = C_1/(1+\delta_C),$$

$$C_2^{(safe)} = \frac{\frac{C_2}{1+\delta_C}\left(\frac{\Delta_{SADC}}{2C_1}+\frac{\Delta_{SDAC}}{2}+\alpha\sqrt{2}\sigma_a\right)}{\delta_L D+\frac{\Delta_{SADC}}{2C_1^{safe}}\frac{1+\delta_L}{1-\delta_C}+\frac{\Delta_{SDAC}(1+\delta_L)}{2}+\alpha\sigma_a\sqrt{2+2\delta_L+\delta_L^2}}, \tag{7}$$

$$C_{k>2}^{(safe)} = \frac{\frac{C_k}{1+\delta_C}\left(\frac{\Delta_{SADC}}{2C_{k-1}}+\frac{\Delta_{SDAC}}{2}+\alpha\sqrt{2}\sigma_a\right)}{\frac{\Delta_{SADC}}{2C_{k-2}^{safe}}\frac{\delta_L}{1-\delta_C}+\frac{\Delta_{SADC}}{2C_{k-1}^{safe}}\frac{1+\delta_L}{1-\delta_C}+\frac{\Delta_{SDAC}(1+\delta_L)}{2}+\alpha\sigma_a\sqrt{2(1+\delta_L+\delta_L^2)}}$$

where δ_L denotes the maximal relative error of L_k estimation. More details about the assumptions and methodology used in derivation of formulas (7) can be found in [15].

The second necessary modification in the self-calibratable adaptive ADC is introduction of the switch SW, shown in Fig. 1, allowing usage of SDAC as a generator of the testing signal, by connecting the output of SDAC to the input of S/H. During self-calibration, the switch is in "cal." position, which enables autonomous generation of testing samples $V^{(j)}$ required by the calibration procedure.

The aim of the self-calibration procedure is determination of the best coefficients L_k corresponding to the actual values of gains $C_k^{(act)}$. The procedure is performed in k^* steps corresponding to the number of internal amplifiers used in the converter. Let us consider the first step $(k=1)$. The testing samples $V^{(j)}$ spanning over the full input range of the adaptive ADC, are converted by the adaptive ADC in $k=1$ cycle (i.e. using only the first amplifier) and there are collected corresponding values $\tilde{y}_1^{SADC,(j)}$. On their basis, there are calculated, according to (1), the corresponding estimates $\hat{V}_1^{(i,j)}$. Since the best value $L_1^{(act)} = (C_1^{(act)})^{-1}$ is not known (as $C_1^{(act)}$ is not known), the estimates are computed using a range of values $L_1^{(i)}$ around the nominal value $L_k^{(safe)} = (C_k^{(safe)})^{-1}$. For each set of estimates $\hat{V}_1^{(i,j)}$ obtained for a particular value $L_1^{(i)}$, one can compute the corresponding mean square errors (MSE) of estimates. The general formula used in this procedure for calculating MSE for subsequent steps k is as follows:

$$MSE_k^{(i)} = \frac{1}{J}\sum_{j=1}^{J}\left[\hat{V}_k^{(i,j)} - V^{(j)}\right]^2. \tag{8}$$

The most appropriate value $\hat{L}_1$ among coefficients $L_1^{(i)}$ is selected as the value $L_1^{(i)}$ for which $MSE_1^{(i)}$ is minimal:

$$\hat{L}_k = \arg\min_{L_k^{(i)}} MSE_k^{(i)}. \tag{9}$$

In further steps $(2 \le k \le k^*)$, when the k-th coefficient $\hat{L}_k$ is searched, the adaptive ADC converts each sample of the testing signal $V^{(j)}$ in k cycles, using algorithm (5) with the previous coefficients $L_1,...,L_{k-1}$ set to the best values $\hat{L}_1,...,\hat{L}_{k-1}$ determined in the previous steps of the calibration. The current estimate $\hat{L}_k$ is chosen according to (9). The range of the considered values $L_k^{(i)}$ in a given step k is defined as $[(C_k^{(safe)}(1+\delta_C))^{-1}, (C_k^{(safe)}(1-\delta_C))^{-1}]$. The borders of the interval relate to the inverted values of gains for extreme errors $\pm\delta_C$. Fig. 2 presents an exemplary plot of $MSE_2^{(i)}$ as a function of the values $L_2^{(i)}$ (for $\delta_C = 5$ %, $\varepsilon_1 = -4.5$ %, $\varepsilon_2 = 4$ %), using which one can easily identify the value $L_2^{(i)} \approx 0.082$ providing minimal $MSE_2^{(i)}$. For $k > k^*$, when the gains are fixed and equal to $C_{k^*}^{(act)}$, the calibration procedure comes down to determination of the coefficients $\hat{L}_k$ using (4), in which the gain C_{k^*} takes the value $(\hat{L}_{k^*})^{-1}$. The complete self-calibration procedure allowing determination of all $\hat{L}_k$, can be implemented in the digital part and performed by the adaptive ADC autonomously, using only the converter's own resources.

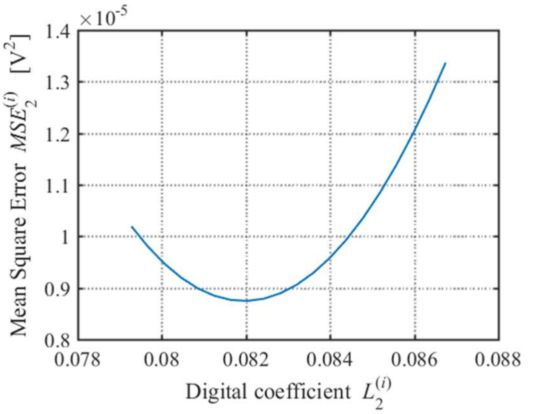


Fig. 2. MSE (8) as a function of digital coefficient $L_2^{(i)}$

IV. RESULTS OF SIMULATIONS

To verify feasibility and examine efficiency of the self-calibration procedure, a relevant model of the adaptive ADC was developed in MATLAB. The performance of the adaptive ADC was assessed using the values of ENOB achieved after k cycles, calculated according to the definition given in IEEE Std. 1241-2010 [14]:

$$ENOB_k = \log_2\left(\frac{FSR}{NAD_k \cdot \sqrt{12}}\right), \qquad (10)$$

$$NAD_k = \sqrt{\frac{1}{M}\sum_{m=1}^{M}\left[\hat{V}_k^{(m)} - V^{(m)}\right]^2}, \qquad (11)$$

where $FSR = 2D$ is the full-scale range of ADC and NAD_k is the rms value of noise and distortion [14]. ENOB (10) was calculated on the basis of the results of conversion of the same (in all experiments) sequences of signal samples $V^{(m)}$ $(m = 1,...,M)$, uniformly distributed in the entire input of the adaptive ADC, $M = 100{,}000$. We assumed stepwise models of SADC and SDAC with the number of output bits of SADC $N_{SADC} = 4$ and the number of input bits of SDAC $N_{SDAC} = 12$, $FSR = 2\,\text{V}$, $\alpha = 4$, $\hat{V}_0 = 0$. Analog noise at the output of the subtraction unit Σ was simulated as a Gaussian zero-mean white noise with the standard deviation equal to $\sigma_a = 10\ \mu\text{V}$. For these values of parameters the threshold number of cycles equal to the number of internal amplifiers is $k^* = 4$. The gains errors were modeled according to (6) with the maximal gain deviation δ_C changed from 0 to 10 %. The maximal relative error of L_k estimation was assumed to be $\delta_L = 1\,\%$. To enable comparison of the results for different values of δ_C, in all experiments instead of random values, the simulated gain errors for $k = 1,2,3,4$ took the following pseudorandom values: $-0.9\delta_C, 0.8\delta_C, -0.6\delta_C, 0.7\delta_C$, respectively.

Fig. 3 shows the behavior of ENOB (in subsequent cycles k) of the adaptive ADC employing the standard algorithm (2)-(5) in presence of gains errors for various gain deviations δ_C. Let us observe that merely one percent errors decrease ENOB significantly. The reason of the serious decrease of ENOB with increasing gain deviations δ_C is correspondingly growing frequency of appearance of saturations in subsequent cycles. The results shown in Fig. 3 confirm that the adaptive ADC operating according to (2)-(5) is very sensitive to gains errors.

The next figure presents the values of ENOB obtained for the adaptive ADC designed and self-calibrated as described in Sect. III. To determine the values of the coefficients $\hat{L}_k$, we used 20 values of $L_k^{(i)}$ uniformly distributed in the intervals $[(C_k^{(safe)}(1+\delta_C))^{-1}, (C_k^{(safe)}(1-\delta_C))^{-1}]$. The results shown in Fig. 4 prove that the proposed self-calibratable adaptive ADC can eliminate very efficiently the negative influence of the gains errors in a noticeably large range of their magnitude. Moreover, the decrease of ENOB with growth of gains deviation δ_C is relatively low and results only from the necessary decrease of the gains values (7).

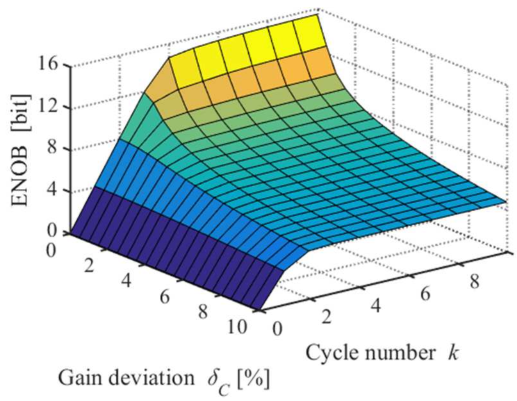


Fig. 3. ENOB of adaptive ADC using the standard algorithm in subsequent cycles k for various gain deviations δ_C

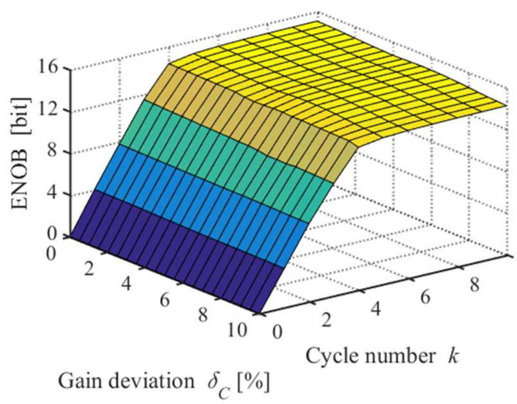
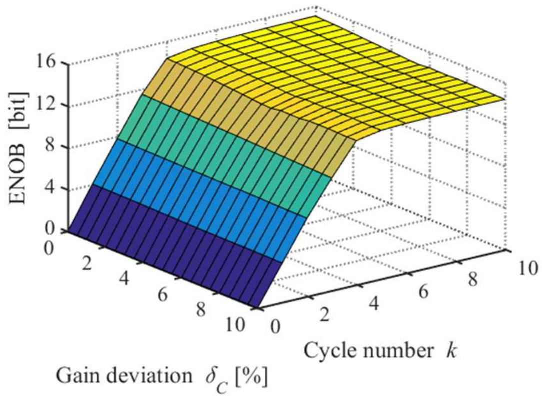
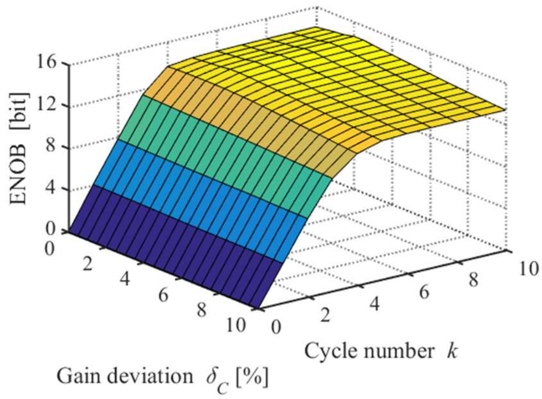


Fig. 4. ENOB of adaptive ADC after self-calibration in subsequent cycles k for various gain deviations δ_C

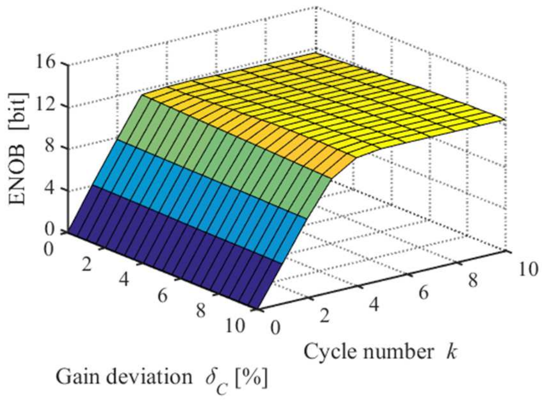
In the next series of experiments, we investigated the influence of SDAC nonlinearity on the effectiveness of the proposed method of self-calibration of the adaptive ADC that uses SDAC as a generator of the calibrating signal. The errors due to SDAC nonlinearity were simulated as the errors of its output voltages with the same values during the process of self-calibration as well as during conversion. The errors were modelled as uniformly distributed in the interval $[-\delta_{SDAC}, \delta_{SDAC}]$ random variations of all possible output voltages. Fig. 5 shows ENOB obtained for $\delta_{SDAC} = 0.5, 1, 2$ LSB, where LSB is the voltage corresponding to the least significant bit of SDAC. Plots of ENOB depending on the SDAC nonlinearity presented in Fig. 5 were obtained for the same parameters as plots in Fig.4. They indicate that small SDAC nonlinearity ($\delta_{SDAC} \le 0.5$ LSB) does not influence ENOB, whereas greater SDAC errors ($\delta_{SDAC} = 1, 2$ LSB) cause significant losses of ENOB. The robustness of ENOB to small SDAC errors can be explained as follows. The gains C_k have been diminished to take into account errors in SDAC (the term $\Delta_{SDAC}/2$ in the denominator in (2)), as well as gain errors (correcting factor in (7)). Due to the min-max approach and slight excessiveness connected with it, there



a)

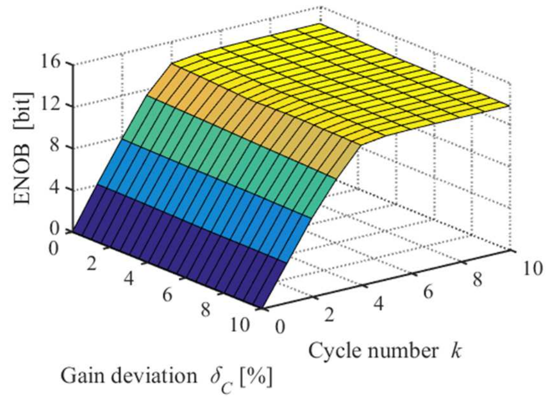


b)

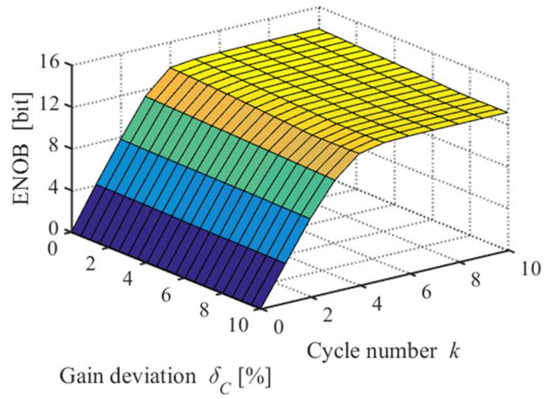


c)

Fig. 5. ENOB of adaptive ADC after self-calibration for various levels of SDAC errors: a) 0.5 LSB, b) 1 LSB, c) 2 LSB



a)



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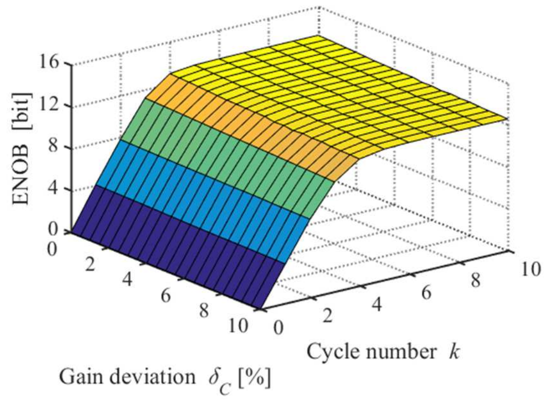

c)

Fig. 6. ENOB of adaptive ADC after self-calibration with taking into account SDAC errors for various levels of SDAC errors: a) 0.5 LSB, b) 1 LSB, c) 2 LSB

exists a slight reserve in the usage of the input range of SADC that accommodates small additional errors, but is not enough for greater values of δ_{SDAC}. Unexpectedly, the losses of ENOB are more visible for lower values of the gain errors (e.g. till $\delta_C \approx 2.5\ \%$ in Fig. 5b). This effect can be explained the same way – lesser excessiveness for lower levels of the gain errors makes the algorithm more sensitive to additional errors. Therefore, for larger SDAC nonlinearity, one needs to take it into account in the conversion algorithm. It can be done by introducing the additional element δ_{SDAC} into the denominator of (2), which in result gives the following formula for C_k:

$$C_k = \frac{D}{\Delta_{SADC}/(2\cdot C_{k-1}) + \Delta_{SDAC}/2 + \alpha\sqrt{2}\sigma_a + \delta_{SDAC}}. \quad (12)$$

Fig. 6 presents the results of simulations corresponding to the results shown in Fig. 5, but obtained using (12) instead of (2) in the conversion algorithm. In Figs. 6b and 6c, there cannot be observed such decreases of ENOB as in Figs. 5b and 5c, which is the effect of the appropriate, greater decrease of C_k. However, the decrease of C_k is a cause of corresponding decrease of the achieved ENOBs, visible even for $\delta_{SDAC} = 0.5$ LSB.

V. NOVELTIES IN THE PAPER

The novelty of this work is development of a new variant of the adaptive sub-ranging ADC capable of self-calibration regarding gains errors of its internal amplifiers. Implementation of the self-calibration capability requires only a slight change in the architecture of the analog part of the adaptive ADC – introduction of a switch as in Fig. 1, and implementation of the self-calibration procedure in its digital part.

VI. CONCLUSIONS

A new variant of the adaptive sub-ranging ADC capable of self-calibration regarding gains errors of its amplifiers is proposed and discussed. The proposed calibration procedure does not require additional external equipment (is fully autonomous). It is realized solely using the internal components already present in the adaptive ADC and used for the purposes of A/D conversion.

It is a particularity of the method of adaptive sub-ranging A/D conversion that it creates a possibility to implement the proposed self-calibration procedure and enables reduction of the requirements to precision of the amplifiers manufacturing. At the same time, the cost (in ENOB per bit) of tackling the gains errors is much less than in conventional sub-ranging ADCs.

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REFERENCES

[1] W. Kester, (Ed.) *Analog-Digital Conversion*, Analog Devices, Inc., 2004.

[2] F. Maloberti, Data Converters, Springer, 2007.

[3] K. Jędrzejewski, A. Platonov, "A New Approach to Optimization of Adaptive ADC with Multi-pass Residual Compensation," Proc. of Polish-Czech-Hungarian Workshop on Circuits Theory, Signal Processing and Telecommunication Networks, Budapest, Hungary, pp. 11-18, 2001.

[4] A. Platonov, K. Jędrzejewski, J. Jasnos, "Design and analysis of algorithmic multi-pass A/D converters with theoretically highest resolution and rate of conversion," Measurement 30(3), pp. 267-278, 2004.

[5] A. Platonov, K. Jędrzejewski, Ł. Małkiewicz, "Principles of optimisation, modeling and testing of intelligent cyclic A/D converters," Measurement 39(3), pp. 213-231, 2006.

[6] Ł. Małkiewicz, A. Platonov, "Methods of additional improvement of intelligent cyclic ADC performance," Proc. of IEEE Instrum. and Measurement Technology Conference IMTC-2007, Warsaw, Poland, 2007.

[7] K. Jędrzejewski, A. Platonov, "Principles of New Method of Optimisation, Design and Modelling of Pipeline A/D Converters," Measurement 42(8), pp. 1195-1202, 2009.

[8] K. Jędrzejewski, "Elimination of Drift-Like Errors in Intelligent Cyclic A/D Converters," Measurement 45(2), pp. 170-174, 2012.

[9] Ł. Małkiewicz, "Reduction of the influence of amplifier gain setting errors on the performance of adaptive ADC," Proceedings of SPIE 8903, pp. 8903H-1 – 8903H-8, 2013.

[10] K. Jędrzejewski, Ł. Małkiewicz, A. Platonov, "Analysis and improvement of post-threshold mode of adaptive cyclic ADC operation," Proceedings of SPIE 9662, pp. 96621X-1 – 96621X-12, 2015.

[11] B. Sahoo, "An Overview of Digital Calibration Techniques for Pipelined ADCs," Proc. of 2014 IEEE 57th International Midwest Symposium on Circuits and Systems (MWSCAS), College Station, TX, USA, pp. 1061-1064, 2014.

[12] A.J. Ginés, E.J. Peralías, A. Rueda, "A Survey on Digital Background Calibration of ADCs," Proc. of European Conference on Circuit Theory and Design ECCTD 2009, Antalya, Turkey, pp. 101-104, 2009.

[13] http://www.analog.com/media/en/technical-documentation/data-sheets/AD679.pdf

[14] Standard IEEE-1241-2010, "IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters," 2011.

[15] Ł. Małkiewicz, K. Jędrzejewski, "Design and Calibration of Adaptive Sub-ranging ADCs Resistant to Amplifiers Gain Errors," Proc. of 21st IMEKO TC4 Symposium and 19th International Workshop on ADC Modelling and Testing, Budapest, Hungary, 2016 (in this issue).