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Linearity Evaluation of High Speed Sampling Delta- Sigma ADC Board

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Abstract **– High-speed sampling delta-sigma ADC boards become popular in scientific and metrology researches these days and its demands on the evaluation and calibration are increasing. The aim of this research is to investigate linearity deviation for delta-sigma ADCs, NI-5922 on PXI platform, to input signal. Here, we developed a system to measure the linearity error of ADC adopting a reference sampling voltmeter and a dummy waveform generator. With this system, we evaluated the linirity error for three units of NI-5922 boards, which were combined with three different chassis based on the PXI and the PXI Express platforms. We found that the linearity error depends on the type of the PXI platforms comined with the ADC boards.**

Keywords **– Analog-to-Digital Converter, Delta-Sigma ADC board, DC linearity**

I. INTRODUCTION

Recently, NI-5922, an analog-to-digital converter employing delta-sigma modulator (delta-sigma ADC) is widely used for metrological and industrial applications, even though the evaluation of the board in metrological aspects is still challenging. The digitizing resolution for the board is flexible, so that it changes with the rate of sampling. At the maximum sampling rate of 15 MS/s, the resolution is 16 bit, while the resolution reaches up 24 bit below 500 kS/s. The core of the ADC basically consists of an oversampling modulator and a digital filter. The oversampling modulator takes samples with a higher sampling rate than desired in conventional ADCs, which results in a lower noise floor in sampling measurements, but might cause rather large linearity error.

In this work, we evaluated the linearity for three different units of NI-5922 boards using a dummy waveform source and a reference sampler. All the measurements were carried out for the 1-V and 5-V input ranges of the boards with fixed parameters; 50 kS/s sampling rate and 1 MΩ input impedance. Also, we repeated the evaluation in several changes of PXI chassis for the ADC units. In this paper the terms, NI-5922 and delta-sigma ADC, are used interchangeably.

II. RELATED RESULTS IN THE LITERATURE

Previous linearity investigations on the ADC board mainly concentrate on AC characterization. In Ref.[1] linearity has been investigated using sinusoidal signal at 1 kHz with a sampling frequency of 100 kS/s, while integral non-linearity (INL) has been measured with stepwise triangular wave forms generated by a programmable Josephson voltage standards (PJVS) from 0.48 Hz to 1 kHz in [2]. However for all the frequencies the normalized INL error was estimated to be less than 4 µV/V in [2].

DC linearity of the board has been investigated

employing an analog differential front-end circuit, where it was found that DC non-linearity can be described by a model of a third –order polynomial [3].

Recently the linearity for the ADC combined to one of the chassis to be investigated in this work was evaluated [4]. The key issue for the study was to elucidate how the linearity error was reflected in differential sampling measurements based on a Josephson voltage standard. The boards showed different DC linearity characteristics thus the different polynomial functions are expected to describe the linearity characteristics.

III. EXPERIMENTAL

A. Measurement setup and method

Schematic diagram of the measurement setup is shown in Fig. 1. A step-wise approximated triangular waveform generated by the 14-bit AWG was fed into the two channels, i.e., the A and B channels, of the delta-sigma ADC board and the reference sampler through an AC multiplexer sequentially.
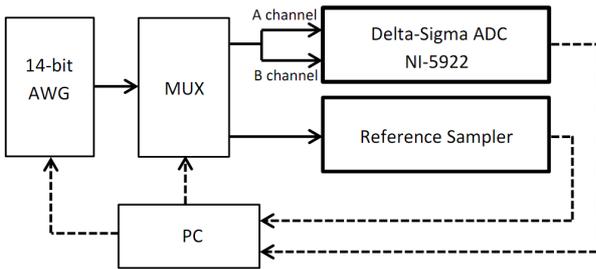

Fig. 1. Schematic diagram of the measurement setup

The waveform with frequency of 5 Hz consists of 40 voltage steps with the same interval per a single period. After the measurements, the samples in the step-transition regions, where overshoot and ringing of the signal appear, were removed, and the samples only on steps are compared with the reference values. Fig. 2 shows the waveforms sampled by the delta-sigma ADC and the reference sampler for 5-V range. For the measurements, the delta-sigma ADC was operated in the sampling rate 50 kS/s with 24 bits resolution for both 1-V and 5-V ranges. Reference sampler collected 400 samples per period; however it is found that the sampling rate of the sampler did not make any significant change in the final results. The ADC and the reference sampler took 250 samples and 10 samples per a step respectively and the mean values, $V_{i(ADC)}$ and $V_{i(RS)}$, obtained after removing samples in the transient region, were considered as the sampled voltage value for the ith step.

The linearity evaluation for the delta-sigma ADC board in this work relies on the reference sampler, Agilent 3458A. Hence it is quite important to confirm the linearity error for the reference sampler. The error can be estimated by measuring the voltage generated with a reference voltage source. Fig. 3 shows the measurement result.
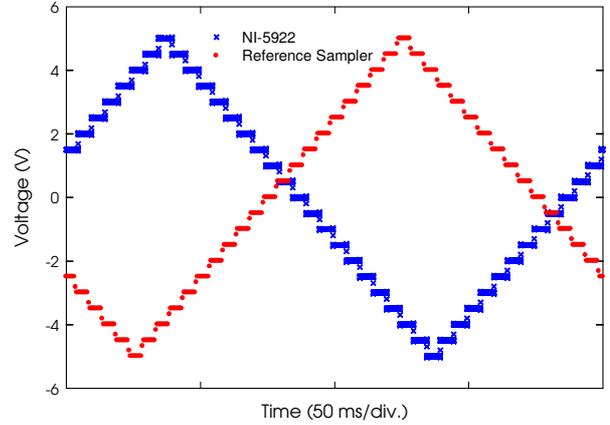

Fig. 2. Triangular waveform sampled by the delta-sigma ADC and the reference sampler

The reference DC voltages from -10 V to +10 V with 0.5 V step were successively generated by a 10-V programmable Josephson voltage standard, the voltages were measured with the reference sampler. After the measurements, the data V_m were compared with a linear function $aV_J + b$, where V_J is output of the Josephson voltage standard. The parameters a and b are adjustable parameters in a least-squares regression. The plot shows the deviation, $V_m - (aV_J + b)$. The maximum deviation is about 0.5 μV, and thus the linearity error for the sampler is estimated to be 0.05 μV/V at 10-V range. The value for the linearity error, however, is inferred to be somewhat overestimated, since the data in Fig. 3 also reflect measurement noise as well as the linearity error.
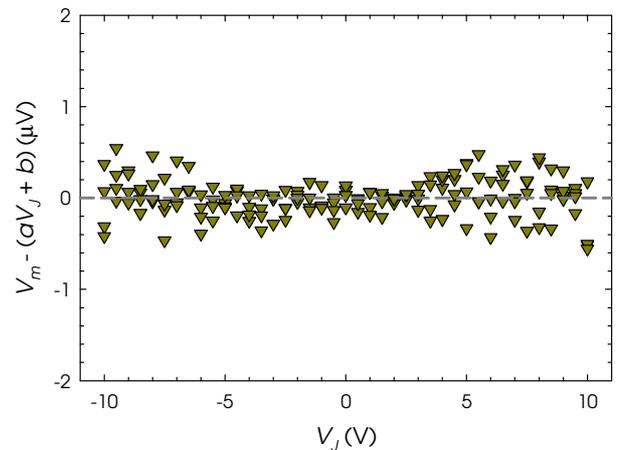

Fig. 3. Linearity evaluation of reference sampler in 10 V Voltage range employing PJVS as the reference voltage source.

The three delta-sigma ADC boards were tested with three different chassis with the different model numbers.

Chassis 1 and chassis 2 are based on PXI express while chassis 3 is based on PXI instrumentation platform. As stated before, a single period of the input signal to the ADC and the reference sampler consists of voltages steps, $n = 40$, with $n/2 + 1$ levels. The measurement error of the ADC was calculated by the averaging the difference between $V_{i(ADC)}$ and $V_{i(RS)}$ over the number of 110 cycles as follows:

$$\Delta V_i = \overline{V_{i(ADC)} - V_{i(RS)}}, \tag{1}$$

where ΔV_i is the ADC error for the ith step. The ΔV_i reflects the gain and linearity errors, and the linearity error corresponds to the deviation from a linear-least squares fit of the ΔV_i using a function $aV_{i(RS)} + b$, where the a and b are adjustable parameters.

B. Results and discussion

As stated before, the measurements were repeated with the three different PXI chassis. Fig. 4, Fig. 5 and Fig. 6 show the linearity deviations for the delta-sigma ADCs; ADC-1, ADC-2 and ADC-3, respectively. The error bars in the plots denote the standard deviations of the samples for the 110 cycles of the AWG output waveforms. These plots show the results only for the A Channel of the ADCs.
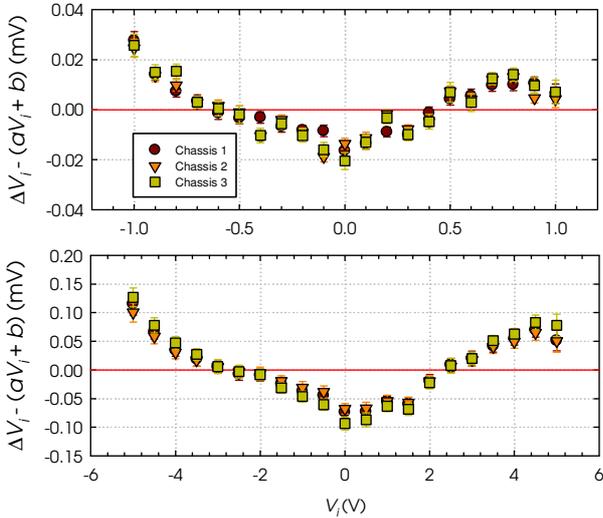

Fig. 4.   Linearity error of delta-sigma ADC-1. (Top) INL in 1-V range. (Bottom) INL in 5-V range.

For ADC-1, the maximum linearity deviation is about 30 µV for 1-V range and less than 150 µV for 5-V range, while the maximum deviations for ADC-2 and ADC-3 are less than 15 µV and 80 µV for 1-V range and 5-V range, respectively.

It is noticeable that the variation of linearity on the chassis is prominently seen for ADC-2 and ADC-3. For instance, when the chassis 2 and chassis 3 are used, the data at 1-V range show severe irregularity with respect to

input voltage. As one can see in the Fig. 5 and Fig. 6, for the ADC-2 and ADC-3, the maximum linearity-error variation due to the chassis change is about 15 µV and 80 µV for 1-V and 5-V ranges, respectively. In fact, even in case of the ADC-1, the degree of the variation is nearly the same as those of the other two boards, but the chassis dependency of the deviation does not look eminent relative to a large linearity error itself.
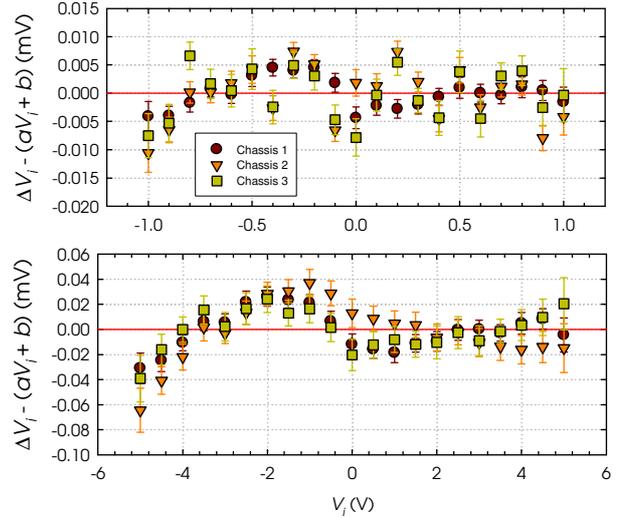

Fig. 5.   Linearity error of delta-sigma ADC-2. (Top) INL in 1-V range. (Bottom) INL in 5- V range.
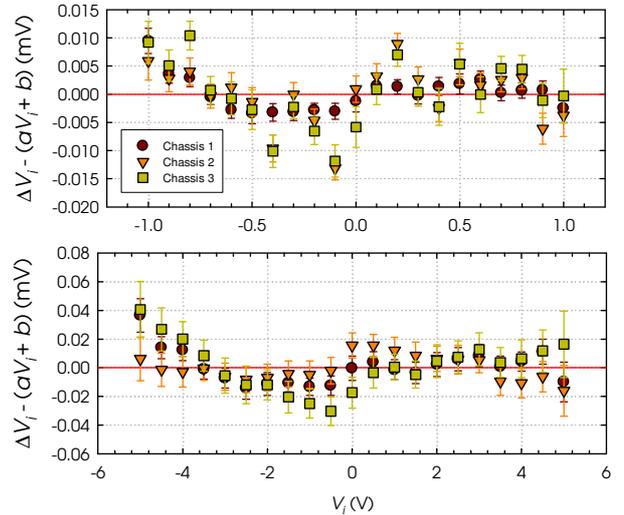

Fig. 6.   Linearity error of delta-sigma ADC-3. (Top) INL in 1-V range. (Bottom) INL in 5-V range.

This means a linearity evaluation for the ADC board performed with a specific chassis would not be valid when the chassis is replaced.

It is noticeable that the overall patterns of the linearity deviation at 1-V and 5-V ranges for the boards are quite similar to each other. This becomes obvious when the

data are normalized with the full-scale value of the ranges as shown in Fig. 7. As one can see, all the six data sets for each board are scaled into a single curve, regardless of the ADC ranges. However, the scaling is not perfect when the boards are combined with the chassis 2 and 3, as notably seen in Fig. 7 (Middle) and Fig. 7 (Bottom). Especially, the data at 1-V range shows severe irregularity with respect to input voltage, compared with the data for the 5-V range. As previously reported in [2], changing the input range of the ADC only affects the analog stage of analog-to-digital conversion. The irregularities in the data might imply that the linearity is affected by the analog input stage as well as the ADC stage.
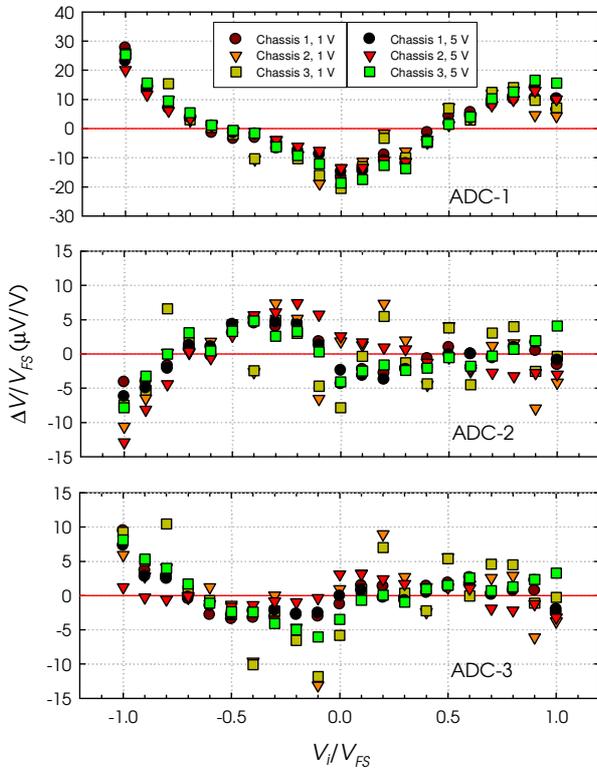

Fig. 7. Normalized results for 1-V range and 5-V range. (Top) INL of ADC-1. (Middle)INL of ADC-2. (Bottom) INL of ADC-3.

IV. NOVELTIES IN THE PAPER

The aim of this work is to investigate the effect of the chassis to the linearity error of the delta-sigma ADCs. For this, we developed a linearity evaluation system for the ADC boards, employing a reference sampler of which the measurement error was evaluated using a programmable Josephson voltage standard. We have tested three units of the boards with the different PXI chassis to examine how the chassis affect in the linearity deviation of the boards.

V. CONCLUSIONS

We developed a system to evaluate linearity for the delta-sigma ADCs employing step-wise approximated triangular waveform. We have measured linearity deviations for three units of NI-5922 by utilizing the system. The linearity error for the two boards among them is estimated to be about 25 µV/V, while it is about 55 µV/V for the other unit. Also, we found that the linearity deviation with respect to input showed different behaviors on the chassis combined with the boards, implying some sort of interference between the boards and the chassis. The maximum variations in linearity error due to the change of chassis are nearly the same for all the three units, which are about 15 µV and 80 µV for 1-V and 5-V ranges, respectively. Since the chassis replacement might result in considerable change of the linearity for the ADCs, the evaluation of the ADCs done with a specific chassis would not be valid as the chassis is changed. The origin of the chassis dependency has to be further investigated.

VI. ACKNOWLEDGMENT

REFERENCES

[1] G. Rietveld, D. Zhao, C. Kramer, E. Houtzager, O. Kristensen C. de Leffe "Characteriztion of a Wideband Digitizer for Power Measurements up to 1 MHz" IEEE Transactions on Instrumentation and Measurement, vol. 60, no. 7, pp. 2195 – 2201, July 2011.
DOI: 10.1109/TIM.2011.2117330

[2] F. Overney, A. Rüfenacht, J.P. Braun, B. Jeanneret, P.S. Wright "Characterization of Metrological Grade Analog-to-Digital Converters Using a Programmable Josephson Voltage Standard" IEEE Transactions on Instrumentation and Measurement, vol. 60, no. 7, pp. 2172 – 2177, July 2011.
DOI: 10.1109/TIM.2011.2113950

[3] T. Mohring, E. Mohns, M. Schmidt, T. Funck "Characterization of a 2-chanel Digitizer with Differential Inputs", Conference CPEM 2012.
DOI: 10.1109/CPEM.2012.6251041

[4] Mun-Seog Kim, G.W.C. Wijayasundara, Hehree Cho, Hyung-kew Lee "Voltage linearity Evaluation for a High-Speed Digitizer Adapted to a Quantum Sampling Voltmeter" , Conference CPEM 2016.

[5] *National Instruments Flex II ADC Technology - The Flexible Resolution Technology inside the NI PXI-5922 Digitizer, www.ni.com.*