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Digital Reconstruction Stage Implementation of FBD Sigma Delta ADC for SDR Receiver

Ali HAROUN[1], Manel BEN-ROMDHANE[2], Rihab LAHOULI[1,2], Chiheb REBAI[2], Dominique DALLET[1]

[1]IMS Research Lab., University of Bordeaux, Bordeaux INP ENSEIRB-MATMECA, France,
351 Cours de la libération, Bâtiment A31, 33405 Talence.
ali.haroun@ims-bordeaux.fr
[2]GRESCOM Research Lab., SUP'COM, University of Carthage, Tunisia,
Cité Technologique des Communications, 2083 El Ghazala, Ariana.
manel.benromdhane@supcom.tn

***Abstract* – This paper presents a fixed point implementation of a digital reconstruction stage in frequency band decomposition (FBD) Sigma Delta analog-to-digital converter (ADC) which is intended for software defined radio (SDR) multistandard receiver. The implemented architecture is composed of 3 parallel branches for the UMTS use case. The digital reconstruction stage is essentially composed of digital finite impulse response (FIR) filters. In addition, the frequency conversions performed in the digital reconstruction stage are ensured by digital oscillators which are carefully tuned to obtain the required frequencies and phases. These oscillators are dedicated to demodulation and modulation operations. The proposed architecture is digitally implemented on a field programmable gate array (FPGA) target. Then, it is tested thanks to FPGA-in-the-loop (FIL) tool using MATLAB/SIMULINK interface. It allows us to compare our system to the simulation results that are done with MATLAB/SIMULINK in floating point.**

***Keywords*— Sigma delta modulators, frequency band decomposition, digital reconstruction, FPGA.**

I. INTRODUCTION

The aim of the software defined radio (SDR) receiver is to allow multiple communication systems to coexist in a single multistandard radio receiver which is reconfigurable, programmable and compact at the cost of a considerable increase in the constraints on the analog-to-digital conversion stage [1]. The idea of SDR receiver is to place the analog-to-digital converter (ADC) as close as possible to the antenna in order to minimize the RF stage and move the analog problems to the digital stage. Indeed, the ADC has to satisfy a wide range of requirements in terms of bandwidth and dynamic range to satisfy multistandard receiver specifications [1]. This exceeds the technological limits of the currently marketed converters [2-3]. In this context, parallel ΣΔ ADC architecture based on frequency band decomposition (FBD) is an attractive candidate guaranteeing high accuracy with an extension of the bandwidth to meet the requirements of multistandard SDR receiver. The proposed FBD ΣΔ ADC design, presented in [4-5], supports the E-GSM, UMTS and IEEE802.11a standards.

The objective of this work is to implement the reconstruction stage FBD ΣΔ ADC architecture for multistandard SDR receiver on FPGA target. This paper is organized as follows. The digital reconstruction stage is briefly recalled in section II. In section III, we present the architecture of the main blocks of the FBD digital reconstruction stage. In section IV, the logic synthesis results and the digital implementation on FPGA target via FPGA-in-the-loop (FIL) tool using MATLAB/ SIMULINK interface are achieved. A spectrum analysis and implementation results are also discussed in section IV. Finally, conclusions are drawn in section V.

II. DIGITAL RECONSTRUCTION STAGE DESIGN OVERVIEW

A digital reconstruction stage of parallel FBD ΣΔ ADC for SDR receiver was proposed in [5]. The FBD ΣΔ ADC architecture is composed of one branch for GSM, 3 branches for UMTS and 6 branches for IEEE802.11a. The UMTS branches are reused for the IEEE802.11a signal processing. The frequency division plan as well as the ΣΔ modulators details is discussed in [5]. For the first branch, only decimation and low-pass filtering operations are needed. However, for the other branches, in phase (I) and quadrature (Q) paths are needed. Thus, the digital reconstruction stage is composed of bandpass filtering, decimation, demodulation and modulation operations.

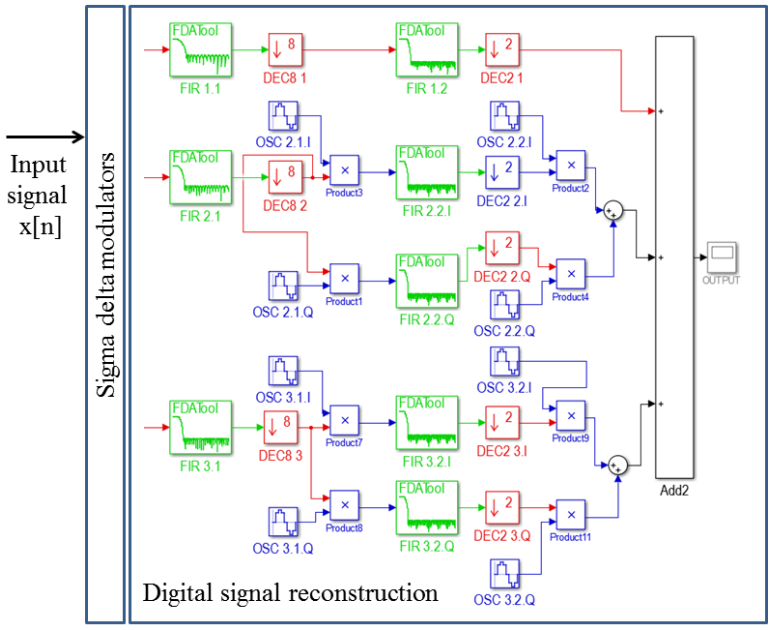

Fig. 1. Digital reconstruction stage of parallel FBD ΣΔ ADC: UMTS use case SIMULINK model.

As far as it concerns the digital filters, there are finite impulse response (FIR) filters and infinite impulse response (IIR) filters. Thanks to their in-band linear phase response and their constant group delay, the FIR filters can achieve smaller in-band signal distortion than IIR filters. Besides, they are unconditionally stable and easier to design. However, for the same constraints, the FIR filters are computationally intensive due to the high number of coefficients [6]. Obviously, IIR filter implementation requires less registers and fewer multiply-accumulate operations. Nonetheless, linear phase for efficient digital signal reconstruction is a requirement in FBD architecture. Therefore, FIR filters are more suited than IIR filters for FBD digital reconstruction stage.

Moreover, in the digital reconstruction stage, decimation is needed to reduce sampling frequency to Nyquist frequency before digital communication algorithms. The decimation operation is always preceded by a decimation filter that serves as an anti-aliasing filter at the down-sampling frequency. To reduce the complexity of such a decimation filter with a high decimation factor, two-stage decimation is performed where the global decimation factor corresponds to the global oversampling ratio (OSR) of the FBD ΣΔ ADC [5]. Besides, the demodulation has to be followed by a filter to attenuate the unwanted frequencies which are due to the multiplication operation. This filter presents high complexity since the unwanted frequencies are at low values and the filter operates at the oversampling frequency of the ΣΔ modulator. To deal with this problem, the authors in [5] opt to place the demodulation operation, which is needed to down-convert the signals to baseband frequencies, after the first decimation stage. Then, after the second stage decimation and filtering operations, the I and Q paths are modulated to return the sub-band signal at its original frequency band. Finally, the sub-band output signals are recombined to obtain the reconstructed signal.

The floating point representation of this architecture is simulated using MATLAB/SIMULINK for UMTS use case. The SIMULINK model of the digital reconstruction stage is illustrated in Fig. 1. The 3 parallel branches are operating at a 72-MHz sampling frequency. The global decimation factor is set to 16. The first stage ensures decimation by a factor of 8 and the second one by 2. This choice allows analog-to-digital conversion of UMTS signals at a 4.5 MHz Nyquist frequency. The first decimation stages use FIR filters whose orders are 29, 39 and 56 for the first, second and third branches, respectively, as designed by FDATool in MATLAB. In addition, to attenuate the overlapping effect due to the second decimation stage, 49-order FIR filters are required in the three branches. However, they are not selective enough to reach 73.8 dB for UMTS dynamic range and 82-order FIR filters in the three branches are necessary to process the UMTS signals.

III. PROPOSED IMPLEMENTATION ARCHITECTURE OF THE DIGITAL RECONSTRUCTION STAGE

The objective of this work is to transform the MATLAB/SIMULINK model of FBD digital reconstruction stage to a hardware description where the filters coefficients and the information flow are represented in fixed point. The hardware description language is the standard VHDL so as to implement the

reconstruction system to either FPGA or ASIC target. First, we begin to describe digital FIR filters. Subsequently, the oscillators (OSC) and decimation (DEC) blocks are described. Then, we present the implementation architectural proposal.

A. FIR blocks

In this sub-section, we are interested on the digital filters. These filters are characterized by a limited number of coefficients which depend on their orders. These coefficients are calculated in floating point using the FDATool in MATLAB. Then, it is mandatory to quantize these coefficients to obtain a fixed-point representation. Therefore, it is possible to provide a physical description using a synthesizable VHDL code for a digital filter. This takes us to describe a standard VHDL code to implement the architecture on any FPGA target.

Generally, the FIR filter is described by the linear combination given in (1),

$$y(n) = \sum_{k=0}^{N} b_k x(n-k) \tag{1}$$

where $x(n)$ represents the value of the input signal, $y(n)$ the value of the FIR output signal and b_k designs the filter coefficients for $k \in [0, N]$ with $N+1$ the order value. The digital filters can be implemented using three basic operations. They are the multiplying element, the summing element and the unit delay element. These elements are sufficient to achieve all possible linear digital filters. For example, we take the case of the low pass filter located on the first branch of the reconstruction stage whose order is equal to 29 (FIR 1.1). The proposed architecture for this FIR filter contains real multipliers, real adders and registers as illustrated in Fig. 2.

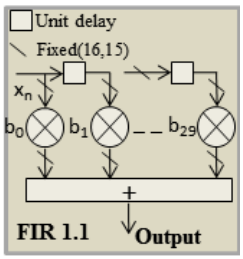

Fig. 2 Architecture of the 29th order FIR filter.

In addition, the description of such architecture in VHDL uses a fixed-point representation of the coefficients' values b_k calculated by FDATool. They are then quantized and coded using 16 bits where 15 bits are assigned to the fractional part. Likewise, adders, multipliers and registers are implemented with 16-bit resolution where 15 bits are assigned to the fractional part. In this proposal, we describe a pipelined architecture [7] that involves multiplying each input signal which is shifted *k* times by the filter coefficient b_k. The FIR output signal is the accumulation of all the obtained multiplications' results.

B. OSC blocks

The oscillator that is implemented to control the demodulation and the modulation is derived from the digital resonator in [8]. It is based on two integrators connected in a loop as shown in Fig. 3. By carefully choosing the values of the gains, a_{12} and a_{21}, and the initial values in the registers R1 and R2, $x_1(0)$ and $x_2(0)$, the required oscillator frequency, amplitude and phase are tuned. The computation of the gains, a_{12} and a_{21}, is done using (2) where a_{12} is equal to 1, f_s is the sampling frequency and f is the oscillator frequency.

$$a_{21} = 2(1 - cos(2\pi f/f_s)) \tag{2}$$

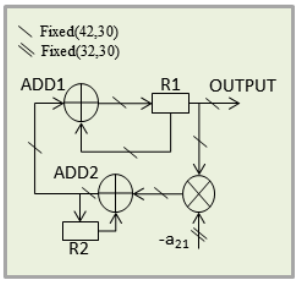

Fig. 3. Conventional digital resonator architecture.

The amplitude, A, and the phase, φ, of the digital oscillator, are tuned using the initial values in the registers, $x_1(0)$ and $x_2(0)$. These parameters, $x_1(0)$ and $x_2(0)$, are then computed as given by (3) and (4).

$$x_1(0) = A\,sin(\varphi) \tag{3}$$

$$x_2(0) = \frac{1}{a_{12}}\left[A\,sin\left(\frac{2\pi f}{f_s} + \varphi\right) - (1 - a_{12}a_{21})\,x_1(0)\right] \tag{4}$$

To more explain how oscillator parameters are computed, let us consider the second-branch demodulation oscillators. In the proposed FBD ΣΔ-based ADC architecture, these oscillators are placed after the first decimation by a factor of 8. These oscillators operate at a sampling frequency equal to $f_s/8$ where f_s is equal to 72 MHz. The oscillation frequency is set at 1.1 MHz which is the second branch central frequency. Therefore, a_{12} and a_{21} are the same for the two oscillators since the gain a_{12} is always equal to 1 and a_{21} is computed using (2) by replacing f_s in the equation by $f_s/8$ but also by taking f equal to 1.1 MHz. Thereafter, the gain a_{21} is equal to 0.5613 for an accuracy of four values after the

decimal point. Besides, the oscillators signal amplitude, A, is set to 2. Furthermore, the initial phase, φ, is set to 0 and $\pi/2$ respectively for the in-phase and in quadrature oscillators. Therefore, $x_1(0)$ is computed using (3). The obtained values are 0 and 2 respectively for the in-phase and in quadrature oscillators. The parameter $x_2(0)$ is computed by using (4). It is equal to 1.3893 and 0.5613 for the first and second oscillator respectively for an accuracy of four values after the decimal point. Otherwise, the modulation oscillators operate at $f_s/16$ sampling frequency. Thus, parameters configuration for those oscillators are evaluated in the same way as for demodulation oscillators for $f_s/16$ sampling frequency.

The architectural description of the oscillator block contains two adders, two registers and one multiplier as shown in Fig. 3. The gain, a_{21}, is quantized on 32 bits where 30 bits are assigned to the fractional part. This precision is needed to reach the required oscillator frequencies which correspond to the central frequencies of the FBD branches sub-bandwidths. However, adders and registers are implemented with 42-bit resolution where only 30 bits are assigned to the fractional part to avoid the saturation of these components.

C. DEC blocks

After the FIR filters and oscillators implementation of the digital reconstruction stage architecture, and to complete our architectural proposal, it remains to implement the decimators by a factor of eight and those by a factor of two. The principle of such decimators is very simple, it consists of under sampled the output signals coming out from FIR filters by choosing one among eight samples in the case of decimator by a factor of eight and one among sixteen in the case of that factoring by two. Note that, we choose one sample among sixteen for the decimator by a factor of two if we synchronize the system with a sampling frequency f_s. To do this, a counter modulo 8 and a counter modulo 16 are implemented respectively for the decimator by a factor of eight and the decimator by factor of two. In Fig.4, we present the architecture of the decimator by factor of eight. It contains one register with 16-bit resolution controlled by a counter modulo 8. We use the same architecture for the decimator by factor of two by using a counter modulo 16.

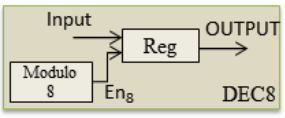

Fig. 4. Architecture of decimator by a factor of 8.

D. Implementation global architecture

Our implementation architectural proposal of the digital reconstruction stage is illustrated in Fig. 5. As the MATLAB/SIMULINK model, it is composed of three branches. The first branch contains two digital filters (FIR) and two decimators by factor of 8 (DEC8) and by factor of two (DEC16). The other two branches contain also two oscillators (OSC) to perform the operations of demodulation and modulation. In addition, we implement in this architecture RAM memories for storing the coefficients of the FIR filters, some multipliers and adders to perform some arithmetic operations. Besides, counters modulo 8 and 16 are used to perform the decimation stages by 8 and 2, respectively.

In the next section, implementation results of the digital reconstruction stage are presented and discussed.

IV. DIGITAL RECONSTRUCTION STAGE IMPLEMENTATION RESULTS

The proposed implementation architecture of the FBD digital reconstruction stage is tested in this section using FPGA-in-the-loop (FIL) tool. This tool takes VHDL description code to implement any architecture on FPGA target using SIMULINK interface. The experimentation is performed with a Virtex-6 FPGA XC6VLX240T. From the VHDL description, we generate the programming file that is uploaded on the FPGA board. Then, the test is operated by a FIL block which is generated by using the programming file and inserted in the SIMULINK model. Indeed, the simulation for the FIL block is performed by communicating its inputs and outputs to the SIMULINK data. The MATLAB/SIMULINK model and FIL simulations are performed so that we can compare the implementation results to floating-point simulation results. The simulation results of the MATLAB/SIMULINK model in floating-point representation and its equivalent implementation on the Virtex-6 FPGA are presented in Fig. 6.

To estimate the hardware complexity of the proposed architecture, FPGA logic synthesis is done in the Xilinx ISE environment. The test is performed with the Virtex-6 FPGA XC6VLX240T-1FF1156. Initially, we estimate the complexity of FIR blocks that need 9152 slices (3304 LUTs and 619 flip-flops), and 494 DSP48 blocks as given in Table 1. Implementation results are also given for each FIR filter. Besides, maximum frequencies for the FIR filters are presented and it is shown that FIR 1.1, FIR 2.1 and FIR 3.1 cannot reach 72 MHz. In fact, that is due to the high number of coefficients that increases the critical path. Moreover, the filters of the second decimation stage deliver data at 8.2 MHz which is also lower than the required 9 MHz for the proposed architecture. Therefore, we propose in future work to improve the maximum frequency by proposing other architectures to minimize the critical path. For example, we cite the polyphase architecture and the transposed architecture. These architectures provide a good compromise between throughput and hardware complexity.

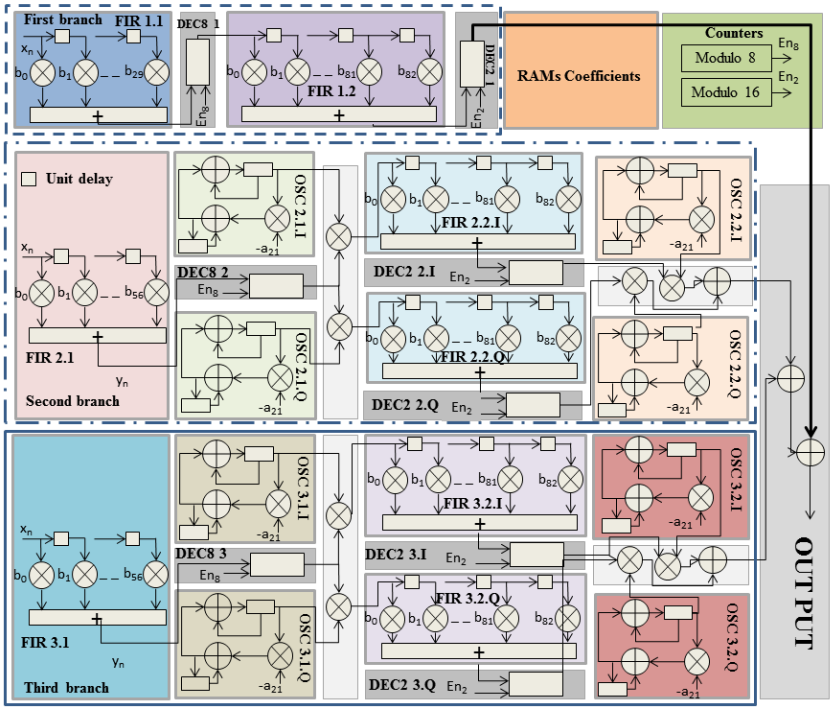

Fig. 5. Implementation architecture of the digital reconstruction stage of parallel FBD ΣΔ ADC.

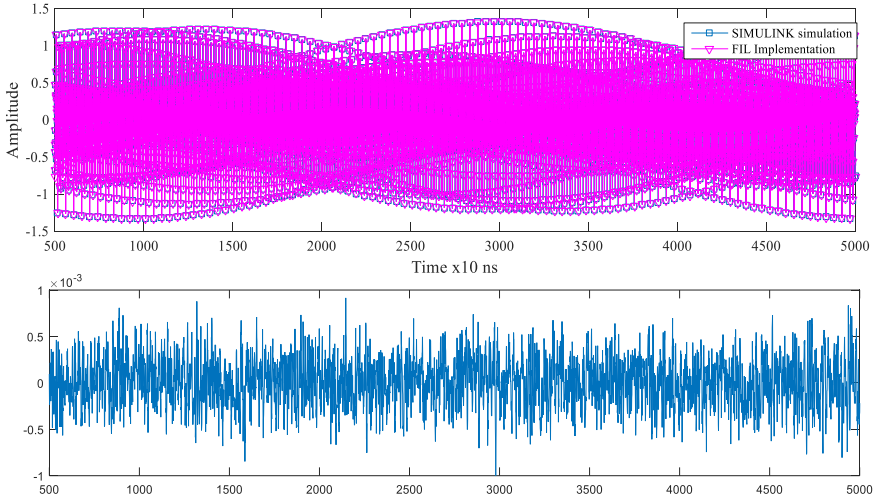

Fig. 6. Output signals of the SIMULINK model versus FIL (up), relative error between SIMULINK model and FIL (down).

Table 1. Synthesis results for the FIR blocks.	FIR 1.1	FIR 1.2	FIR 2.1	FIR 2.1.I	FIR 2.1.Q	FIR 3.1	FIR 3.1.I	FIR 3.1.Q	All FIRs
Slices	544	1392	672	1392	1392	976	1392	1392	9152
LUTs	127	580	156	563	563	189	563	563	3304
Flip-flops	41	94	47	96	96	53	96	96	619
DSP48s	28	73	38	75	75	55	75	75	494
Maximum frequency (MHz)	19.51	8.43	14.92	8.20	8.20	10.79	8.20	8.20	8.20

In a second time, the complexity of digital reconstruction stage FBD is estimated. It needs some multipliers that can be implemented in DSP48 blocks. Indeed, the architecture of the digital reconstruction stage FBD consumes 11219 slices (1344 flip-flops and 4603 LUTs), and 558 DSP48 blocks as given in Table 2. It is shown that the reconstruction stage needs a very important number of DSP48 blocks that represents 72 % of available blocks. Therefore, we have to adopt filter optimization solutions such as polyphase filters. Indeed, other digital circuits will be implemented as the ΣΔ modulator and digital communications algorithms.

Table 2. Synthesis results for the digital reconstruction stage.

	Used	Available	Utilization
Slices	11219	301440	3%
Flips Flops	1344	14478	9%
LUTs	4603	150720	3%
DSP48 blocks	558	768	72%

Finally, to test the reconstruction stage implementation, a multi-tone input signal, composed of three sine-wave signals, is applied at the input of the FBD architecture. The sine-wave frequencies are 300 kHz, 800 kHz and 1900 kHz which are in first, second and third sub-bandwidth, respectively. The sine-wave normalized amplitude is set at 0.45. The normalized amplitude is defined as the input amplitude out of the power supply voltage. The recombined global output signal spectrum of the FBD ΣΔ-based ADC for FIL on Virtex-6 FPGA and the obtained spectra from MATLAB/SIMULINK simulation are compared in Fig. 7.

The signal-to-noise ratio (SNR) of this output signal is computed in both of the implementation and simulation results. The obtained value from the simulation results is greater than the obtained value from the implementation solution. This lower value is due to quantization noise effect of the fixed-point representation.

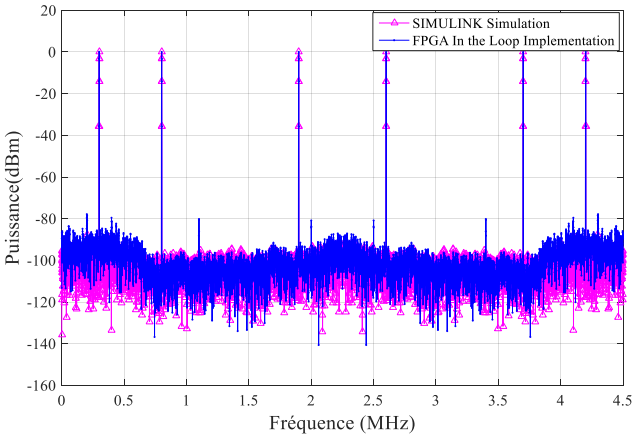

Fig. 7. Spectrum of the recombined output signal.

V. CONCLUSIONS

In this paper, we propose the architecture in fixed-point representation of the digital reconstruction stage for the FBD ΣΔ-based ADC for multistandard SDR receiver. The proposed architecture is based on demodulation that brings the ΣΔ modulators outputs to baseband before proceeding to the second-stage decimation. The parallel signals are then modulated and combined to form the global output signal. The digital reconstruction stage is implemented on FPGA for the UMTS use case. Then, we perform FPGA-in-the-loop verification with Virtex-6 FPGA board using MATLAB/SIMULINK environment. Simulation results and output signal spectrum show that the proposal is good enough for the UMTS required dynamic range. The proposed architecture implementation consumes a large amount of DSP blocks. Therefore, as future works, we will optimize filters implementation by decimating their outputs and by using polyphase structure of filters to increase the maximum frequency.

VI. ACKNOWLEDGMENT

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REFERENCES

[1] A. Maalej, M. Ben-Romdhane, C. Rebai, A. Ghazel, P. Desgreys, P. Loumeau, “Towards time-quantized pseudo-random sampling for green communication,” IEEE Trans. on Cir. and Sys. II, vol. 61, no. 6, pp 443-447, Jun. 2014.

[2] B. Murmann, “A/D converter trends: Power dissipation, scaling and digitally assisted architectures, ” IEEE Custom Integrated Circuits Conference, pp. 105-112, 2008.

[3] B. Murmann, ADC Performance Survey 1997–2015 [Online] : http://www.stanford.edu/~murmann/adcsurvey.html 2015

[4] R. Lahouli, M. Ben-Romdhane, C. Rebai, D. Dallet, “Towards flexible parallel sigma delta modulator for software defined receiver,” IEEE Int. Instrum. and Meas. Technology Conf., May 2014.

[5] R. Lahouli, M. Ben-Romdhane, C. Rebai, D. Dallet, “Digital reconstruction stage of the FBD ΣΔ-based ADC architecture for multistandard receiver,” IMEKO TC4, 2014.

[6] D. Marković, R. W. Brodersen, DSP Architecture Design Essentials, Springer Science & Business Media- Technology & Engineering, ISBN 9781441996602, 2012.

[7] T. S. Chang, C. W. Jen, “Hardware-efficient pipelined programmable FIR filter design, ” IEE Proc. Comp. and Digital Techniques, vol. 148, no. 6, pp. 227-232, 2001.

[8] W.-B. Lin, B.-D. Liu, “Multitone signal generator using noise-shaping technique,” IEEE Proc. Circuits, Devices and Systems, vol. 151, pp. 25-30, 2004.