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FPGA-synthesizable Filter Model Based Bitstream DAC for Hardware-in-the-Loop Simulators

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***Abstract* – The advances in FPGA technology have enabled fast real-time simulation of power converters, filters and loads. HIL (Hardware-in-the-Loop) simulators taking advantage of this technology have revolutionized control software and hardware development for power electronics. HIL simulators can reproduce the same analogue signals that would be measurable on real power converter circuits. A very common limitation in these applications is the usable pin count of the FPGA, because many analogue signals are needed and there are other functions as well. Switching frequencies in today's power converters are getting higher and higher, so the emulated current signals' frequencies are also increasing. Σ-Δ DACs provide an efficient, FPGA-synthesizable solution using a single pin for each output, but the output signal's bandwidth and latency is usually not sufficient, because of the used analogue filters. The subject of this paper is to introduce a new bitstream DAC architecture, which is capable of reproducing higher frequency current signals (usually triangle waves) more accurately than traditional Σ-Δ solutions.**

***Keywords* – Σ-Δ DAC, HIL simulation, FPGA**

I. INTRODUCTION

General power converters consist of two main parts: a power stage (main circuit) and a digital controller unit, which is usually realized using a DSP or FPGA. Testing such a controller unit on its original main circuit is expensive and dangerous. Because of this, offline computer simulation is often used for testing such converters [1] [2]. There are very precise models for offline simulation (e.g. PSPICE based simulators), but they can be only used for initial testing of the control algorithms, not the implementation. A low-power model of the main circuit can be built under laboratory conditions, but it will have parameters (time constants and quality factors) differing from the ones of the original system.

A very effective way to test controller units' both hardware and software is HIL (Hardware-In-the-Loop) simulation [3]. It combines the advantages of other testing methods: low cost like offline computer simulation, complex tests like laboratory testing and realistic conditions like testing on the field. HIL technology also allows the simulation of rare events like failures of certain components which otherwise would be hard to test on an ordinary test bench.

The main concept of using HIL simulation in power electronic systems is that computational models replace the high-power parts of the system [4] [5]. HIL simulators are typically realized using FPGA circuits [5] [6]. The simulated parts are connected through real physical interfaces like analogue and digital channels to the control boards under development, so the boards can be tested and validated in their seemingly real environment. A good HIL simulator is completely transparent for the controller unit, so that the controller is unable to distinguish between the simulator and a real system. Therefore HIL simulation can significantly shorten development time and reduce costs [6].

Nowadays and in the near future, switching frequency of power converters is increasing, especially when silicon carbide semiconductor devices are spreading [7].

Switching events usually affect currents directly, so triangle waveforms are common in current signals. The main component of controller units is the current controller [6], which needs to react fast for current changing. That's why accurately reproducing these triangular current signals are one of the most critical tasks in HIL simulators. Other analogue outputs' bandwidth are usually lower.

In a typical HIL simulator, often 20-30 analogue outputs are required and there are many other important functions: PWM inputs, sensor emulation, communication buses, etc. The number of available I/O pins on common FPGA development boards usually becomes the most limiting factor when designing a HIL simulator. The use of a self-designed FPGA card would prolong the development process, which is contradictory to the original aim.

The optimal solution for these requirements is some kind of Σ-Δ DAC [8]. It is effectively synthesizable in an FPGA, requires only an additional analogue low-pass filter circuit. It uses only one FPGA pin (unlike external DACs with parallel or serial interfaces) and the achievable accuracy is mostly sufficient. However, the low-pass filter adds phase latency to the output signal and limits its bandwidth significantly.

The subject of this paper is an improved bitstream DAC, which eliminates most of these side effects, also FPGA-synthesizable and requires the same filter circuit as a traditional Σ-Δ DAC.

II. RELATED RESULTS IN THE LITERATURE

The simplest type of Σ-Δ DACs uses the first order Σ-Δ modulator as well as the Σ-Δ ADCs. Note that in the literature more research has been done to the ADCs, but most of the results can be applied to DACs as well. Many papers deal with Σ-Δ modulators in general, covering the ADC and DAC topics as well.

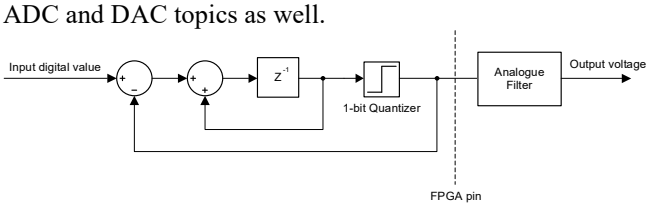

Fig. 1. First-order Σ-Δ DAC

The first-order Σ-Δ DAC can be seen in Fig. 1 [8]. It contains a discrete-time integrator before a 1-bit quantizer (DAC), which converts the data into a bitstream. The bitstream is subtracted from the input, so the integrator processes only the differences. The average of the bitstream is proportional to the digital input value, so a low-pass analogue filter on the output pin restores the desired analogue signal.

The converter is operated with much higher frequency than the Nyquist-frequency of the input signal, which is called oversampling [8]. The quantization noise distributes over a wider spectrum and less remains in the useful signal spectrum after the filtering. This method is called noise shaping and it is an important advantage of Σ-Δ converters [9]. The other useful feature is the guaranteed linearity [8], which is caused by the 1-bit DAC and the averaging method.

Increasing the oversampling frequency the SNR (Signal to Noise Ratio) also increases. The other possibility for improvement is the use of a higher order modulator loop for noise-shaping. A second-order Σ-Δ DAC can be seen in Fig. 2.

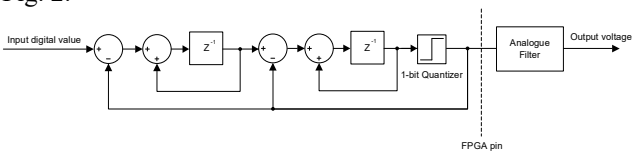

Fig. 2. Second-order Σ-Δ DAC

As the order of the noise shaping increases, more noise will be shifted to higher frequencies of the output spectrum and the output signal after the filter will be more accurate [9].

It is possible to construct higher order Σ-Δ converters, but there can be instability issues with three or more integrators in the loop because of their phase delays. Instead using of higher order loops, multi-staged converters made of first- or second-order loops have become popular. This alternative approach is called MASH (Multi-stAge-noise-SHaping) [9]. An example DAC can be seen in Fig. 3 [10].

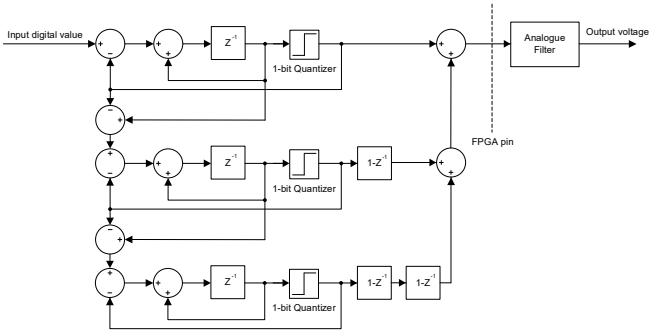

Fig. 3. MASH Σ-Δ DAC

The basic idea of that structure is that consecutive Σ-Δ loops process the quantization noise of the former one. The difference of the integrator's and the quantizer's output gives the quantization error of the modulator, which is lead to the next stage. On the output of the integrators, the same number of digital differentiators are required. This example is a third-order one, although higher order MASH DACs can be constructed [11].

All these Σ-Δ architectures can be used with a general N-bit quantizer on their outputs, not only a 1-bit one. Using more bits naturally increases SNR and makes lower

oversampling ratio possible but also reduces linearity [8].

All of these advantages make Σ-Δ converters popular mainly in audio applications. High resolution (16-24 bits are typical) is achievable relatively easily and with a simple analogue circuit. FPGA-implementation of these DACs are also common, because of the simple external circuit requirement [12] [13] [14], using FPGA pins as 1-bit DACs.

However, for HIL simulators, the output latency is also an important parameter. However, the output analogue filter with low cut-off frequency increases the SNR, but causes significant latency and removes higher order components from the output signals, if the oversampling frequency is limited.

III. DESCRIPTION OF THE METHOD

The output bandwidth of Σ-Δ DAC is limited by the applied analogue low-pass filter at the output. In order to reduce the output fluctuation and increase SNR the time constant of the filter cannot be decreased arbitrary. The output fluctuation depends on the filtering and the operating frequency of Σ-Δ DAC. The latter is limited by the hardware technology (mostly the external circuit). With current technology the clock frequency can be up to 50 MHz typically.

The common switching frequency of high power converters is in the range of 10-100 kHz. For realistic current ripple emulation the bandwidth of the DAC should be at least an order of magnitude greater than this frequency. The cut-off frequency of the commonly used Σ-Δ DAC analogue filter is below this frequency because of the output fluctuation limitation. The aim of the presented new DAC architecture is to compensate the low-pass characteristic of the analogue filter.

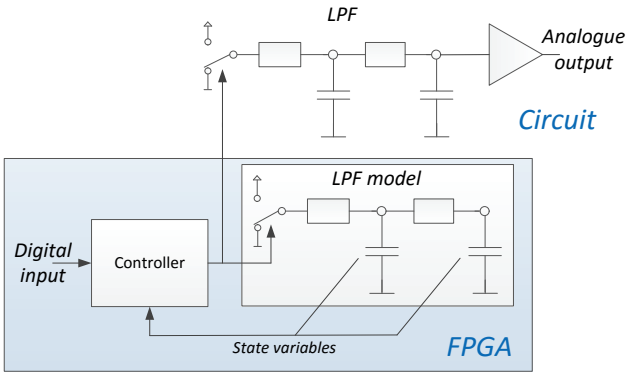

Fig. 4. Main architecture of the filter model based DAC

The main architecture of the DAC can be seen in Fig. 4. By taking advantage of the high resources of the current FPGA technology the dynamic model of the output filter can be implemented. The used filter is a second-order RC low-pass filter in this study. A controller calculates the bitstream from the N bit wide digital input and the filter model's state variables. According to the bitstream on the FPGA pin the analogue output is generated by the low-pass filter and the state variables of the filter model are calculated. By applying a controller architecture which is insensitive to the uncertainty of the filter's parameters the identity of the modelled and the real analogue output signals can be assumed.

The FPGA synthesizable discrete time model of the second-order RC low-pass filter can be seen in Fig. 5, where ΔT is the period of the DAC clock frequency, τ is the time constant of the low-pass filter. The two state variables are calculated using the Forward-Euler discretization method which requires the least resource for the implementation.

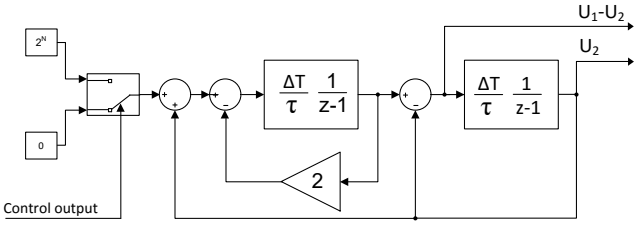

Fig. 5. Low-pass-filter model

The controller architecture can be seen in Fig. 6. Error signal generated from the subtraction of the input reference signal and the calculated output of the filter model (U_2). The controller contains a proportional part with pP coefficient. This error signal is also lead to a saturated integrator part with pI coefficient, which ensures that the long term average of the bitstream will equal to the input conversion value. For fast dynamic response of the DAC the discrete differential values of the conversion value and the filter model's output are used for bitstream generation as well, with pD coefficient. The differential value of the calculated U_2 voltage (the charging current of the last capacitor) is proportional to U_1-U_2, which is used in the controller instead of re-differentiate the output voltage. The conversion value needs to be differentiated separately.

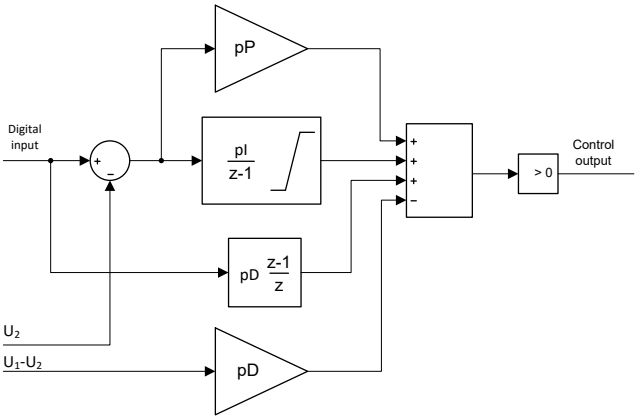

Fig. 6. Controller architecture

IV. TEST RESULTS

The proposed DAC architecture was verified with both simulation and measurement. From the aspect of the output bandwidth and dynamic behaviour, the three DAC types introduced in Section II are roughly the same, the difference is only in the oversampling frequency ripple and the SNR. This is because all of them produces output bitstream with average voltage meeting the required conversion value. The settling time of these DACs depends only on the output analogue filter, signal components above its cut-off frequency are not possible to produce. In the tests the new filter-model based DAC were compared to the traditional first-order Σ-Δ DAC seen in Fig. 1.

The test circuit consists of a second-order R-C filter followed by an operational amplifier on the digital output pin of the FPGA. The schematic of the circuit can be seen in Fig. 7, and the circuit parameters in Table 1. It was the same for the two bitstream type DACs.

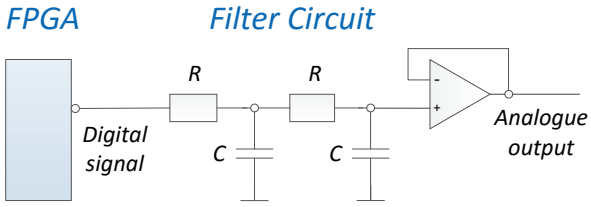

Fig. 7. Test circuit schematic

Table 1. Parameters of the test circuit

Name	Sign	Value
FPGA clock frequency	f	12.5 MHz
Filter resistance	R	130 kΩ
Filter capacitance	C	100 pF
Time constant of the filter	τ	13 µs
Cut-off frequency of the filter	f_c	12.24 kHz
DAC resolution	N	12 bits
DAC full scale voltage	U_{FS}	5 V

The model of the analogue filter was also built in Matlab/Simulink, which is an excellent offline simulation environment and HDL code can also be generated directly for FPGA circuits [6]. Therefore simulation and measurement results are expected to be very similar.

The simulation results can be seen in Fig. 8. The test signal was a triangular wave with a frequency of 10 kHz, amplitude of 610 mV_{pp} and offset of 2.44 V. In other words, the conversion value changed between 1750 and 2250.

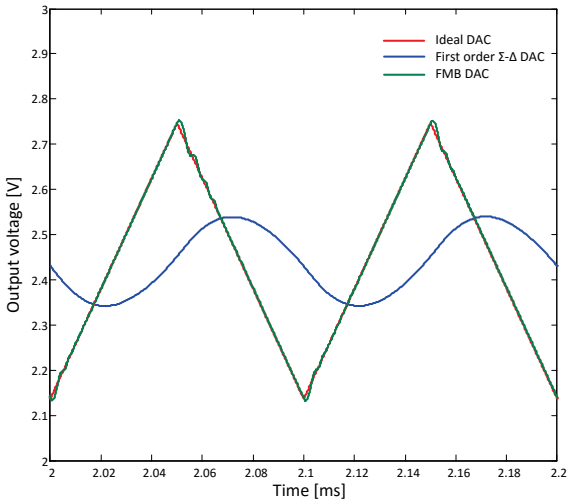

Fig. 8. Simulation result of different DAC output signals

As it can be seen, the first-order Σ-Δ DAC cannot reproduce the reference signal because it contains higher frequency harmonic components than the cut-off frequency of the analogue filter. In contrast to the Σ-Δ DAC, the presented new filter model based DAC can generate the input signal quite accurately, without significant phase delay and amplitude error. However, small ripples can be seen after the peeks of the triangle wave, which slightly decreases the SNR. These ripples are caused by the controller unit in the new DAC, which is tuned to achieve fast settling time, therefore some overshoot occurs when the conversion value (or its differential) changes rapidly.

It can be also observed in the step response of the circuit, which is in Fig. 9. The first-order Σ-Δ DAC reaches the required voltage very slow, defined by the step response of the filter. In contrast, the filter-model based DAC settles much faster, with a small overshoot, compensating the low bandwidth of the filter.

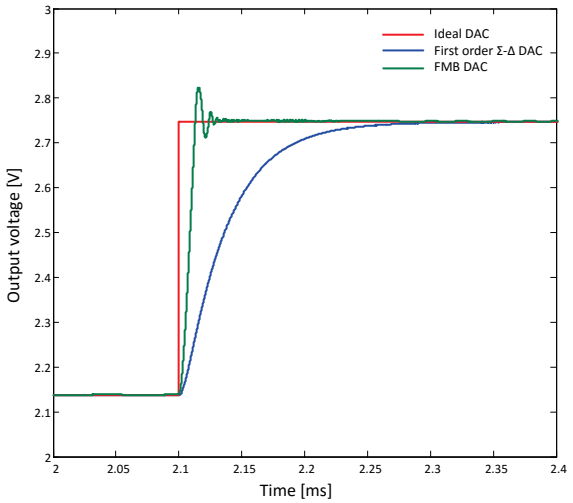

Fig. 9. Step response of the DACs

In the target application, these triangular shaped output signals are typically parts of current control loops, so minimal phase delay is an important requirement. The controllers usually sample the average or peak values of the current signals, so the ripples in the triangular signal in Fig. 8 are acceptable. Square waves are not common in power converters' feedback signals, so the new DAC does not needed to be optimized for them.

The main benefit of the new DAC architecture is that it can compensate the low bandwidth of the output analogue filter. This behaviour was examined quantitatively with another simulation. Using sine waves for test signals with different frequencies on both DACs can show the frequency characteristics of the converters.

For this simulation the sine waves' frequency was changed between 100 Hz and 100 kHz. With each excitation, a FFT was done with the output signal to calculate the exact amplitude and phase of the fundamental harmonic component (the distortion of the original sine wave). From this data, the Bode-diagram of the converters can be made. They can be seen in Fig. 10 and Fig 11.

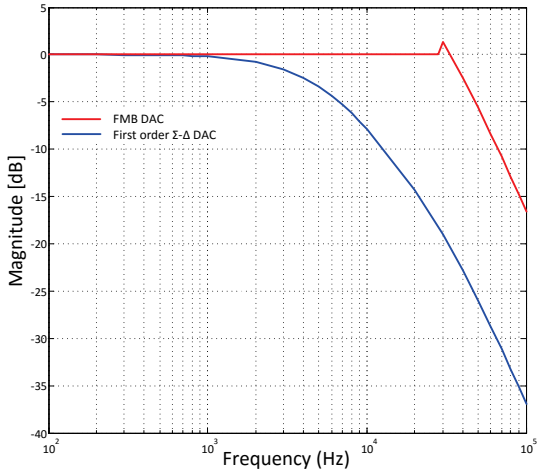

Fig. 10. Bode magnitude diagram of the DACs

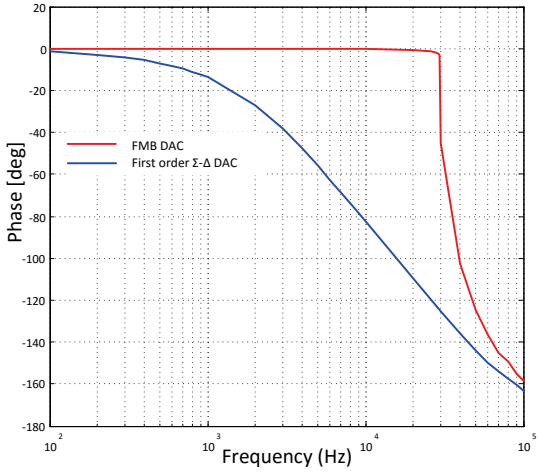

Fig. 11. Bode phase diagram of the DACs

The first-order Σ-Δ DAC's amplitude and phase characteristics is nearly identical to a typical second-order low-pass filter's Bode-diagram. In contrast, there is a measurable improvement with the filter model based DAC. The low-pass effect is fully compensated up to 30 kHz, even a small positive gain is measurable at this frequency. Above this, phase delay is increasing dramatically. This test also shows that for a 10 kHz triangle wave the new solution should give much better results than the traditional Σ-Δ DAC.

After simulation, measurements with the real circuit on Fig. 7 was done. The test signal was the same triangle wave as in the simulation. As a reference signal, the output of an AD9115BCPZ type parallel interfaced DAC was used. It was driven with 50 Msps, so its bandwidth is sufficient to consider it an ideal DAC in the 10 kHz frequency domain.

The results can be seen in Fig. 12. A 20 MHz bandwidth limit was set on the oscilloscope channels to remove the environmental noise from the signals. It does not affect the results, because this frequency is several orders of magnitude higher than the cut-off frequency of the low-pass filters. It is clearly visible, that the measurements show high degree of similarity with the simulation results on Fig. 8, the same conclusions can be drawn from it.

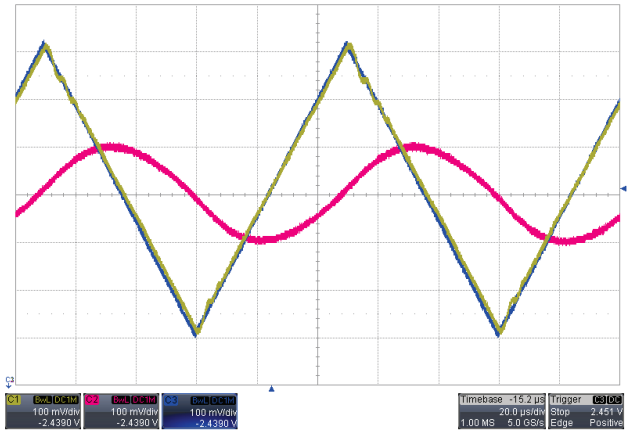

Fig. 12. Measurement result of different DAC output signals

Another important question about the new DAC is the implementation cost, how many FPGA resources are needed for realization? Table 2 shows the resource usage for one instance of the traditional first-order Σ-Δ DAC and the new filter model based one. The used FPGA is a Xilinx Artix-7 XC7A200T-2FBG676, both DACs has a resolution of 12 bits.

Table 2. FPGA resource usage of the DACs

DAC type	LUTs	Registers	DSP slices
First-order Σ-Δ	76	15	0
Filter model based	273	80	7

The used FPGA has 740 DSP slices, 269200 registers and 134600 LUTs in total. In Xilinx 7 series FPGAs, each

DSP slice contains a 25x18 bits 2's complement multiplier [15]. These multipliers are responsible to do the required calculations for the filter model and controller in Fig. 5 and Fig. 6, which is obviously unnecessary for the first-order Σ-Δ DAC. With some optimization on the multiplier factors, they could be approximated by a factor of 2, reducing the DSP slice usage.

It is clearly visible, that the new DAC uses 4-5 times more resources than the simple integrator-based one, but, considering today's FPGA capabilities, it seems to be an acceptable trade-off for the improved bandwidth.

V. NOVELTIES IN THE PAPER

The main contribution of this paper is to present a new bitstream DAC architecture, which is capable of generating analogue signals with higher frequency components than the cut-off frequency of the applied output filter. In other words, it compensates the effect of the filter, increasing the bandwidth of the output signal, compared to the traditional Σ-Δ DACs with the same analogue filter.

The target application is Hardware-In-the-Loop simulators, so the new DAC is optimized mainly for triangular waveforms and settling time, not the SNR.

VI. CONCLUSIONS

A filter model based controller approach was used to create a new bitstream DAC architecture, optimized for FPGA-based HIL simulators, which is verified by simulation and measurement. The new DAC offers improved bandwidth compared to the traditional bitstream solutions, however, it requires more internal FPGA resources. It is ideal for applications with limited FPGA pin count and low-cost external hardware.

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