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A Method to Reduce Influence of Gain Errors and Offsets of Internal Components on Performance of Adaptive Sub-ranging ADCs

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Abstract **– The paper proposes a method of designing and calibrating of an adaptive sub-ranging ADC that is robust to both gain errors and offsets of the components of its analog part, which may simplify and reduce the costs of manufacturing of adaptive ADCs. For facilitation of postproduction calibration, we propose a method of measurement of the actual gain and offset of particular analog tracts used in subsequent stages of conversion, that utilizes the sub-ADC already present in the analog part of the adaptive ADC. Efficiency of the proposed approach is discussed and evaluated on the basis of the results of simulation experiments.**

Keywords – sub-ranging ADC, adaptive ADC, calibration, gain and offset estimation

I. INTRODUCTION

Today, possibilities of improvement of analog-to-digital converters (ADCs) [1],[2] seem to be, to a large extent, exhausted. An exception are adaptive sub-ranging ADCs [3]-[8], which still offer unexploited resources and possibilities for improvements that have been recently investigated in numerous researches, e.g.[3]-[8]. Adaptive sub-ranging conversion is an extension of the well-known conventional sub-ranging method of analog-to-digital (A/D) conversion ([1], [2]), whose main advantage is a good compromise between speed, resolution, complexity and power consumption, which gives conventional sub-ranging ADCs a decent share in the contemporary ADC market. New, unique features of the adaptive sub-ranging ADCs, mainly actual *computing* of intermediate codes and the resulting possibility to set gain values of the internal amplifiers to arbitrary values (not only integer powers of two), create a possibility to improve conversion quality measures beyond the values achievable by conventional sub-ranging ADCs and limited mainly by their simple “bits shifting” method of codes forming (see e.g. [5] for deeper explanation on the advantages of the adaptive over the conventional sub-ranging ADCs).

However, iterative way of functioning of the sub-ranging ADCs makes them very sensitive to imperfections of the analog components used in each iteration of conversion (among them the deviations of gains values from the nominal values and offsets of various components of the analog tract). This results in the unwelcome very high requirements to precision of their analog components. Even when precise components are used, it is not possible to fully eliminate gain errors and offsets and their disadvantageous influence on quality of conversion. That is why in conventional sub-ranging ADCs, aside increasing sizes and complexity of analog components, designers introduce redundancy in form of using only some of the bits obtained in subsequent cycles of conversion. Less significant bits are due to these errors not fully reliable and have to be verified and possibly corrected with use of digital algorithms [1], which slows down the speed of conversion.

Our studies show that transition to adaptive version of the sub-ranging converter [3]-[8] creates possibilities of a more efficient tackling of the problem of imperfections of its components, allowing significant reduction of the requirements on the precision of analog components. In our earlier researches on reduction of the influence of amplifiers gains errors and offsets, due to high complexity of analysis, each of the two factors were considered separately. The knowledge gained from these researches allow us now to formulate the task of joint analysis and more efficient simultaneous reduction of the influence of these two factors that always coexist in each sub-ranging ADC and are responsible for the resultant linear distortions of the particular analog tracts.

II. ADAPTIVE SUB-RANGING ADC

Principle of functioning of the adaptive sub-ranging ADC is described on the basis of the block diagram shown in Fig. 1. The analog part is the same as in conventional sub-ranging ADCs. Sampling of the input signal is performed by the sample-and-hold unit (S/H in Fig. 1). The captured input voltage V is held at the S/H output during K cycles (iterations) of conversion. In each k-th cycle, the compensation signal $\hat{V}_{k-1}^{SDAC}$ is subtracted from the input sample V in the subtraction unit (Σ) to produce the residue signal e_k. The compensation signal $\hat{V}_{k-1}^{SDAC}$ is the analog equivalent, formed by the internal D/A sub-converter (SDAC) with N_{SDAC}-bit input, of the estimate $\hat{V}_{k-1}$ of the input voltage V, computed in the previous cycle of conversion. The residue signal e_k is

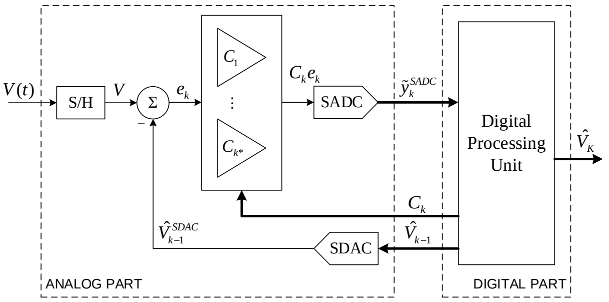

Fig. 1. Block diagram of adaptive sub-ranging ADC.

amplified by the appropriate internal amplifier with gain C_k (value C_k increases in subsequent cycles) from a bank of amplifiers, and quantized by the coarse flash A/D sub-converter (SADC) with N_{SADC}-bit (2-6 bits) output code $\tilde{y}_k^{SADC}$. The sub-code $\tilde{y}_k^{SADC}$ of the amplified residue signal $C_k e_k$, formed by SADC in the current *k*-th cycle, is used in the digital part of the converter to form the intermediate code (estimate) of the input sample according to the following relationship:

$$\hat{V}_k = \hat{V}_{k-1} + L_k \tilde{y}_k^{SADC} - L_k C_k (\hat{V}_{k-1} - \hat{V}_{k-1}^{SDAC}), \qquad (1)$$

where L_k is a digital coefficient whose value corresponds to the value of the gain C_k. The final estimate $\hat{V}_K$ of the input sample V (the final result of its analog to digital conversion)is obtained after K cycles of conversion. In conventional sub-ranging ADCs the codes $\hat{V}_k$ are formed using components that perform simple bit operations, whereas in the adaptive sub-ranging ADC, the codes $\hat{V}_k$ are actually calculated in each cycle of conversion in a simple computing unit.

Optimization of the adaptive ADC consists in development of the method for determining optimal values of the amplifiers gain coefficients C_k and corresponding coefficients L_k in algorithm(1), such that minimize MSE of conversion, or equivalently maximize ENOB (effective number of bits) in each cycle of conversion. Optimal values of coefficients C_k, L_k in case of absence of technological imperfections in the analog part are determined as follows (see [3]-[5]and other works). In the pre-threshold interval of cycles of conversion $(1 \le k \le k^*)$, in which ENOB of adaptive ADC grows fastest - linearly, the parameters C_k, L_k should be set to the following values:

$$C_k = \frac{D}{\Delta_{SADC}/(2 \cdot C_{k-1}) + \Delta_{SDAC}/2 + \alpha\sqrt{2}\sigma_a}, \quad L_k = C_k^{-1}, \quad (2)$$

where D is a half of the input range of SADC; $\Delta_{SADC} = D \cdot 2^{-(N_{SADC}-1)}$ and $\Delta_{SDAC} = D \cdot 2^{-(N_{SDAC}-1)}$ are the quantization intervals of SADC and SDAC, respectively; σ_a^2 is the variance of internal analog noises; α denotes the saturation factor dependent on the assumed permissible probability μ of saturation of SADC ($\mu \ll 1$).

The threshold number of cycles k^* can be assessed as the minimal value of k for which:

$$\Delta_{SADC}/(2 \cdot C_{k-1}) < \alpha\sqrt{2}\sigma_a + \Delta_{SDAC}/2. \qquad (3)$$

In the post-threshold interval of cycles of conversion ($k > k^*$), in which ENOB of the adaptive ADC grows more slowly – logarithmically, the gains C_k can be fixed, but the coefficients L_k should be adjusted continually as follows [5]:

$$C_k = C_{k^*} = \frac{D}{\alpha\sqrt{\Delta_{SDAC}^2/12 + 2\sigma_a^2}}, \qquad L_k = C_k^{-1}\left(1 - \frac{P_k}{P_{k-1}}\right),$$

$$P_k = P_{k-1} - \frac{C_k^2 P_{k-1}}{\sigma_\xi^2 + C_k^2(\Delta_{SDAC}^2/12 + \sigma_a^2 + P_{k-1})}, \qquad (4)$$

where σ_ξ^2 denotes the variance of the SADC quantization noise. Initial condition for (4)is $P_{k^*} = \Delta_{SDAC}^2/12 + 2\sigma_a^2$.

A sub-ranging adaptive ADC designed according to algorithm (1)-(4) is optimal in case of ideal realization of the adaptive ADC but very sensitive to possible imperfections of the analog part, in particular to gain errors and offsets of the analog components.

III. RELATED RESULTS IN THE LITERATURE

This work on one hand develops the results of [3]-[8] and other works, concerning optimization and particularities of functioning of the adaptive sub-ranging ADCs. On the other hand, it investigates a problem of development of efficient methods of reduction of the influence of analog components imperfections that was addressed (and not fully satisfactorily solved) in many works concerning conventional sub-ranging ADCs, e.g. [1], [2].

Let us notice that in subsequent cycles of conversion the errors of the amplifiers gains and analog components offsets increase the range of the signal e_k (either directly or by increasing error in previous estimates $\hat{V}_{k-1}$), which in turn increases the probability of saturation of SADC, i.e. the probability of appearance of large error in the final estimate $\hat{V}_K$. To keep the probability of abnormal errors below the permissible value, the nominal gains C_k need to be diminished. In known sub-ranging ADCs, for this purpose, the gains of the amplifiers in particular cycles are reduced by half [1],[2], which decrements the speed of conversion by as much as 1bit per cycle. This decrement by half is largely excessive, but is necessitated by the principle of forming of output codes in conventional sub-ranging ADCs. Building up output word as a juxtaposition of codes of successive observations $\tilde{y}_k^{SADC}$ imposes a constraint on possible nominal gains C_k values – they have to be exact integer powers of two (as shifting a binary code by several positions is equivalent to multiplying the decimal number it represents, by an integer power of two).

In adaptive sub-ranging ADCs, thanks to a different method of codes forming, i.e. actual computing estimates $\hat{V}_k$ as a result of algebraic operations, in each cycle of conversion, in a computing block, the constraint on possible gains values limiting them to integer powers of two is removed, i.e. gains C_k can take arbitrary values. This creates the possibility to set the gains C_k also to relevant values, not lower than sufficient for elimination of SADC saturations. In this paper, we integrate and extend the results of works [6]-[8], obtained for gains errors and offsets separately, and propose their joint treatment, enabling full linear calibration of all analog ducts of the adaptive sub-ranging ADC and significant improvement of its performance.

IV. DESCRIPTION OF THE METHOD

The proposed method of designing and calibration of the adaptive ADC with minimized influence of gain errors and offsets of the analog components, is based on the approach developed in works[6]-[8], and consists of two stages which are briefly described below.

A. Pre-manufacturing modifications

At design stage, in response to increase of the residue signal e_k:

$$e_k = V - \hat{V}_{k-1}^{SDAC}, \tag{5}$$

caused by the gain errors and offsets (jointly described by variable err_k):

$$\overline{e}_k = e_k + err_k,\ (k = 1,...,k^*), \tag{6}$$

the nominal gains values determined by (2), optimal in absence of the gain errors and offsets, need to be accordingly reduced:

$$C_k^{(safe)} = \gamma_k \cdot C_k, \qquad \gamma_k < 1. \tag{7}$$

Let us note that the coefficients(2), have been chosen in such a way that signal e_k is in each cycle fitted to the input range $[-D, D]$ of the SADC (with probability not lesser than $1-\mu$), hence

$$C_k \cdot \max|e_k| \approx D. \tag{8}$$

The reduced, safe values of gain $C_k^{(safe)}$ and increased values $\max|\overline{e}_k|$ should satisfy the same equation:

$$C_k^{(safe)} \cdot \max|\overline{e}_k| \approx D. \tag{9}$$

Using(8) and(9), we can determine the general formula for the gain reduction coefficient γ_k:

$$\gamma_k = \frac{C_k^{(safe)}}{C_k} = \frac{D}{\max|\overline{e}_k|} \cdot \frac{\max|e_k|}{D} = \frac{\max|e_k|}{\max|\overline{e}_k|}. \tag{10}$$

The value γ_k and the reduced gain values $C_k^{(safe)}$, depend on the maximal values of the adaptive ADC realization errors, which determine the value $\max|\overline{e}_k|$, namely:

- the expected maximal technological deviation δ_k^C of the amplifiers gains, modeled as follows:

$$C_k^{(act)} = C_k^{(ref)}(1+\varepsilon_k), \qquad k = 1,..,k^*, \tag{11}$$

where $C_k^{(act)}, C_k^{(ref)}$ are the actual and the nominal amplifier gain values in the cycle k, respectively; the variable ε_k is the relative gain error assumed to be a random value among realized chips with zero mean, limited to the interval $[-\delta_k^C, \delta_k^C]$,

- the expected maximal value $\delta_k^{off} \cdot D$ of offset modeled as follows:

$$\overline{e}_k^{(off)} = e_k + O_k,\ k = 1,..,k^*, \tag{12}$$

where $\overline{e}_k^{(off)}$, e_k are the signals at amplifier's input with and without offset, respectively; the offset O_k is assumed a random zero-mean value limited to the interval $[-\delta_k^{off} \cdot D, \delta_k^{off} \cdot D]$.

Our previous researches[6]-[8] showed that significant improvement of performance of the non-ideally realized adaptive ADC is obtained when the actual gain values and offsets are measured after the manufacturing of the ADC and taken into account in the conversion algorithm. Determination of the actual gain values and offsets is always performed with some error and these measurement errors will also increase the values $\max|\overline{e}_k|$ in (10), and therefore also need to be taken into account. We have considered them in form of:

- parameter $\tilde{\delta}_k^C$ determining the range of errors of gain measurement $[-\tilde{\delta}_k^C, \tilde{\delta}_k^C]$,
- parameter $\tilde{\delta}_k^{off} \cdot D$ determining the range of errors of offset measurement $[-\tilde{\delta}_k^{off} \cdot D, \tilde{\delta}_k^{off} \cdot D]$.

Table 1.

$$C_k^{(safe)} = \gamma_k C_k^{(ref)}\,, \quad k = 1,..,k^*,\ \gamma_1 = \frac{1}{1+\dfrac{\tilde{\delta}_1^{off} D}{D+\Delta_{SDAC}/2+\alpha\sigma_a}} \cdot \frac{1}{1+\delta_1^C}\,,$$

$$\gamma_2 = \frac{\dfrac{\Delta_{SADC}}{2C_1^{(ref)}} + \dfrac{\Delta_{SDAC}}{2} + \sqrt{2}\alpha\sigma_a}{\dfrac{\Delta_{SADC}}{2C_1^{safe}\left(1-\delta_1^C\right)\left(1-\tilde{\delta}_1^C\right)} + \dfrac{\tilde{\delta}_1^C}{1-\tilde{\delta}_1^C} D + \dfrac{\Delta_{SDAC}}{2\left(1-\tilde{\delta}_1^C\right)} + \alpha\sigma_a\sqrt{1+\left(\dfrac{1}{1-\tilde{\delta}_1^C}\right)^2} + \left(\dfrac{\tilde{\delta}_1^{off}}{1-\tilde{\delta}_1^C} + \tilde{\delta}_2^{off}\right) D} \cdot \frac{1}{1+\delta_2^C}\,,$$

$$\gamma_k = \frac{\dfrac{\Delta_{SADC}}{2C_{k-1}^{(ref)}} + \dfrac{\Delta_{SDAC}}{2} + \alpha\sqrt{2}\sigma_a}{\dfrac{\Delta_{SADC}}{2C_{k-1}^{(safe)}\left(1-\delta_{k-1}^C\right)\left(1-\tilde{\delta}_{k-1}^C\right)} + \dfrac{\tilde{\delta}_{k-1}^C}{1-\tilde{\delta}_{k-1}^C} \dfrac{\Delta_{SADC}}{2C_{k-2}^{(safe)}\left(1-\delta_{k-2}^C\right)} + \dfrac{\Delta_{SDAC}}{2\left(1-\tilde{\delta}_{k-1}^C\right)} + \alpha\sigma_a\sqrt{1+\left(\dfrac{1}{1-\tilde{\delta}_{k-1}^C}\right)^2} + \left(\dfrac{\tilde{\delta}_{k-1}^{off}}{1-\tilde{\delta}_{k-1}^C} + \tilde{\delta}_k^{off}\right) D} \cdot \frac{1}{1+\delta_k^C}\,.$$

Using(10), (5), (1), (11), (12)and parameters δ_k^C, $\delta_k^{off} \cdot D$, $\tilde{\delta}_k^C$, $\tilde{\delta}_k^{off} \cdot D$, one can derive, in a similar way asdescribed in [6]-[8], the formulas for the safe, adequately reduced, values $C_k^{(safe)}$ that are given in Table 1.

The second necessary modification in the pre-manufacturing stage, aside the gains values reduction, is that SDAC should be fed with signal:

$$B_k^{com} = \begin{cases} \hat{V}_{k-1} + \hat{O}_k, & k = 1,...,k^*, \\ \hat{V}_{k-1} + \hat{O}_{k^*}, & k > k^*, \end{cases} \tag{13}$$

instead of just $\hat{V}_{k-1}$ (as in Fig. 1). Variable $\hat{O}_k$ in (13) is the measured value of offset in k-th cycle. The two dependencies in (13) result from the fact that in post-threshold cycles of conversion, the same k^*-th analog tract with the same amplifier (see formula (2)) and the same resultant offset $\hat{O}_{k^*}$, is used. This modification realizes compensation of offsets in the analog part, using SDAC. Application of this modification practically reduces the value $\max\left|\overline{e}_k\right|$ to the value in absence of offset, and is also taken into account in derivation of formulas given in Tab. 1 as a possibility to increase the gains C_k.

B. Post-production calibration

The second, post-production stage of the adaptive ADC calibration consists in measurement of the actual gain values $C_k^{(act)}$ and offsets O_k. Then, on the basis of the estimates $\hat{C}_k^{(act)}$, the coefficients L_k are calculated using (2) and (4); estimates $\hat{O}_k$ are used in (13).

Estimation of the actual value of the gain $C_k^{(act)}$ and effective offset O_k at the amplifier input, in a given stage of conversion, can be performed in multiple ways. We propose to reduce this task to the following one: to determine the gain and output offset of the block “amplifier + SADC”. This allows us to apply the methods of ADC gain and offset evaluation described in IEEE Std. 1241-2010 [9], if only we consider the block “amplifier + SADC” as an ADC with unknown gain $C_k^{(act)}$ and output offset $C_k^{(act)}O_k$.

To estimate the gains and offsets of the particular blocks “amplifier + SADC” for subsequent cycles k, we employed the independently based method described in Sect. 7.4.1 of the standard [9]. Using our notation in the formulas (35) and (36) from [9], we obtain the following relationships for the estimates of gain and offset of the k-th block “amplifier + SADC”:

$$\hat{C}_k^{(act)} = \frac{\Delta_{SADC}(2^{N_{SADC}}-1)\left(\sum\limits_{k=1}^{2^{N_{SADC}}-1} kT[k] - 2^{(N_{SADC}-1)}\sum\limits_{k=1}^{2^{N_{SADC}}-1} T[k]\right)}{(2^{N_{SADC}}-1)\sum\limits_{k=1}^{2^{N_{SADC}}-1} T^2[k] - \left(\sum\limits_{k=1}^{2^{N_{SADC}}-1} T[k]\right)^2},$$

$$\hat{O}_k = \left(T_1 + \Delta_{SADC}(2^{(N_{SADC}-1)}-1) - \frac{\hat{C}_k^{(act)}\sum\limits_{k=1}^{2^{N_{SADC}}-1} T[k]}{2^{N_{SADC}}-1}\right)\frac{1}{\hat{C}_k^{(act)}}, \tag{14}$$

where $T[k]$ are the transition levels between codes k and $k-1$, T_1 is the ideal value corresponding to $T[1]$. Determination ofthe code transition levels $T[k]$ was performed using the method based on the sine-wave histogram test also described in [9] (Sect. 6.4).

In order to be able to use the formulas in Table 1 at the pre-manufacturing stage to determine the safe gain values $C_k^{(safe)}$, we need to know the maximal values of gain and offset measurement errors $\tilde{\delta}_k^C$ and $\tilde{\delta}_k^{off}$. These errors depend on the specific method of gain and offset estimation used at post-manufacturing stage. The way of assessment of these errors for the independently based method (14) with code transition levels determined using the sine-wave histogram test, was given in [10]. However, the analysis of the possibility of application of the solutions proposed in [10]for our needs showed that it is impossible due to the fact that the assumptions made in [10] are not fulfilled in our problem, e.g. the nominal gains are not equal to 1, but range from 1 in the first cycle to even several thousands in the last cycles of conversion, or the number of the output bits in SADC is usually lower than assumed in [10].

Therefore, we decided to evaluate the ranges of the gain and offset measurements errors $\tilde{\delta}_k^C$ and $\tilde{\delta}_k^{off}$ in simulations. We established that the level of the errors depends on the gain values. For that reason, we needed to evaluate these errors for each cycle separately. (In the simulation assessment of $\tilde{\delta}_k^C$ and $\tilde{\delta}_k^{off}$, we should assume some values of the gains which according to the formulas in Table 1 depend on $\tilde{\delta}_k^C$ and $\tilde{\delta}_k^{off}$. This difficulty can be overcome by determining the expected gain values approximately, assuming $\tilde{\delta}_k^C = 0$ and $\tilde{\delta}_k^{off} = 0$ in formulas in Table 1).

The values of $\tilde{\delta}_k^C$ and $\tilde{\delta}_k^{off}$ for a given cycle k can be estimated on the basis of the set of values $\hat{C}_k^{(act),(i)}$ and $\hat{O}_k^{(i)}$ obtained for I realizations of the test signal consisting of a sum of a sine-wave and an additive noise with the variance σ_a^2. Each i-th ($i = 1,...,I$) realization of the test signal is processed by the k-th block “amplifier + SADC” and the results are subjected to the histogram test.The obtained set of code transition levels are used in the independently based method (14)to give one pair of values $\hat{C}_k^{(act),(i)}$ and $\hat{O}_k^{(i)}$. The values of $\tilde{\delta}_k^C$ and $\tilde{\delta}_k^{off}$ can be calculated approximately as three times the root mean square of the estimation errors: $\hat{C}_k^{(act),(i)} - C_k^{(act)}$ and $\hat{O}_k^{(i)} - O_k$ (similarly as in “three-sigma” rule).

V. SIMULATION RESULTS

In order to verify the capabilities of the proposed design and calibration method, a relevant model of the adaptive sub-ranging ADC with implemented procedure of the actual gains and offsets estimation was developed. The sine-wave histogram method [9] for determination of codes transition levels together with the independently based method of ADC gain and offset estimation [9]were employed for determining the gains and offsets of particular linearly distorted analog tracts of the adaptive sub-ranging ADC. As ADC performance measure, we used ENOB after k cycles of conversion calculated according to the definition given in [9]:

$$ENOB_k = \log_2\left(\frac{FSR}{\sqrt{12}NAD_k}\right), NAD_k = \sqrt{\frac{1}{M}\sum_{m=1}^{M}\left[\hat{V}_k^{(m)} - V^{(m)}\right]^2}, \quad (15)$$

where $FSR = 2D$ is the full-scale range of ADC and NAD_k is the rms value of noise and distortion [9], M is the number of input samples $V^{(m)}$. The following parameters of adaptive sub-ranging ADC were assumed: $FSR = 2$ V, $N_{SADC} = 4$, $N_{SDAC} = 12$, $\sigma_a = 10$ μV, $\alpha = 4$ .For these values of parameters the threshold number and the number of internal amplifiers is $k^* = 4$. $M = 10^5$ samples of ramp signal were converted in each experiment. To facilitate analysis, we assumed that parameters δ_k^C, $\delta_k^{off} \cdot D$, $\tilde{\delta}_k^C$, $\tilde{\delta}_k^{off} \cdot D$ are fixed in subsequent cycles and equal δ^C, $\delta^{off} \cdot D$, $\tilde{\delta}^C$, $\tilde{\delta}^{off} \cdot D$, respectively. To enable comparison of the results for different values of the maximal relative gain errors δ^C or the maximal offsets $\Delta^{off} = \delta^{off} D$, we repeatedly used the following representative sequence of values of gain errors: $\varepsilon_1 = 0.9 \cdot \delta^C$, $\varepsilon_2 = -0.8 \cdot \delta^C$, $\varepsilon_3 = 0.6 \cdot \delta^C$, $\varepsilon_4 = -0.7 \cdot \delta^C$ and offsets: $O_1 = -0.8 \cdot \Delta^{off}$, $O_2 = 0.9 \cdot \Delta^{off}$, $O_3 = -0.7 \cdot \Delta^{off}$, $O_4 = 0.6 \cdot \Delta^{off}$ .The maximal values of measurement errors $\tilde{\delta}_k^C$ and $\tilde{\delta}_k^{off}$ were estimated as described in Sect. IV, using $I = 10^4$ sine-wave histogram tests. The number of samples in every single sine-wave histogram test was also equal to 10^4.

Fig. 2 shows the trajectories of ENOB obtained in simulations for the increasing maximal gain errors δ^C changed from 0 to 5% at the fixed level of maximal offsets $\Delta^{off} = 100$ μV.

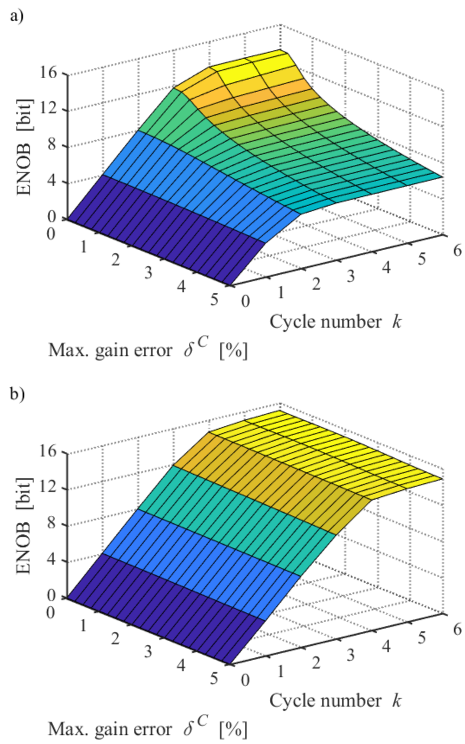

Fig. 2. ENOB of adaptive ADC without (a) and with (b) calibration, for various maximal gain errors δ^C, at fixed level of maximal offsets $\Delta^{off} = 100$ μV.

Fig. 3 shows ENOBs for the increasing maximal offsets Δ^{off} changed from 0 to 1000 μV at the fixed level of maximal gain errors $\delta^C = 0.5\%$.

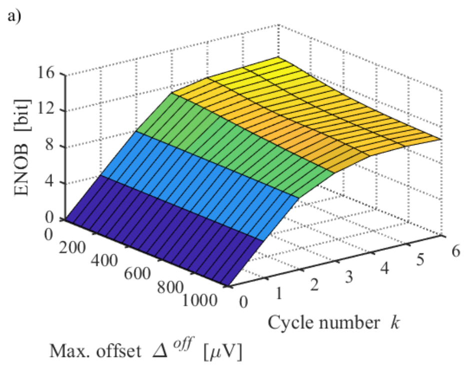

Fig. 3. ENOB of adaptive ADC without (a) and with (b) calibration, for various maximal offsets Δ^{off} *, at fixed level of gain errors* $\delta^C = 0.5$ % .

Plots in Figs. 2a and 3a correspond to the adaptive sub-ranging ADC without calibration, and in Figs. 2b and 3b to its modified and calibrated variant .One can observe that gain errors or offsets cause significant, unacceptable losses in ENOBs for the adaptive ADC without calibration (Figs. 2a and 3a).

The losses in ENOBs increase with the increase in the level of gain errors or offsets, which is caused by increasing with errors level, frequency of appearance of saturations in particular cycles of conversion. The corresponding results obtained for the adaptive ADC with calibration (Figs. 2b and 3b) show that this version is resistant to gain errors and offsets. ENOBs achieve the values close to those achieved by the ADC without gain errors and offsets. There is a gentle, almost unnoticeable, diminution in ENOBs (in the considered ranges of errors) with the increase in the level of gain errors or offsets, which is related to the necessary adequate decreasing of the gains to values $C_k^{(safe)}$ (Table 1).

VI. CONCLUSIONS

A new method for design and calibration of adaptive sub-ranging ADCs that maximally reduces the influence of both gain errors and offsets of the analog tracts used in subsequent cycles of conversion was proposed. The method employs the unique features of the adaptive ADC which allow introduction of the necessary modifications to nominal gains values and compensation signal. In the paper, there was also proposed an original approach to estimation of the actual gains and offsets in the analog tracts of the manufactured ADC which uses a modification of the IEEE 1241 Standard [9] method of ADC gain and offset estimation.

The results of simulations confirmed that application of the proposed solutions creates a possibility to significantly reduce the influence of gain errors and offsets. The latter allows reduction of the requirements on precision of the internal components of adaptive sub-ranging ADCs and, in consequence, of their manufacturing costs.

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