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Development of Quantum voltage noise source chip for Johnson noise thermometer system

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***Abstract* – Quantum voltage noise source (QVNS) based Johnson noise thermometer (JNT) system employing Josephson junctions (JJs) to generate calculable and quantum accurate pseudo-noise waveform as an artificial noise in measuring the thermodynamic temperature of a resistor. In this paper, we present the progress of design, fabrication, and characterization of the QVNS chip in NIM.**

Keywords – Quantum voltage noise source, Johnson noise thermometer, Josephson junctions, pulse driven.

I. INTRODUCTION

In the new International System of the Units (SI), the unit of thermodynamic temperature, kelvin, is defined upon the fundamental constant k_B, the Boltzmann constant. In order to ensure the link between the practical metrology standards and the temperature scale to the revised definition, national metrology institutes conducted researches to determine the value of k_B by varies of ways during the past few years.

There were various methods to link the kB to temperature [1, 2]. JNT is a method to obtain the thermodynamic temperature through the measurement of the noise of electrons' movement within conductors. NIST proposed the method of employing JJs as a QVNS [3], which can compare the calculable and quantum accurate pseudo-noise waveform as an artificial noise and the thermodynamic temperature of a resistor. After the SI redefinition, Johnson noise thermometers could be used as a quantum electrical method to measure thermodynamic temperature.

The QVNS chip in the NIM JNT system [4] was provided by NIST previously. We began to develop QVNS chip years ago in NIM [5]. We have improved the design to achieve larger operation margin. In this paper, we present the progress of design, fabrication, and the primarily characterization of the QVNS chip by using $Nb/Nb_xSi_{1-x}/Nb$ Josephson junctions.

II.CHIP FABRICATION

A. Chip Design

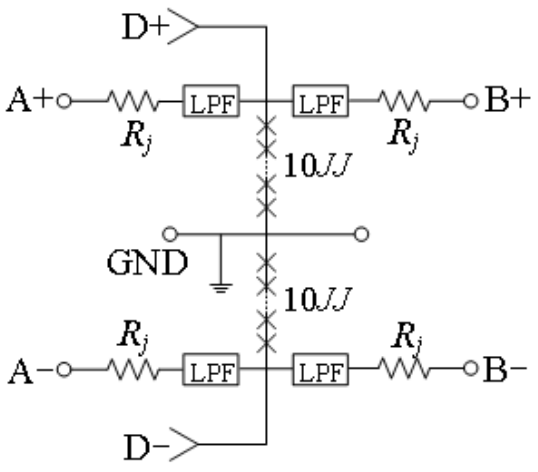


Figure 1. QVNS circuit for two-channel JNT cross-correlation measurements.

The QVNS electrical circuit was shown in Fig. 1. Like the NIST design [6], the QVNS chip consists of two identical Josephson junction arrays. Three wires are used in each channel (A and B) for the differential pair and ground. The ground provides the reference for the differential amplifiers. Two JJ arrays are used to produce

the opposite polarity waveforms, each array has 10 $Nb/Nb_xSi_{1-x}/Nb$ Josephson junctions. To improve operating margins, damped counter-wound inductive coils are used low pass filters for the high speed DCG signals.

B. Chip Fabrication

The QVNS chip fabrication process was performed on a 2-inch silicon substrate, self-shunted and non-hysteretic SNS $Nb/Nb_xSi_{1-x}/Nb$ junction technology was used. The $Nb/Nb_xSi_{1-x}/Nb$ sandwich structure is deposited on an oxidized Si wafer using the Lesker CMS-18 sputter system. We have improved the design on Nb_xSi_{1-x} barrier layer to achieve larger operation margin. The Nb_xSi_{1-x} barrier layer was co-sputtered at the Nb target power of 38 W and Si power of 250 W for 235 seconds, estimated to be 40 nm thick. The barrier parameters are designed to make the junctions have a good response on the frequency of 5 GHz. The stress mapping of the wafer after $Nb/Nb_xSi_{1-x}/Nb$ sandwich structure deposition is shown in Fig. 2. The average stress of the structure is 88 MPa. The Josephson junctions are 6 μm × 12μm in area, and distributed at 4 μm intervals along the CPW center line.

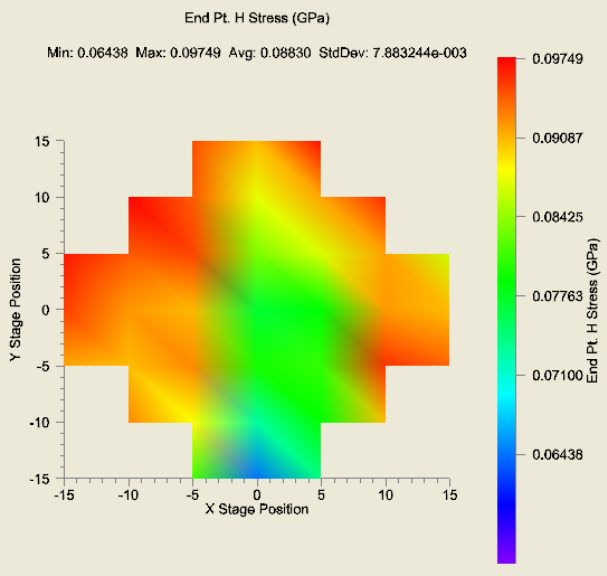


Figure 2. The stress mapping of the wafer after $Nb/Nb_xSi_{1-x}/Nb$ sandwich structure deposition.

The junctions, electrodes and SiO_2 vias were etched by ICP-RIE systems. The junction area of each junction is an important parameter. It is important to make a vertical etching profile. The junctions were etched with 10 sccm of SF_6, 18 sccm CHF_3, at 3 mTorr, 300 W of ICP power and 80 W of RIE power by Oxford PlasmalabSystem100 ICP180. The Nb electrodes were etched to a slope profile with 50 sccm of CF_4, 8 sccm O_2, at 100 mTorr, 300 W of ICP power and 100 W of RIE power by Trion Phantom ICP/RIE. In order to ease the later Nb film coverage, it is desirable to etch the SiO_2 film with sloped profiles. The SiO_2 layer inside vias should be etched away completely in order to obtain excellent connection between counter electrodes and Josephson junctions. And the recipe should have a slow Nb etch rate since Nb layer is beneath the SiO_2 layer. The vias were etched to a slope profile with 100 sccm of CHF_3, 50 sccm O_2, at 100 mTorr, 300 W of ICP power and 60 W of RIE power by Trion. The wafer is cooled by Helium at 20℃. LEP400 Etch Depth Monitor is used to monitor the etching depth during the etching.

III. MEASUREMENT RESULTS AND DISCUSSIONS

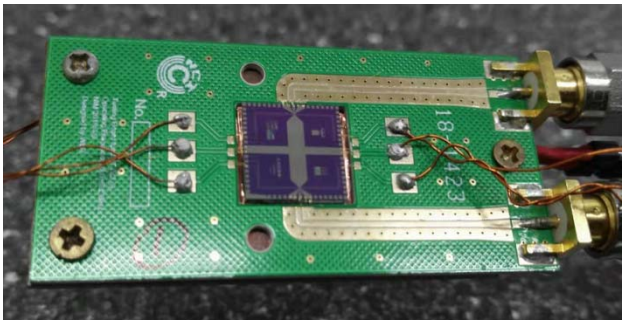
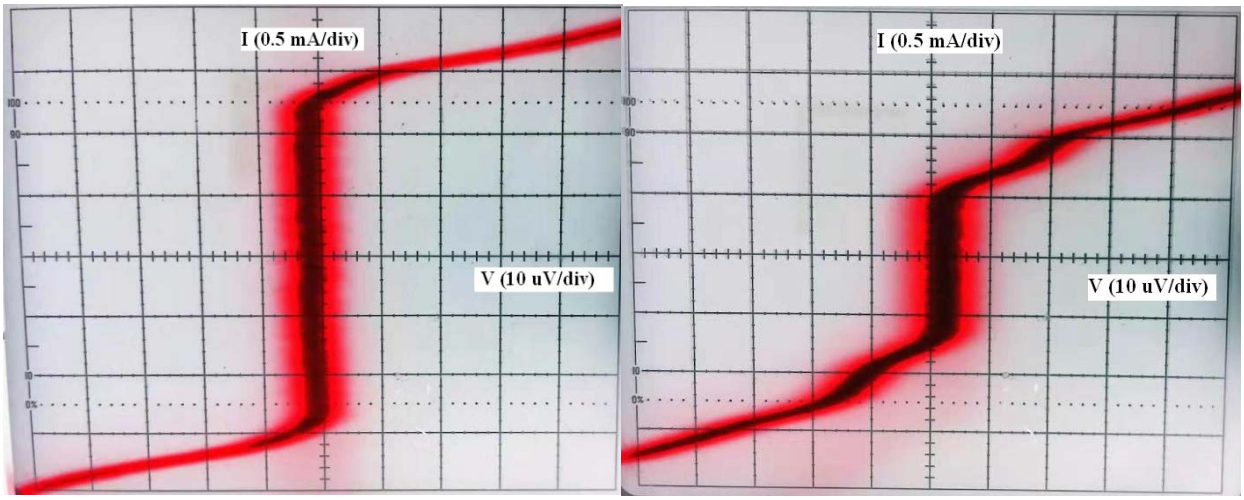


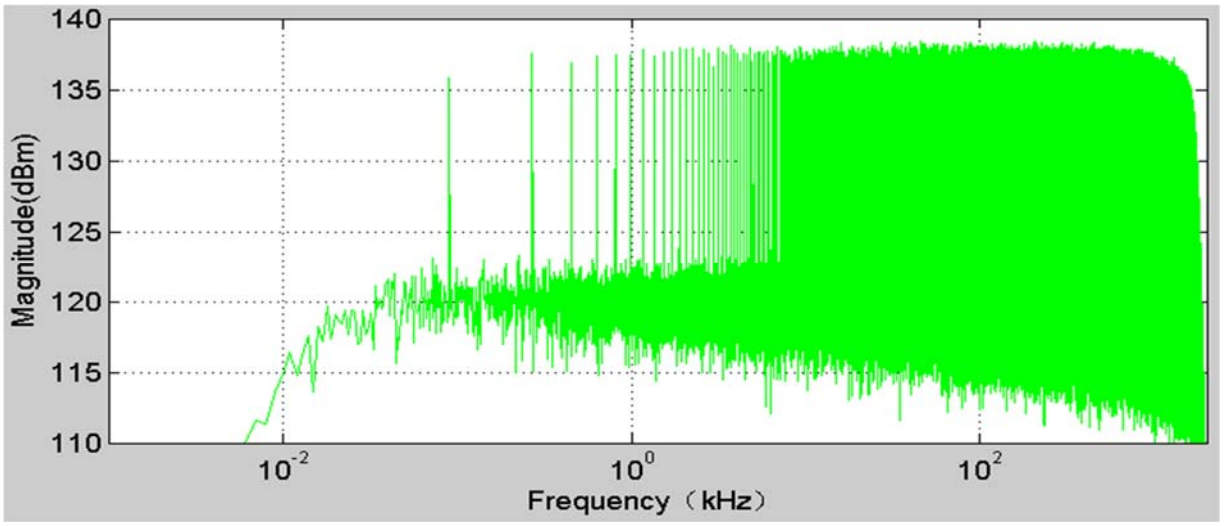
Figure 3. The test package of the quantum voltage noise source chip.

For the measurements, the chip is mounted on a PCB in a magnetically shielded probe, as shown in Fig. 3. The probe is cooled to 4.2 K in a liquid-helium Dewar. In order to briefly check the functionality of the QVNS chip by JNT electronics, we synthesize an odd-distribution multitone signal with frequency bins ranging from 90 Hz to 4MHz. The waveform is encoded in a $M = 55555520$ bit-long binary pulse pattern using 3rd-order Delta-Sigma modulation technique, the pulse pattern generator is clocked at 9.9999936 GHz with a sampling frequency of $f_s = 4.9999968$ GHz, thus the repetition frequency of the waveform is $f_s/M = 90$ Hz. The power spectrum density of the multitone signal equals to that of the thermal noise generated by a 100 Ω resistor placed at the triple point of water. We select odd-distribution multitone signals rather than even-distribution multitone signals to minimize the nonlinear distortions.

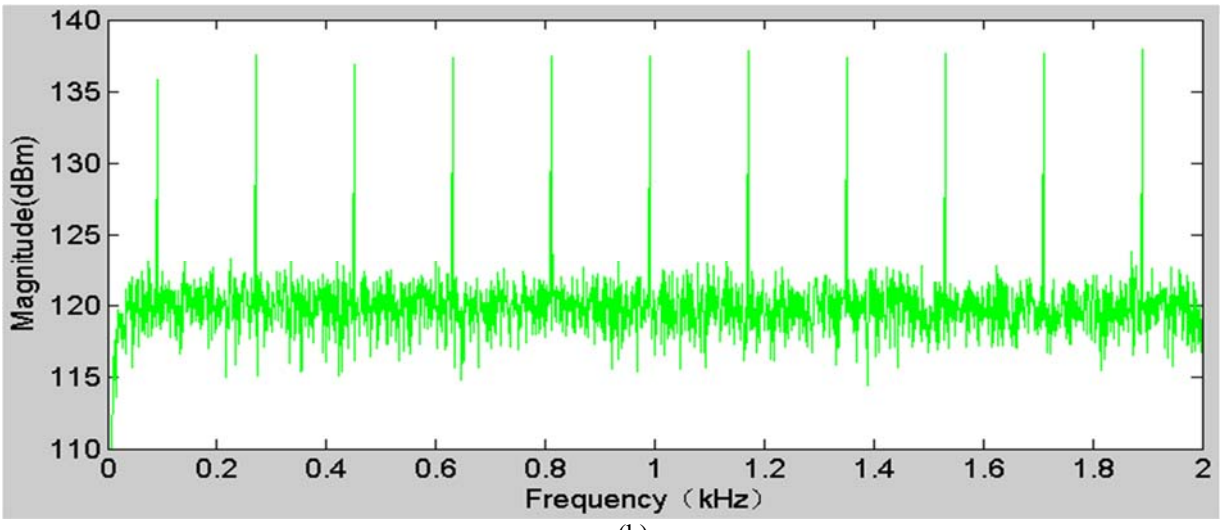


(a) (b)

Figure 4. IV curves without (a) and with (b) pulse applied on the QVNS chip, dc-component in the output voltage is expected to be zero by bipolar pulses.



(a)



(b)

Figure 5. Digitally sampled spectral measurement of multitone signal synthesized by the quantum voltage noise source chip. The peaks are the generated harmonic tones.

The IV curves of a JJ array with and without pulse bias are shown in Fig. 4. The critical currents $I_c \approx 1.2$ mA for the junctions, and the normal resistance $R_n \approx 6.1$ mΩ per junction. The characteristic frequency $f_c = K_{J-90} I_c R_n =$ 7.3 GHz, which is at the same order of the pulse frequency of 5 GHz.

Digitally sampled spectral of 20 measurements on the multitone signal generated by one of the arrays is shown

in figure 5. Commercial ADCs with a high resolution of 16 bits at 4 MHz sampling frequency are used for data acquisition. The sampled data are transmitted to a computer through optical fiber. Fast Fourier transforms (FFTs) are performed on the data in the computer. The auto-correlation (channel A and B) and cross-correlation power spectra are then calculated and averaged for analysis. As expected, no even harmonic distortion tones could be observed above the noise floor, which means the JJ array working under pulse driven mode accurately.

IV. CONCLUSION

The Nb/NbxSi1-x/Nb Josephson junction QVNS chips were fabricated in NIM. A multitone signal was generated by 10 JJs to briefly check the functionality of the QVNS chip. No harmonic distortion tones could be observed above the noise floor in digitally sampled spectral. We have improved the design on Nb_xSi_{1-x} barrier layer to achieve larger operation margin. The QVNS chip has been designed, fabricated and successfully tested, which verifies the design.

ACKNOWLEDGMENT

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REFERENCES

[1] L. Pitre, F. Sparasci, D. Truong, A. Guillou, L. Risegari, and M. E. Himbert, “Determination of the Boltzmann constant using a quasispherical acoustic resonator,” *Int. J. Thermophys.*, vol. 32, no. 9, pp. 1825–1886, Sep. 2011.

[2] B. Fellmuth, J. Fischer, C. Gaiser, O. Jusko, T. Priruenrom, W. Sabuga,and T. Zandt, “Determination of the Boltzmann constant by dielectricconstant gas thermometry,” *Metrologia*, vol. 48, no. 5, pp. 382–390, Oct. 2011.

[3] S. P. Benz, J. M. Martinis, S. W. Nam, W. L. Tew, D. R. White, “A new approach to Johnson noise thermometry using a Josephson quantized voltage source,” *Proc. of TEMPMEKO 2001*, April 2001.

[4] J. Qu, Y. Fu, J. Zhang, H. Rogalla, A. Pollarolo, and S. P. Benz, “Flat Frequency Response in the Electronic Measurement of Boltzmann’s Constant,” *IEEE Trans. Appl. Supercond.*, vol. 62, no. 63, pp. 1518–1523, Jun. 2013.

[5] Y. Zhong, L. Wang, J. Li, J. Qu, K. Zhou, Q. Zhong, W. Cao, X. Wang, Z. Zhou, K. Fu, Y. Shi, “Quantum voltage noise source chip development at NIM,” *CPEM 2018*, July 2018.

[6] S. P. Benz, P. D. Dresselhaus, and C. J. Burroughs, “Multitone waveform synthesis with a quantum voltage noise source,” *IEEE Trans. Appl. Supercond.*, vol. 21, no. 3, pp. 681–686, Jun. 2011.