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A Novel Recursive Analog to Digital Conversion Method

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***Abstract* – This paper presents a novel scheme for conversion of analog to digital signals. Applying a native conversion resolution of just one bit with only one comparator the converter is able to increase the resolution as it can be the case with dual slope or $\Delta\Sigma$ converters. The new concept is based on a recursive operation. Therefore the converter is named rADC - recursive ADC. By processing ten recursive cycles a 10 Bit 1 MSa/s test result has been achieved by simulation of a 180nm CMOS test circuit. The rADC components of the CMOS test circuit are a comparator, a S/H circuit, some gates, transmission gates and two resistors. By the means of a digital control sequence the upper and lower converter reference voltages are redefined in each cycle. As a result the number of cycles or iterations, respectively, determine the resolution of the recursive ADC.**

Keywords: recursive analog to digital converter rADC, ADC conversion rate, ADC resolution

I. INTRODUCTION

Various types of data converters exist for different types of application. Flash A/D converters provide a high conversion rate but they require a large number of components for example 255 comparators and resistors and a lager amount of digital gates for an 8 bit converter. The circuit complexity will increase exponentially with n number of bits $(2^n - 1)$. They are unfavorable in terms of the chip area, resolution and the costs of the integrated circuit. Pipeline A/D converters provide a better balance but they still need a larger number of components.

Successive-approximation A/D converters operate with a comparator and a D/A converter requiring a linearly increasing number of components with respect to the required resolution of n bits, without regarding special converter types [1]

Whereas $\Delta\Sigma$ modulators and integrating A/D converters have much less components at the expense of the conversion speed. The basic versions of such converters require an amplifier for signal integration and a single comparator in order to generate the digital output signal.

The new rADC concept needs slightly more components than a dual slope A/D converter or the first order $\Delta\Sigma$ modulator. In terms of circuit complexity the rADC is most likely comparable with these architectures. With respect to the flash A/D converter the resolution can be chosen higher but the conversion rate is lower. Compared with the successive-approximation SAR A/D converter the conversion speed of a rADC is similar, but the rADC requires no linear increasing number of components with respect to the converter resolution. This is the major difference or advantage, respectively. Furthermore the resolution and the conversion rate is digitally and flexibly adjustable just by defining the number of cycles and the signal period.

Table 1. ADC comparison

ADC type	typ. resolution	typ. sampl. rate	physical resolution aspect
Dual slope	$<$ 16bit	100kSa/s	low native resolution
$\Delta\Sigma$	$<$24bit 5	50kSa/s	low native resolution
rADC	$<$10bit	1MSa/s	low native resolution
SAR	$<$12bit	1MSa/s	linear DAC area increase
Flash	$<$8bit	1GSa/s	exponential area increase
Pipelined	8 - 15 bit	100kSa/s	linear area increase

Table 1 summarizes typical on the market available A/D converter concepts - without regarding special or at the edge types and includes the new rADC concept. The converter architecture of the rADC is different compared with all others.

II. RECURSIVE ADC CONCEPT

In equation 1 the voltage resolution v_{step} is determined by the number of bits (#bit) and by the reference voltages.

$$v_{step} = \frac{reference\_range}{2^{\#bit}} \tag{1}$$

If the reference range is taken as the main parameter and systematically reduced, the smallest step voltage v_{step} is linearly resized, so that smaller reference voltages of ADCs can result in a higher resolution. This means that even coarse A/D converters could have a higher resolution if the reference range is systematically reduced during the conversion process.

Based on this idea, the following described method changes the reference voltage range during the conversion

process, resulting in a higher resolution than the native resolution of the converter provides. This can be for example 3 native bits, as delineated in this section. Whereas the CMOS test circuit in the next chapter operates with a native resolution of 1 bit. Other native resolutions are possible.

Figure 1 shows an example of the refinement of an A/D converter with a 3 bit native resolution. The 1^{st} conversion or iteration in the figure leads to a digital output of "011", while the input voltage v_{in} is in the range between "011" and "100".

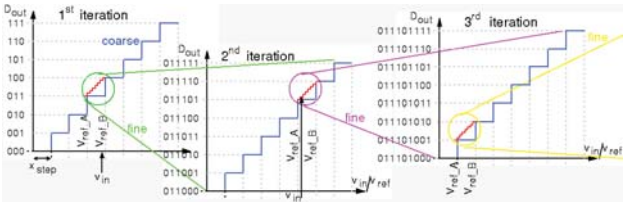

Fig. 1. Refinement of coarse A/D converters

For these two binary values the corresponding analog voltages V_{ref_A} and V_{ref_B} can be generated with a DAC. If these voltages are stored in a sample and hold circuit S/H and used as the new references for the native ADC the resolution is increased according to equation 1. This can be done recursively several times, resulting in an increase of resolution depending on the number of recursions. Figure 1 shows a second and third iteration thus enhancing the digital output D_{out} from 3 bit to 6 bit and for the third iteration to 9 bit.

This kind of reference voltage modification of native A/D converters is depicted in the scheme of figure 2.

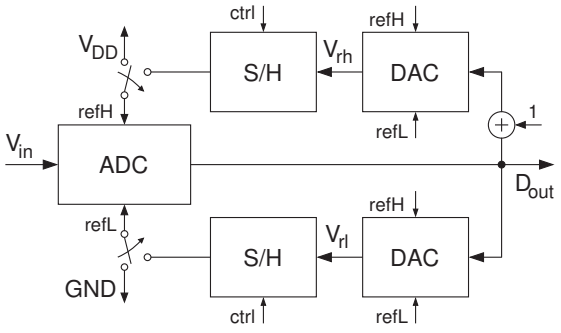

Fig. 2. Recursive A/D converter concept [2]

An analog input signal v_{in} is applied to the input of an A/D converter -ADC- with a coarse or native resolution, respectively. For the 1^{st} conversion the reference voltages of the A/D converter are connected to the power supply voltages (or any other initial large voltage range) for a large dynamic range. The A/D converter generates afterwards a digital output D_{out}. The number of bits $\#bit$ of signal D_{out} depends on the native resolution of the converter. Basically, the number of bits or components, respectively, should be kept small in order to to achieve the main benefit of the new concept like a small circuit complexity and chip area (e.g. components for a 3 bit flash converter in order to realize figure 1). A simple comparator generating only one output bit would be the smallest native A/D converter solution. The resolution of the coarse converter is always a trade-off between conversion speed and circuit complexity.

In order to generate new reference voltages for the next iteration, the digital output D_{out} and a second calculated value $D_{out}+1$ are converted with DACs to analog voltages V_{rh} and V_{rl}. The reference voltage of these DACs V_{ref_A} and V_{ref_B} must be identically with the ADC reference voltage.

The reference voltages for the next iteration V_{rh} and V_{rl} are stored in a sample and hold S/H circuit before providing them at their outputs. A control circuit generates clock signals clk for the S/H and an $init$ signal (determines the conversion period) for the two-way switch.

III. TEST CIRCUIT

A. Circuit Architecture

As already mentioned the architecture in fig. 2 allows different types and resolutions of ADCs and DACs. For a very first approach the test circuit with the smallest native resolution option has been considered.

The test circuit implementation with a native 1-bit (flash) ADC realized be a single comparator entails a minimum number of components, chip area and power consumption. The circuit is shown in figure 3. The unipolar power supply for the component parts is 3 V referring to GND. The initial lower and upper converter reference voltages V_{DRmin} and V_{DRmax} are connected to $1V$ and $2V$, respectively. An init signal $init_1$ starts the conversion. With the first clock cycle of clk_1 and clk_2 the maximum conversion range is applied (setting $V_{DR_{max}} = refH$ and $V_{DR_{min}} = refL$) across the resistors. The two resistors halves the voltage and generate the signal $refM$. Depending of the input voltage v_{in} and the signal $refM$ the comparator output results in a "0" or "1".

The CMOS comparator and the two resistors R in figure 3 operate as a 1-bit flash ADC. The analog switches (CMOS transmission gates) and the digital switch control signal b_s perform the 1-bit DAC function.

Depending on the output state of the comparator signal bs, which can be either "0" or "1", the opening or closing switch forward the voltages for the upper reference voltage either refH or refM and for the lower reference refL or refM voltage. Each cycle defines therefore for the following cycle the next upper and lower reference voltage. One of it changes to refM the other reference voltage is

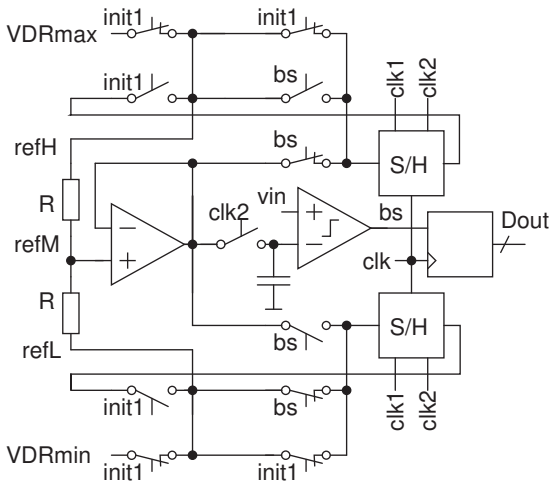

Fig. 3. rADC test circuit

kept unchanged. So each cycle halves the voltage difference between upper and lower reference voltage. As a result the reference voltage refM approaches the value of the input voltage v_{in} successively. If the clocks clk1 and clk2 appear n times within one period of an init1 signal the voltage resolution v_{LSB} of the converter is

$$v_{LSB} = \frac{V_{DRmax} - V_{DRmin}}{2^n} \tag{2}$$

For the 10 bit A/D converter of this example, the number of cycles are n=10. The smallest voltage step is therefore $v_{LSB} = (2V - 1V)/2^{10} \approx 1mV$.

The closing and opening switches must be controlled by non-overlapping control signals in order to prevent that two parallel analog switches (OR function) conduct at the same time, which would entail erroneous results.

At the output a SiPo register (serial input, parallel output) generates the 10 bit parallel output information.

B. Comparator

A fast comparator with a small overdrive voltage is required for this design. For a unipolar power supply voltage of $VDD = 3V$ the typical comparator parameters have been determined by simulation. The reference voltage for the comparator values in table 2 is $VDD/2 = 1.5V$.

Table 2. Comparator parameters

Parameter		typical value
Input offset	v_{io}	< 1 mV
Propagation delay time	t_{pd+}	1.6 ns
	t_{pd-}	1.7 ns
Large signal gain	A_v	1000 V / mV

The propagation delay times in table 2 is analyzed for an overdrive voltage of $v_{ov} = 50mV$. An overdrive voltage of $v_{ov} = 1mV$ increases the propagation delay time to $t_{pd} \approx 10ns$.

C. Sample and Hold S/H

The output of the DAC in figure 3 is connected to a sample and hold circuit. This circuit part is shown in figure 4.

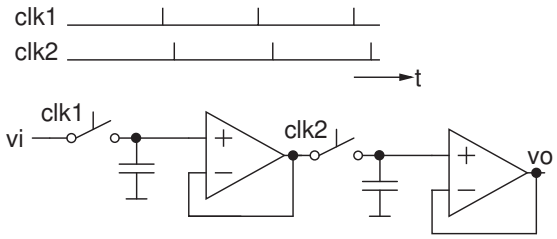

Fig. 4. Sample and Hold circuit

The two stage switch and capacitor elements are decoupled with voltage followers. According the S/H timing the clocks pulse width Pw=30ns and the clock period Per=100ns are adjusted for both clocks $clk1$ and $clk2$. These control signals in figure 4 must not overlap in order to prevent that the input signal is being processed directly to the output. Therefore the clock signal $clk2$ is 10 ns delayed regarding clock signal $clk1$. As an example for a 10 bit converter 10 periods have to be applied, achieving a total conversion time of $1\mu s$ or a conversion frequency of $1MHz$, respectively.

D. OPAMP

The full custom rail-to-rail input/output CMOS operational amplifier requires a large bandwidth for high speed converters. A design with a folded cascode gain stage and a class A/B output amplifier has achieved the following results, as listed in table 3:

Table 3. OPAMP parameters

Parameter		typical value
Systematic input offset	v_{io}	$< 750\mu V$
Large signal gain	A_v	$150V/mV$
Slew rate	$SR+$	$33V/\mu s$
	$SR-$	$15V/\mu s$
Gain bandwidth product	GBP	$115MHz$

This OPAMP is only used as a voltage follower in the S/H circuits. A further voltage follower decouples the two resistors and the switch / capacitor element in figure 3.

E. Analog Switches

The accuracy of the converter in figure 3 is also influenced by the analog switches. The on-resistance should be small in order to realize low time constants in conjunction with the S/H load capacitor, which is important with respect to the converter speed. On the one hand the transistor width / length ratio should be large for low on-resistances on the other hand would large ratios entail a significant charge injection. But charge injection of the switch is critical and impacts directly the accuracy. Therefore the transistors size as well as the switch architecture are important in order to reduce the charge injection effect.

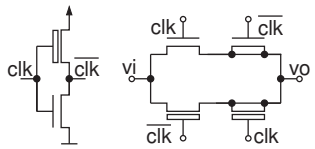

Fig. 5. Analog Switch

Figure 5 shows a complementary switch design.The incorporation of a pmos and a nmos transistor lowers the effect of charge injection significantly in the moment of switching because the amount of electrons and holes are approximately equal for equal transistor sizes. Additional dummy switches conduce to reduce the clock feedthrough effect. As an estimation the transistor width of the dummy switches is chosen with the half size in comparison to the conducting switch transistors. The dummy transistors are switched with inverted clock signals, resulting in an overall very low charge injection effect.

F. Non-Overlapping Control Signal Generator

Figure 3 includes opening and closing switches for the signals initial signal $init1$ and the streaming signal of the bit bs. The $inti1$ signal is used to start the conversion process, whereas the bs signal contains the bits which are part of the conversion result. They are store in a register and the are used to control the simulation process.

In case of applying the $intit$ and the bs signal simultaneously to the opening and the closing switch an error occurs at the output. Due to the fact that both switches would conduct for a very short period of time, the signals at the output of this OR configured switches would be warped.

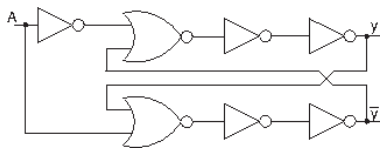

Fig. 6. Non-overlapping signal generation

Therefore it is a requirement that only one of the opening and closing switch configuration is conducting in one point of time. A mutual influence of the input signals can be prevented if the opening an the closing switch are controlled by non-overlapping signals.

Basically the circuit in figure 6 is composed of a latch. A short signal delay occurs at the outputs. This circuit is used for the $init1$, bs and $clk2$ signals.

IV. RESULTS AND DISCUSSION

A. Simulation results

Based on ideal hardware description models for the test circuit described previously, the simulation results for a DC input voltage of $v_{in} = 1.814V$ and 10 iterations are considered in figure 7.

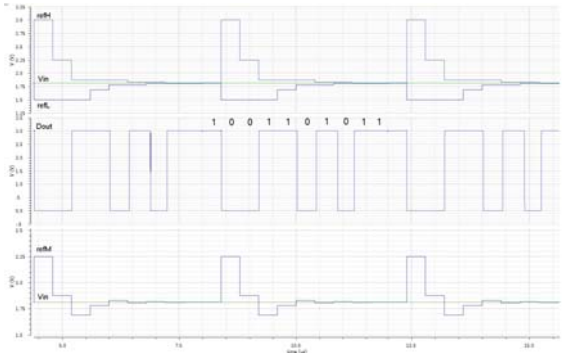

Fig. 7. rADC model based simulation result

The upper stripe plots both reference voltages ($refH$ and $refL$). They converge to the input voltage v_{in} and half every cycle the voltage difference. The serial output signal D_{out} in the middle stripe contains the digital output information. If $refH$ changes $D_{out} = 0$ and if $refL$ converges $D_{out} = 1$. The serial digital information can be obtained from the graph as 1001101011_b. The lower strip shows the average voltage $refM$ of both reference voltages with respect to the input voltage v_{in}. As long as the errors of the analog circuit are small enough, the number of cycles or the resolution, respectively, can be increased. In order to verify the result: $1001101011_b = 619_{dec}$ and $1.814V/3V \cdot 1024 = 619.1787$.

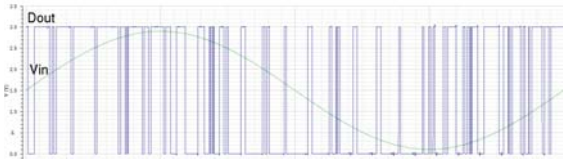

Fig. 8. Digital output signal rADC

Figure 8 shows the serial output signal for sine wave

input signal.

Following figure 9 is based on the CMOS circuit described in the previous chapter and shows the simulation result for a sine wave signal with a period of 100μs. This signal is one hundred times converted within this period. The conversion rate is 1MSa/s. Both reference voltages ($refH$ and $refL$) envelope the sine wave signal.

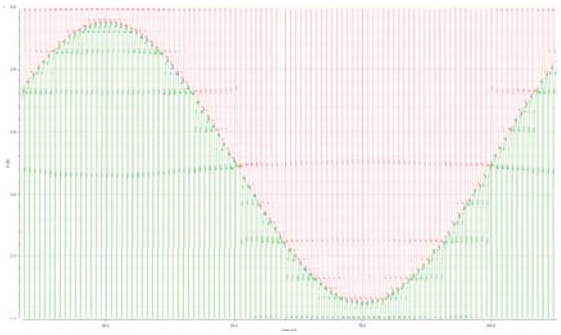

Fig. 9. Reference voltages envelope of a sine wave signal

A more detailed view is shown in figure 10. A sine wave signal with a period of 20 μs is converted 20 times while the input signal changes continuously.

As a result the new A/D converter concept operates with 1 MSa/s and a resolution of 10 bit with the CMOS components and the clock timing described before. The bandwidth and the offset of the OPAMP and the comparator limit the conversion speed.

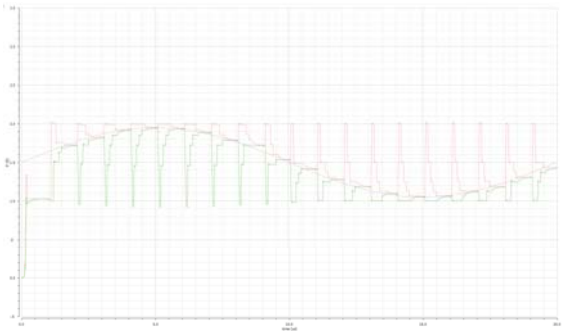

Fig. 10. Conversion of a sine wave signal

B. Discussion

The first approach of a recursive A/D converter accomplished conversion speed and resolution in the mid-range of available A/D converters. The main idea of this concept is to reduce chip area for A/D converters with higher resolutions. Before chip layout completion an estimation of the chip area could be done based on the components required. For prove on concept 11 analog switches, two resistors, one comparator and five OPAMPs are used for this test circuit. The power consumption of the circuit is $\approx$ 600 μW. Architectural improvements could reduce the amount of components, the required chip area and power consumption. For instance the resistors could be replaced by capacitors. Whereas higher resolutions and higher conversion rates entail improvements for the analog components.

Compared with methods like flash A/D converters or successive approximation SAR A/D converters the new A/D type has a native resolution of only 1 bit. Compared with an integrating A/D converter or a $\Delta\Sigma$ modulator the conversion speed is larger.

So the new concept is suitable for mediate conversion rates but allows also small integrated circuits. The resolution ideally depends on the number of recursions. Low OPAMP and comparator offsets as well as a small clock feedthrough are the main concerns with respect to the converter resolution.

V. CONCLUSION

For the new proposed recursive A/D converter concept a first test circuit has been presented. The method requires internally sample and hold circuits and in addition an A/D and a D/A converter. There native resolution can be with 1 bit as small as possible. Larger native resolutions allow larger conversion speeds. Analyzed has been the concept itself and the expected performance category. A deeper analysis extracting parameters like INL, DNL and ENOB is future work.

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