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CONSIDERATIONS ON THE INFLUENCE OF THE GROUNDING SET-UP CONFIGURATION ON ESD SUSCEPTIBILITY

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Abstract – Some unexpected failures during ESD tests upon a sensitive fluxgate magnetometer leaded to measurements of the ground potential of the three PCBs, composing our DUT. A significant improvement of the minimum discharge voltage causing errors was obtained only after reducing the impedance of the shielded internal ground lead and equalizing the lengths of the grounding cables connecting the three "shelves" to the "ESD common point ground". RF measurements techniques and results, graphics, models and equivalent circuits are presented.

Keywords: ground potential, ESD immunity.

1. BACKGROUND OF THE PROBLEM

The measures having to be implemented for defending our equipment from ESD are focussed on the well-stated four main directions:
-to reduce static accumulation just from the beginning;
-to insulate in order to avoid sudden discharge;
-to screen the sensitive circuits against disturbing fields that follow the discharge (blocking capacitive coupling);
-to offer a substitute low impedance path (bypassing the sensitive parts) for the discharge current.

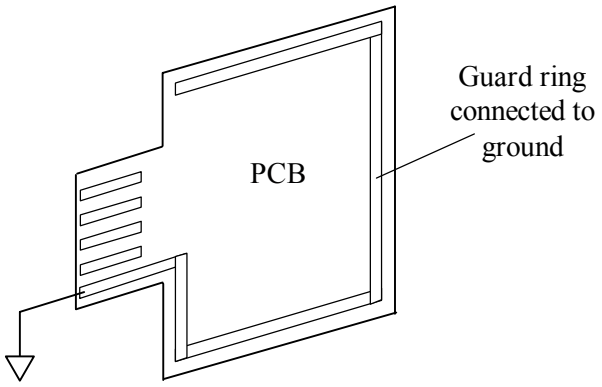

Fig.1 Electrostatic guard ring for ESD protection for sensitive PCBs

The most usual key for obeying this last desideratum is to safely and firmly ground all the exposed metallic components and the signal local grounds of the PCBs, regarded as distinctive "shelves" in the cabinet. Putting this into practice also means: separate I/O and digital grounds, reduced overall inductance of the ground system, compact ground loop area. Another implemented precaution was a copper (printed) guard ring at the whole periphery of each PCB, excepting, obviously, the connector to main board (not connected to circuits on board, but tied to the pull out lever and the frame ground), fig.1.

2. STARTING POINT

During the pre-compliance tests of a sensitive fluxgate magnetometer, we have chosen the quick testing method [1] for ESD immunity investigation. Our ESD test-gun has a fast-fire alternative for air discharge, with the output relay disabled and the internal high-voltage generator coupled directly to the probe tip. The discharge happens once the "head" charges sufficiently to break down the air gap to the equipment under test. Our primary option for this timesaving method (but not carefully controlled), justified by our expectations that ESD tests would be easily passed, finalised with an irreversible damage for the entrance analogue circuitry (many other not so harmful "digital" errors previously occurred).

3. IMPROVING OUR ESD GROUNDING SYSTEM

Effective ESD ground is of critical importance. Initially, we grounded all components of the work area (work and walking surface, wrist strap, equipment and auxiliary ground) to the same electrical ground point called the " ESD common point ground", properly identified by the settled symbol, fig.2.

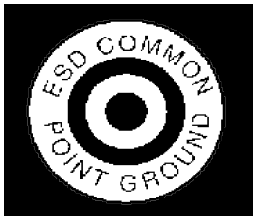

Fig.2 The symbol for "ESD common point ground"

We engaged our efforts (shown in fig.3) towards compulsory improvements, by implementing the ESD Association Standard ANSI EOS/ESD 6.1-Grounding recommendations [2] and IEC Standard 61000-4-2, [3].

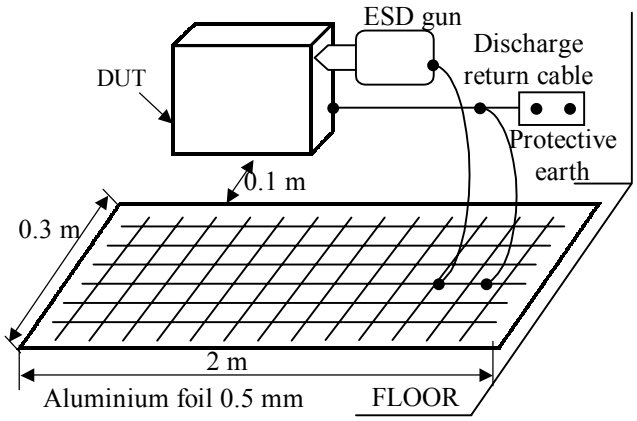

Fig.3 Recommendations IEC standards (here implemented) for a reliable test

The following step was to connect this "ESD common point ground" to the third wire (green) electrical ground connection (namely, to the metallic chassis), preferred option because all electrical equipment at the workstation is already connected to this ground. So, the same electrical potential is referred to all components of our workstation. The single-point ground connection prevents the potential differences to bleed off a charge-accumulation. Interior electronics was separated from ungrounded parts of the enclosure by 1 cm and from grounded parts by 1 mm to put a stop to secondary arc discharges to the circuitry. (1cm was calculated considering that the breakdown electric field strength in normal humidity air is of about 30 kV/cm, and an ungrounded part can reach the potential of the charged body, some 25 kV), [4].

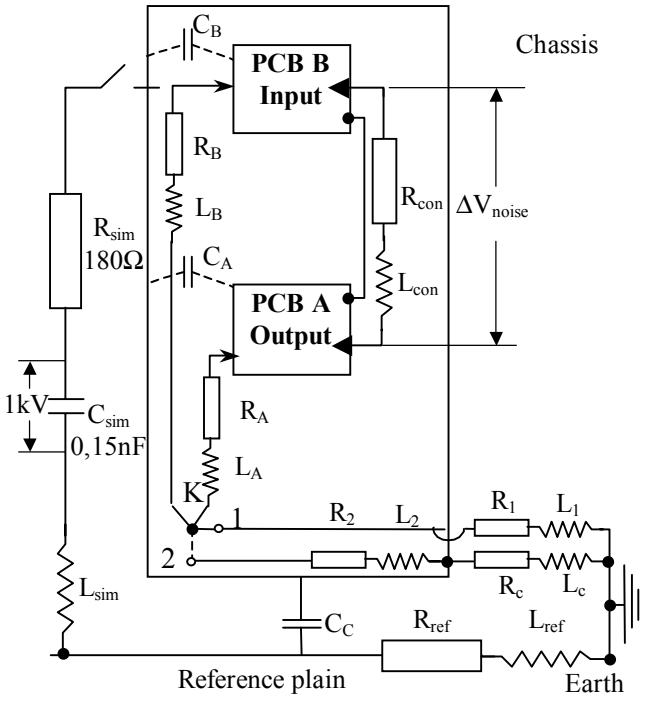

Fig.4 Simplified diagram for connecting the signal reference of two PCBs

Newly done measurements evaluated the minimum discharge voltage causing errors by a parity check. A 100Ω resistance was inserted into the signal line for reducing the noise margin to about 30% and facilitating the immunity measurements with discharge voltages less than 10kV, [5]. Another attempt was focussed toward reducing the cable ground impedance (a twisted pair having the shield made up of two aluminium foil sheets each 30μm thick and, respectively, a copper wire-lattice, ϕ=0,8). At 20 MHz, their measured impedances (reasonable conformity with computed values from Schelkunoff's equations) were 25Ω and 17Ω, meaning an increasing in the minimum discharge voltage causing errors from 2,5kV to 3,5kV.

4. THE INFLUENCE OF INTERNAL GROUND CONDUCTOR LENGTHS ON ESD IMMUNITY

The previously mentioned "minimum discharge value" was even under usual expectations. Using a troubleshooting storage scope, with 500MHz bandwidth, 2 GSa/s sample rate, provided with powerful digital features, we detected, immediately after the discharge, considerable ground between two PCBs (technologically connected at a mutual distance of 2,5 meters), with the peak-to-peak amplitude of 25 Volts, decreasing to zero in more than 1μs. The simplified diagram for connecting the signal reference of two PCBs is presented in fig.4. To be blame for the previously mentioned potential unbalanced is the abrupt release of the electrostatic energy from the ESD simulator to the chassis, lifting up the potential in the PCB ground planes (the applied voltage between the discharge point and the ground plane is divided between the parasitic capacitors and ground cable lump resistors and inductors, affecting the ground equilibrium). This ground potential un-equilibrium between PCBs means alteration between receiving and sending signal reference, consequently a contribution to the minimum discharge value causing errors. We developed and tested a circuit simulation, gathering both the ESD gun and the grouped together constants of the ground elements (interface ground connection, internal and external ground wires and planes).

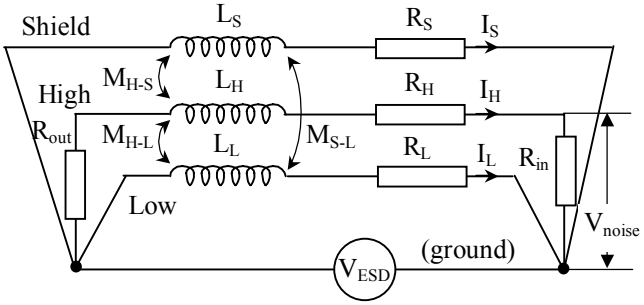

Fig.5 Model for computing the effective noise voltage induced by ground potential difference (due to ESD)

From this model, the influence of the cable length connecting the PCBs ground derives obviously. For evaluating the fraction of this ground potential dissimilarity acting like an explicit noise voltage, we tested an equivalent model of the cable linking the two PCBs, based on the output impedance of the sending circuit, the input impedance of the collecting one, the galvanic resistance, the

own impedance and the mutual impedance of the two twisted wires and the overall shield. The percentage of the effective noise voltage was about 10% at 10 kHz, going below 1% in the MHz field (reasonable correspondence between measured and estimated values).

There were plotted many comparative graphics (measured values versus predicted ones through calculation) representing, :

- The influence of the ratio of the internal ground wire lengths upon noise voltage due to the PCB's ground potential differences, fig. 6;

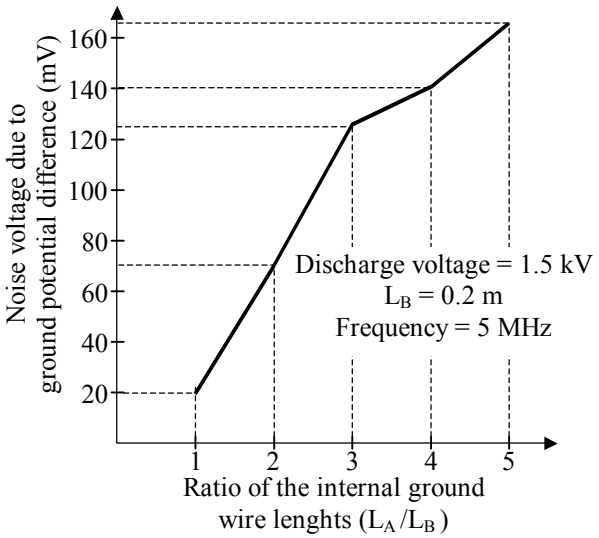

Fig.6 Influence of the ratio of the ground wire lenghts on the common mode noise voltage (between the PCBs)

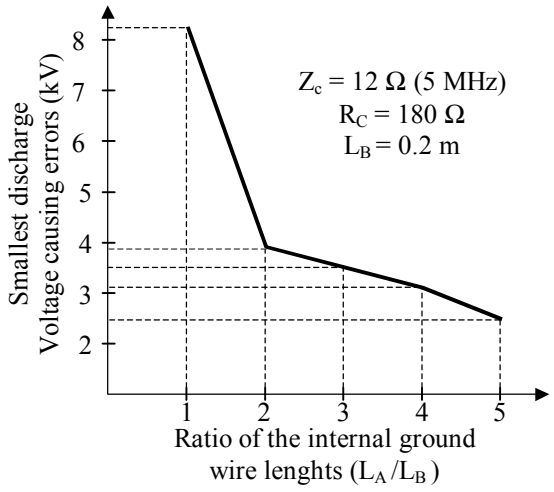

Fig.7 Influence on immunity of the ratio of the ground wire lenghts

- The influence of the internal ground wire impedance upon the PCB's ground potential differences;
- Relationship between ground potential variations in the DUT and the real noise voltage sensed at the entrance of the most sensitive PCB;
- Influences upon the causing errors smallest discharge voltage (immunity) of the ratio of the grounding wires length (characteristic impedance at 5 MHz as parameter), fig.7;
- Influences upon the causing error smallest discharge voltage of the impedance grounding wires (the ratio of lengths of the grounding wires being the parameter);

5. CONCLUSIONS

The mostly common methods for increasing the discharge voltage causing errors to DUT were implemented and the results were below expectations (about 3,5 kV). A significant improvement was obtained (8 kV) by using cables of low impedance and of the same length, for connecting the two most sensitive PCBs to the established "ESD common point ground". Connecting the signal reference (ground) of the three PCBs directly to the chassis (single point option) is not recommended from the point of view of the possibility of coupling to the "signal" of other parasitic currents (different sources) circulating through the chassis. But this inconvenient is eclipsed by the advantages due to the existence of an "ESD common point ground". In all the phases of our work, we followed the methodology fixed and developed in [6].

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REFERENCES

[1] T. Williams, K. Armstrong, "EMC For Systems and Installations", *Newnes*, Oxford, UK, pp. 258-260, 2000.
[2] ESD S6.1-1999, "Grounding -- Recommended Practice", ESD Association, Rome, NY 13440.
[3] IEC 61000-4-2, "EMC-Part4-Testing and measurement techniques- Electrostatic discharge immunity test", 1995.
[4] ESD TR 20.20, "ESD Handbook", ESD Association, Rome, NY 13440.
[5] T.Mori, O. Ibaragi, T. Kon, K. Shinozaki "Relationship of equipment grounding system configurations to ESD immunity", *IEEE International Symposium on EMC*, pp. 354-359, 1987.
[6] ANSI ESD S20.20-1999, "Standard for the Development of an ESD Control Program", ESD Association, Rome, NY 13440.

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