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MINIMISING ERRORS DUE TO NON-SIMULTANEOUS SAMPLING OF VOLTAGE AND CURRENT IN DIGITAL POWER MEASUREMENT SYSTEMS

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Abstract - A common solution to measure electrical power is through the use of systems that digitise voltage and current signals. However, several errors can affect the accuracy of such systems, namely transducer errors, sampling errors [1] and analogue-to-digital conversion errors. Sampling errors can be very important especially when low-cost solutions for digitalisation are considered. In this case, besides truncation errors caused by spectral leakage, non-simultaneous sampling of voltage and current signals, due to the absence of sample-and-hold-circuits, can also introduce large amplitude errors. In the present paper, an easy solution to minimise the last type of errors is proposed and some simulation and experiment results are presented to validate that solution.

Keywords: power measurement, signal sampling, measurement errors.

1. INTRODUCTION

Several microprocessor-based systems are nowadays used for power measurements. The programmable interface controller (PIC) [2] is an attractive solution due to its low cost and integrated analogue-to-digital conversion capabilities. For very low-speed applications, pulse-width modulated conversion schemes can even be considered to provide analogue-to-digital conversion [3][4]. However, if external sample-and-hold (S&H) and timing circuits are not used, measurement system's accuracy can be substantially affected by timing errors. A solution to minimise truncation errors, caused by frequency variation of the input signals, was already presented by the authors [5]. The advantage of synchronous sampling is especially significant when the signal frequency exhibits time fluctuations and can easily be obtained by using a phase-locked loop (PLL) circuit.
In this paper the effect of non-simultaneous sampling of voltage and current signals is analysed and a simple solution to minimise the resulting errors is proposed. Simulation programs to study the influence of sampling rate and phase difference in the presence of sampling errors are also presented.

2. SYSTEM DESCRIPTION

In order to minimise errors caused by input signal frequency variation, a PLL timing circuit can be used to assure an integer number of sampling periods in each measurement cycle. The solution of the PLL timing circuit assures also that the relative sampling factor (N/M) can automatically be adjusted and gives the following relation between input signal frequency (f) and sampling rate (f_S):

$$f_S = \frac{N}{M} f \qquad (1)$$

If the measurement cycle includes N samples of voltages and current signals, it is always assured that truncation errors are cancelled, even if signal's frequency is higher than the sampling rate. A proper choice of M and N coefficients can optimise measurement system's accuracy for a large range of input signal frequencies. The measurement cycle must be always an integer multiple of MT, where T represents the input signal period. Auto-averaging measurement capabilities can be obtained by choosing an integer value greater than unity at the expenses of measurement speed (number of readings per second).
To minimise sampling errors caused by non-simultaneous sampling of voltage and current signals, an alternated capture mode is considered, whose time sampling sequence is given by:

$\ldots, u_{k-1}, i_{k-1}, i_k, u_k, u_{k+1}, i_{k+1}, \ldots$ (alternate sequence)

instead of:

$\ldots, u_{k-1}, i_{k-1}, u_k, i_k, u_{k+1}, i_{k+1}, \ldots$ (direct sequence)

The alternate sampling sequence can be easily obtained by using an external 2-input multiplexer whose select line is synchronised with sampling frequency (f_S) but with a frequency two times lower. Fig. 1 represents the block diagram of such a power measurement system.

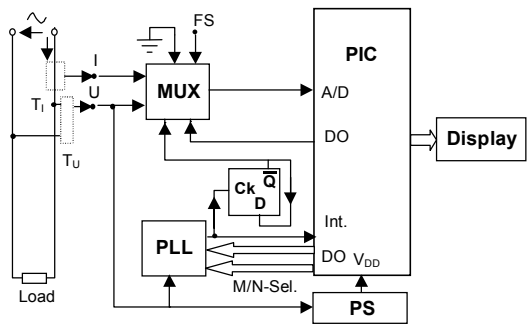

Fig. 1. Measurement system block diagram: PIC- programmable interface controller; MUX- multiplexer; PLL- phase-locked loop; Int- interrupt; A/D- analogue-to-digital input; DO- digital output; M/N Sel.- sampling rate selection to counters M and N; PS- power supply circuitry; T_U- voltage transducer; T_I-current transducer; FS- full-scale reference voltage.

Two reference signals, with well-known amplitudes, can also be used to cancel offset and gain measurement errors. The reference amplitudes are typically equal to ground and full-scale (FS) voltage amplitudes.

2.1. Loss of accuracy caused by sampling errors

Assuming that voltage and current signals are sinusoidal, for a fixed sampling error (Δt) between voltages and current samples, sampled amplitudes of voltage and current signals are given by:

$$\begin{aligned} u[n] &= U\text{sen}\left(2\pi\frac{f}{f_S}n+\varphi\right) \\ i[n] &= I\text{sen}\left(2\pi\frac{f}{f_S}\left(n+\frac{\Delta t}{T_S}\right)\right) \end{aligned} \tag{2}$$

where U represents the voltage amplitude, I the current amplitude, φ the phase difference between voltage and current signals, f the input signal frequency, $f_S = 1/T_S$ the sampling frequency, n the sample order and Δt the timing error associated with non-simultaneous sampling.

For a measurement cycle with N points, the active power is given by:

$$P=\frac{1}{N}\sum_{n=0}^{N-1}U\text{sen}\left(2\pi\frac{f}{f_S}n+\varphi\right)I\text{sen}\left(2\pi\frac{f}{f_S}\left(n+\frac{\Delta t}{T_S}\right)\right) \tag{3}$$

Using the trigonometric equality for the product of two sine functions and taking into consideration that $f_S.T_S=1$, it is possible to obtain:

$$\begin{aligned} P=&\frac{1}{N}\sum_{n=0}^{N-1}\frac{UI}{2}\cos(\varphi-2\pi f\Delta t)- \\ &-\frac{1}{N}\sum_{n=0}^{N-1}\frac{UI}{2}\cos\left(4\pi\frac{f}{f_S}n+\varphi+2\pi f\Delta t\right) \end{aligned} \tag{4}$$

Being the average value of a sinusoidal function null, the second summation term of the last expression is zero and (4) is equivalent to the following relation:

$$P = U_{ef}\,I_{ef}\cos(\varphi-2\pi f\Delta t) \tag{5}$$

where U_{ef} and I_{ef} represent the root mean square value of voltage and currents signals, respectively.

The relative error caused by non-simultaneous sampling, η_{PS}, for a direct sequence acquisition, is than given by:

$$\eta_{PS} = 100\left(\frac{\cos(\varphi-\Delta\varphi)}{\cos(\varphi)}-1\right)\% \tag{6}$$

Relative errors are proportional to timing errors ($\Delta\varphi=2\pi f\Delta t$) and for a fixed value of timing error (Δt) the measurement error increases with signal frequency. These errors can be particularly high when power factor ($\cos\varphi$) is near zero (pure inductive or capacitive circuits).

However, if an alternate sequence is considered, phase errors ($\Delta\varphi$) are alternatively positive and negative and the effect of sampling errors tends to be nullified in average during the measurement cycle. This result is then obtained without need of external S&H circuits and this reason justifies the selection of an alternate sampling sequence for voltage and current signal acquisition.

3. SIMULATION RESULTS

Several MATLAB programs were developed to study the effects of the different error sources in digital power measurement systems. The main input parameters used for simulation purposes are: phase difference between voltage and current signals (φ), relation between signal and sampling frequencies (f/f_S), relation between fixed timing error and sampling period ($\Delta t/T_S$) and converter's number of bits (B).

Figure 2 represents the relative error of power measurement, caused by non-simultaneous sampling, as a function of timing error amplitude ($\Delta t/T_S$) for two different values of phase difference: $\varphi=\pi/6$ and $\varphi=\pi/3$. As expected, the errors are larger when phase difference is near $\pi/2$. For $\varphi=\pi/3$ the maximum error is almost equal to 30% when direct sequences are used (curves 1 and 3) and $\Delta t/T_S=1$. However, when for the same simulation conditions, alternate sequences are used, errors are always smaller than 1,2%.

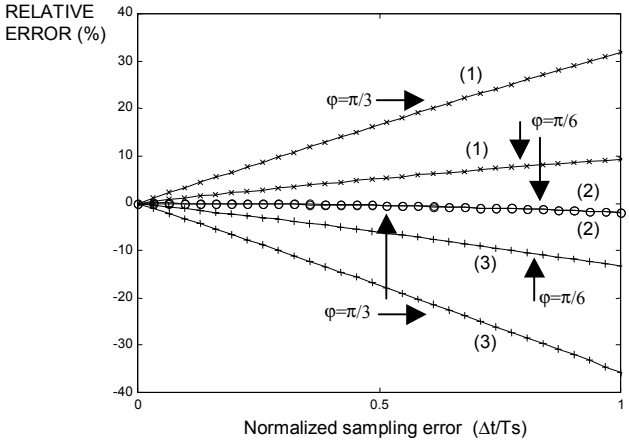

Fig. 2. Simulated relative error of power measurement caused by non-simultaneous sampling, as a function of timing error amplitude ($\Delta t/T_S$). Simulation parameters: $\varphi=\pi/6$ and $\varphi=\pi/3$, $f/f_S=1/32$, $0\leq|\Delta t/T_S|\leq 1$ and B=12 bits. Results for: (1) direct sequence with voltage delay, (2) alternate sequence and (3) direct sequence with current delay.

Figure 3 represents the effect of phase difference (φ) for a fixed sampling error amplitude ($\Delta t/T_S=0{,}5$). The phase difference varies between 0º and 85º with increments of 2,74º. Even when $\varphi=85$º, where the direct sequences gives absolute errors over 100%, the alternate sequence assures very low error amplitudes.

Finally, Fig. 4 represents the effect of sampling rate for a given phase difference ($\varphi=\pi/4$). Two different values of sampling rate relation are used: $f/f_S=1/32$ and $f/f_S=1/64$. As expected, measurement errors for direct sequences are lower when sampling rate increases but error levels of alternate sequences can only be achieved with direct sequences when the sampling rate is very high ($f/f_S<1/1024$).

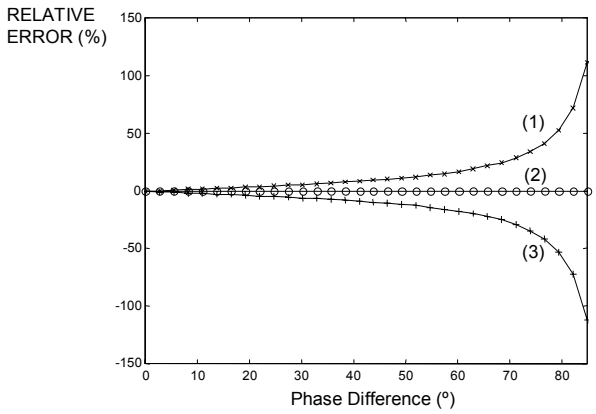

Fig. 3. Simulated relative error of power measurement caused by non-simultaneous sampling, as a function of phase difference between voltage and current signals. Simulation parameters: $0º \le \varphi \le 85º$, $\Delta\varphi = 2{,}74º$, $f/f_S = 1/32$, $\Delta t/T_S = 0{,}5$ and B=12 bits. Results for: (1) direct sequence with voltage delay, (2) alternate sequence and (3) direct sequence with current delay.

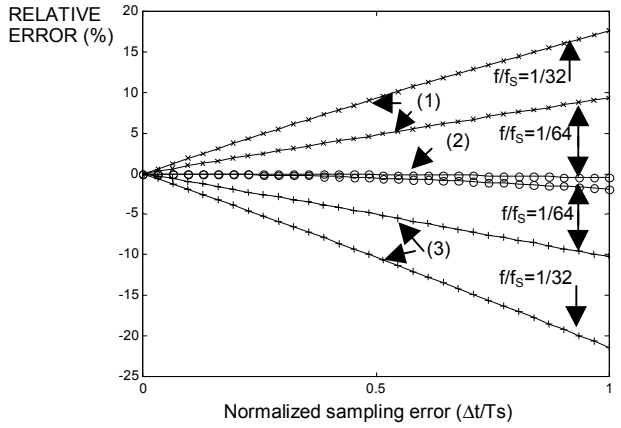

Fig. 4. Simulated relative error of power measurement, caused by non-simultaneous sampling, as a function of sampling rate. Simulation parameters: $\varphi = \pi/4$, $f/f_S = 1/32$, $f/f_S = 1/64$, $0 \le |\Delta t/T_S| \le 1$ and B=12 bits. Results for: (1) direct sequence with voltage delay, (2) alternate sequence and (3) direct sequence with current delay.

Simulation results clearly show that measurement errors can be very high and much larger than quantisation errors. Even when phase difference is near $\pi/2$ (pure reactive loads) or when relative sampling rate is small, the usage of an alternate sequence almost cancels errors due to non-simultaneous sampling of voltage and current signals.

4. EXPERIMENTAL RESULTS

A virtual instrument based on a data acquisition board was used to confirm the theoretical and simulation results. The main hardware components of the test system include a PC equipped with a data acquisition board, a digital phase-shifter and a signal generator. The software, developed with the graphical programming language LabVIEW [6], uses as main input parameters the sampling rate, the time delay between acquisitions and the phase difference between voltage and current signals. Alternate and direct sequence measurements of active and reactive power are obtained by changing the order of channels acquisition.

4.1. Digital Phase-Shifter

A digitally controlled phase-shifter was used to adjust the phase difference (φ) between voltage and current signals. The signal generator (HP33120-A) used for test purposes has a signal to noise relation (S/N) equal to 80dB and a spurious-free dynamic range higher than 70dB which assures that the generator is not a significant source of error. Figure 5 represents the hardware diagram of the digitally controlled phase-shifter circuit.

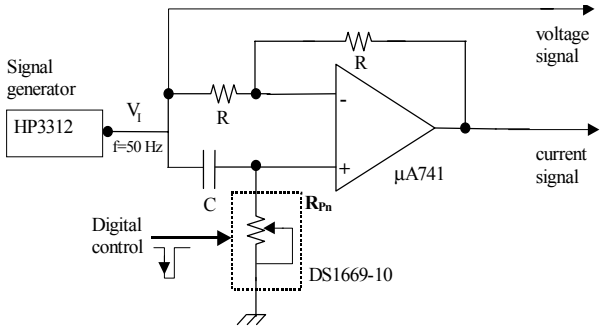

Fig. 5. Hardware diagram of the digitally controlled phase-shifter circuit (R=10kΩ, C=0,5μF).

The digital potentiometer (DS1669-10) specifications include 64 possible uniform tap points over its entire resistive range (0-10 kΩ), a cut-off frequency (-3dB) equal to 1MHz and an absolute linearity error lower than 0,75 LSB.

The resistance adjustment is set by using a single digital control line that causes the wiper position to increment for each low-going pulse, until the potentiometer reaches the maximum resistance, when it will reverse direction and wiper position decrements. If R_{Pn} represents the resistance of the digital potentiometer, after n low-going pulses, the phase difference between voltage and current signals is given by:

$$\varphi = -2\mathrm{arctg}\left(2\pi f R_{Pn} C\right) \qquad (7)$$

where f represents signal's frequency.

The phase-shifter characteristic enables an automatic measurement system characterisation, easy detection of hysteresis errors and easy implementation of averaging techniques to cancel random noise sources with null average values.

4.2. Results

Figure 6 represents the relative error of power measurement for direct and alternate sequences, when the following test conditions are used: $f/f_S = 1/32$, $\varphi = \pi/4$ and B=12. The continuous lines represent the simulation results and the different symbols, near each curve, represent the measurement data for twelve different amplitudes of sampling errors. In all the cases, the alternate sequence gives an active power measurement error smaller than 0,6%.

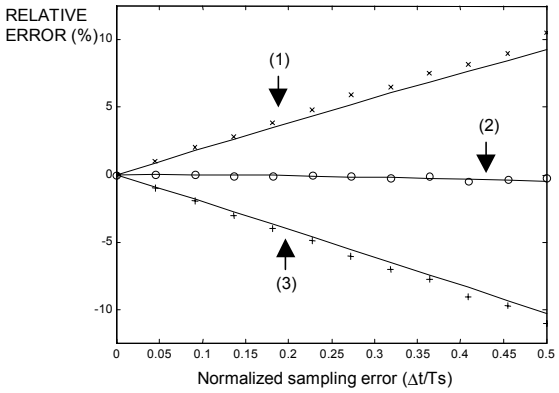

Fig. 6. Measured relative error of power measurement for direct and alternate sequences, for the following test conditions: $f/f_S=1/32$, $\varphi=\pi/4$ and B=12. Results for: (1) direct sequence with voltage delay, (2) alternate sequence and (3) direct sequence with current delay.

Figure 7 represents the error difference between simulated and experimental data. The differences, always lower than 1,25%, can be justifies by others error sources, namely: phase-shifter resolution and nonlinearity jitter errors and A/D conversion errors.

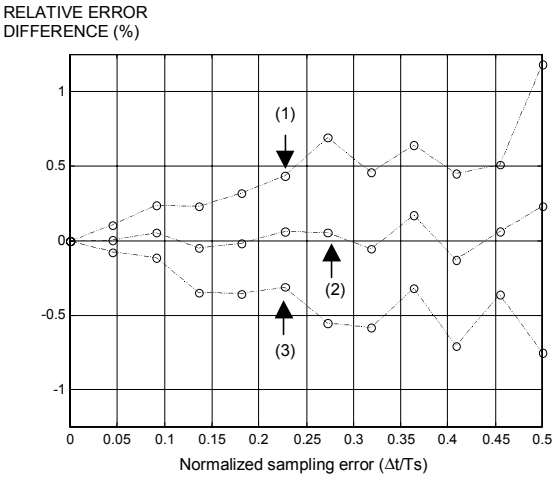

Fig. 7. Measured relative error differences between simulated and experimental results for: (1) direct sequence with voltage delay, (2) alternate sequence and (3) direct sequence with current delay.

4. CONCLUSION

The solution presented is particularly important for low-cost power measurement systems with a single ADC and no S&H circuits. Signal processing and A/D conversion delay effects are minimised by using alternate sequences. Thus, it is possible to extend the frequency domain of the measurement system without a significant degradation of its accuracy.

The principle presented for single phase active power measurements can be extended, with minor changes, to multiphase or reactive power measurements. In this last case, the only difference is that, before signal processing, the voltage and current samples must be phase shifted by a quarter of period relatively to its real phase difference (φ).

5. ACKNOWLEDGEMENTS

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