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TIME-INTERVAL MEASUREMENTS, USING TAPPED DELAY LINES IMPLEMENTED IN PROGRAMMABLE LOGICAL STRUCTURES

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Abstract – The time-interval measuring systems for time-resolved spectroscopy are discussed in this paper. For instance, for time-of-flight (TOF) spectrometry or lifetime decays measurement applications a simple gated counting system (boxcar), a real-time multichannel scaler (RTMS) or a time-interval interpolator is used. We present the new high-resolution (RTMS) system for an intensity function measurement. In this system, the digital tapped delay lines are used. These system with 1,0 ns and 0,5 ns resolution, with tapped delay lines implemented in the structure of the complex programmable logic device FLEX10K 30E are presented.

Keyword: Time-interval measurement, Multichannel scaler, delay lines.

1. INTRODUCTION

Many physical phenomena can be observed as random processes. Processes characterized by highly localized events, relative to the time of observation and distributed randomly in a continuum are of particular interest. Multiphoton ionization process, photoluminescence process of atoms and molecules can be good example of such process [1, 2].

The analysis of such processes is for instance applied in time-of-flight mass spectrometry and time resolved spectroscopy during the investigations of the decay time of the population of the excited atoms [3]. The method of measurement of the intensity function depends on the type of random process. One of the intensity functions measuring systems is the real time multichannel scaler – RTMS [3]. A high time-resolution and small dead-times should characterize the optimal intensity function measuring system. The measuring system consists of two consecutively working time-interval collecting register has a good resolution and a small dead-time. A high degree of the system integration can be obtained by using the regular structures of ASIC [4], FPGA [5, 6] or CPLD [7] devices.

The CPLD structures are very effective and useful for the counters, arithmetic, and the interface units implementation. Generally, the programmable CPLD devices are relatively fast and can operate with the signal frequency up to 300 MHz. An additional advantage of the modern CPLD structures is the possibility of the in-system programming (ISP) and reconfiguration. This feature allows for reconfiguration of the circuits directly in-system. It is enable us for up-dating the implementation and very fast response for the market signals.

Moreover the output signals generated by the circuit implemented in the CPLD device have very short rise and fall times, necessary for a high-resolution system.

This real-time measuring system, implemented in programmable logical structures, enable us to obtain a resolution of the time-interval measurement equal to 0,5 ns or 1,0 ns and double-pulse resolution equal to 5 ns.

2. MEASURING SYSTEM

The time-interval measuring system consists of two units: voltage controlled tapped delay line and data acquisition unit. A block diagram of the multichannel system for intensity function measurement with resolution 0,5 ns or 1,0 ns is shown in Fig. 1 and Fig. 2.

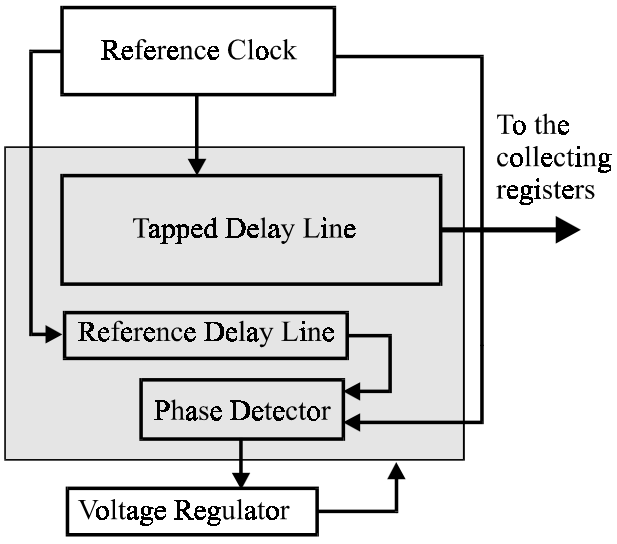


Fig. 1. The unit of voltage controlled tapped delay line

In Fig. 1 the voltage controlled tapped delay line is shown. In Fig. 2 the constant fraction discriminators, the collecting registers and other elements of the data acquisition unit of the measuring system are shown. The constant fraction discriminators allow to very precise location of the trigger and input pulses in time.

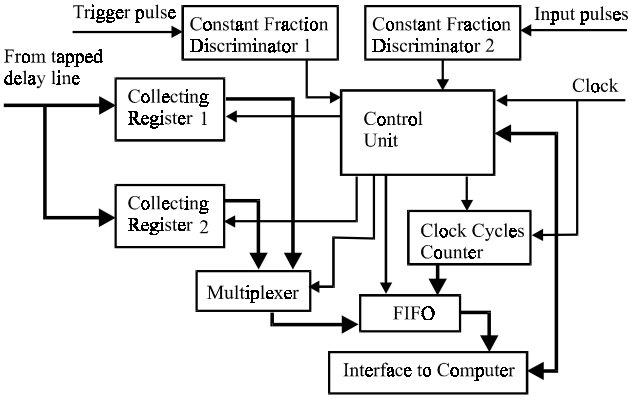


Fig. 2. Block diagram of the measuring system (Without tapped delay line unit)

The reference clock should be a low jitter and very stable oscillator, which period T is equal to

$$T = n\tau, \tag{1}$$

where n is a number of taps and τ is a single tap delay.

During the measuring cycle two collecting registers are working consecutively in two different modes.

In this system, during the measuring mode, the collecting registers are edge triggered by the trigger pulse and each of the input pulses, latching the data (reference clock phase) in a collecting registers [7]. During the data transfer mode, the data are transferred from the appropriate collecting register and from the clock cycles counter to the memory. If one of the collecting registers is in measuring mode the second is in data transfer mode.

As well as the constant fraction discriminators and standard clock, the FIFO memory unit is outside the CPLD device. However the small memory can be organized inside the CPLD using the embedded blocks external memory can be bigger increasing range of the measuring system.

When the trigger pulse occurs, the clock cycles counter begins to count the number of clock cycles. In this case the resolution of such measuring system is limited by the resolution of the phase measuring circuit (tapped delay lines) and the standard clock frequency.

The maximum intensity of the input pulses is not limited by the memory access time (usually several ns), because the collecting registers work consecutively. A double-pulse resolution of the measuring system is usually limited by constant fraction discriminators (usually to 5 ns). In consequence of such limits each collecting register can counts zero, one or two pulses during one clock period (in this case 8 ns). Of course the data is transferred and recorded only if the number of counts is different then zero. The high-resolution system allows collection of the pulses from a detector for highly dynamical intensity function processes.

3. DELAY LINE

Uncertainty of the measuring results of the time-interval measuring system depends straight from the delay line quality.

Small differences between calculated and measured delay times of the delay taps can be obtained by the special method of the delay line design. This method depends on control of the delay times during the design process. Algorithm of the design process is shown in Fig. 3.

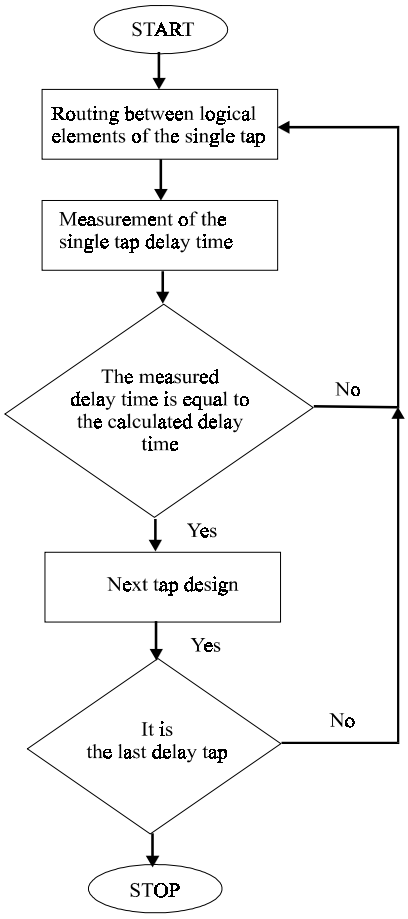


Fig. 3. Algorithm of the delay line design process

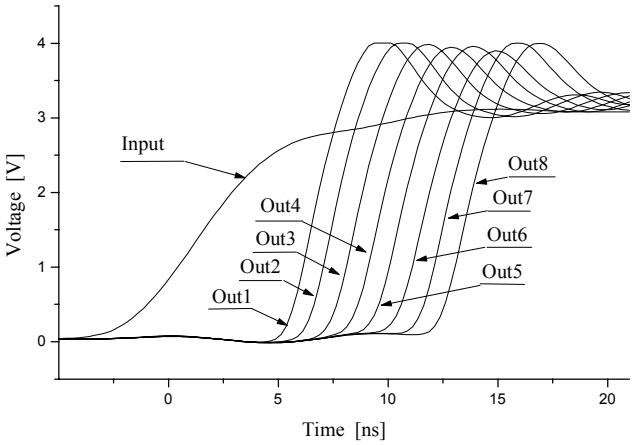
The delay time differences obtained during design process of the 8-tap delay line are presented below, in the Table 1.

TABLE 1. Measured and calculated delay times

Number of output pin	Measured delay times [ns]	Calculated delay times [ns]
Out8	11,88	11,90
Out7	10,93	10,90
Out6	9,92	9,90
Out5	8,88	8,90
Out4	7,92	7,90
Out3	6,91	6,90
Out2	5,87	5,90
Out1	4,94	4,90

The programmable device used for the delay line implementation is fast, so the rise time of the output signals is relatively small. The signals from 8-tap and 16-tap delay lines implemented in a FLEX 10K 30E device are shown in Fig. 4.

a)



b)

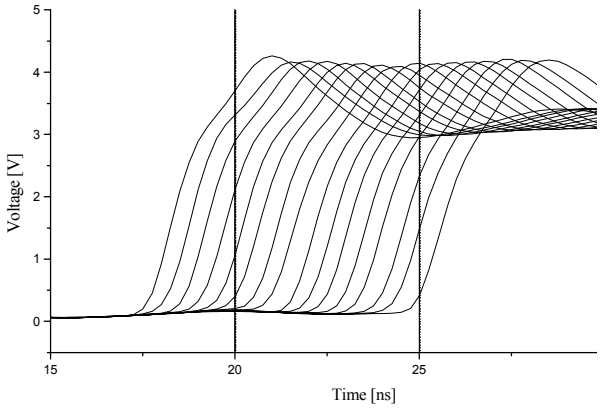


Fig. 4. The measured (Oscilloscope LeCroy LT374) output signals from
a) 8-tap (1,0 ns)
b) 16-tap (0,5 ns) delay lines

These signals are fed to the data inputs of the collecting registers. Each collecting cycle is equal to the reference clock period $T = 8$ ns.

However the tapped delay lines are sensitive on temperature fluctuation (0,3 %/K), they are sensitive also on a supply voltage fluctuation (5 %/0,15 V) and can be controlled by the supply voltage [6]. When the supply voltage increases the tap delay decreases.

The influence of the temperature fluctuations on the delay time for the single tapped delay line is shown in Fig.5. When the temperature increases the tap delay also increases.

It means that stabilization of the delay line is possible using the reference delay line characterized by the total delay time equal to the reference clock period and the additional correcting circuit. This circuit consists of the fast phase detector, shown in Fig.6 and the voltage regulator. The voltage regulator consists of the filter, shown in Fig. 7 and controlled power supplier, which is shown in Fig. 8.

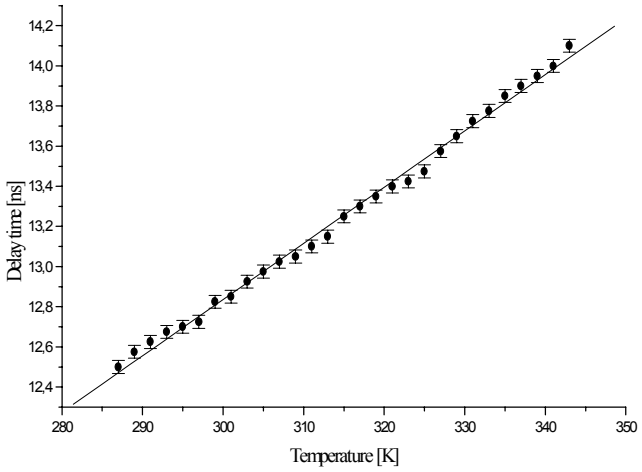


Fig. 5. The delay time in function of temperature

The reference delay line and the phase detector are implemented in the same programmable device, which include the tapped delay line. The voltage regulator is realized outside the CPLD, and consists of discrete components. The phase detector generates pulses of width depending from the phase shift at the both clock inputs of the edge-triggered flip-flops. If the CPLD temperature increases the total delay of the reference delay line also increases and the width of the pulses on the output Dout1 is greater than the width of the pulses on the output Dout2.

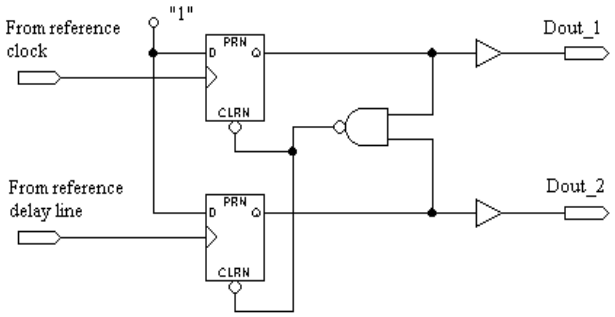


Fig. 6. The phase detector [6]

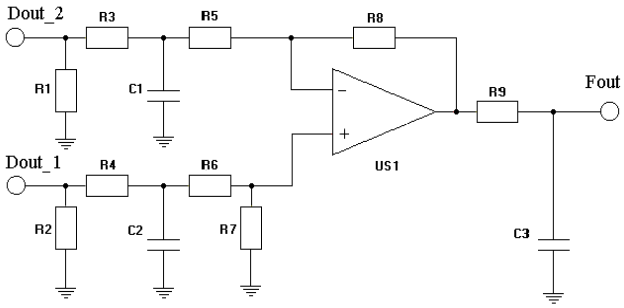


Fig. 7. The voltage regulator filter

The filter converts the different width pulses from the phase detectors outputs to the control signal for the supplier.

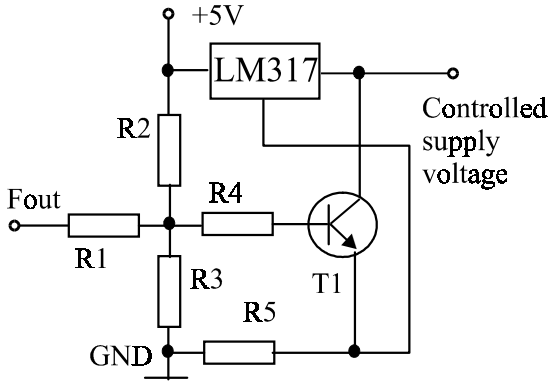


Fig. 8. The controlled power supplier

Final test result of the temperature compensated delay line is shown in Fig. 9.

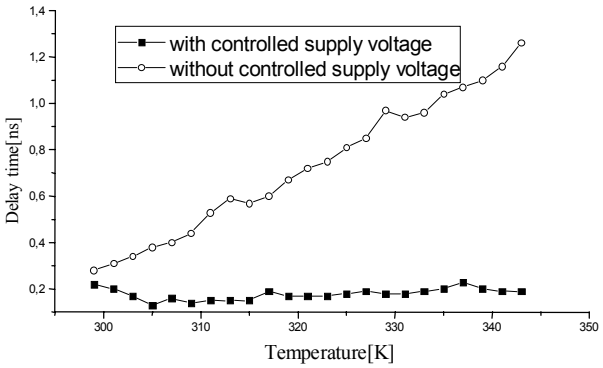


Fig. 9. The delay times: the temperature compensated and non-compensated delay line in function of temperature

As it is shown in Fig. 9, influence of the temperature fluctuations on the temperature compensated delay time of the tapped delay line is relatively small and can be omitted. In this case, the maximum deviation from the nominal delay is equal to 100 ps in full range of the temperature fluctuations.

4. CONCLUSIONS

The results obtained during the tests confirm that application of the programmable logical devices in the construction of high-resolution intensity function measuring systems gives good results. However most of the system units can be functionally (using HDL – hardware description language) described, we want to point out, that the architecture of tapped delay lines should be structurally described. We should emphasis, that one of the advantages of the application of programmable logical devices is the improvement of the metrological parameters. Moreover, application of such devices increases the flexibility of the measuring system, increases the degree of system integration and leads straight to increasing the system reliability. It is very important, that in this way the system resolution increases without limiting of the double-pulse resolution (dead-time).

Acknowledgments

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