

DESIGN, IMPLEMENTATION AND METROLOGICAL CHARACTERIZATION OF A COST-EFFECTIVE DSP-BASED W-CDMA TRANSMITTER

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Abstract – A W-CDMA transmitter based on the TMS320C6701 digital signal processor is here presented. The most significant strategies adopted for its implementation are described in detail; all the results obtained from an exhaustive metrological characterization are also given. Thanks to the high portability, good flexibility and, above all, very low cost, the W-CDMA transmitter is suitable for educational purposes, mainly concerning measurements on telecommunication systems, at universities as well as research centres.

1. INTRODUCTION

Nowadays, most measurement instruments for designing, manufacturing, and testing telecommunication systems is very expensive if related to the poor economical resources that a number of universities, as well as research centres with didactic aims, have at their disposal [1-8],[19],[21]. The difficulty and, sometimes, impracticality of acquiring the aforementioned instrumentation limits the possibility of these institutions of enhancing their educational offer; no advanced classes can, in fact, be activated, capable of tracking the rapid evolution of the technology and measurement strategies in the telecommunications field.

This is the reason why the Department of Computer Science and Control Systems of the University of Naples - Federico II and the National Multimedia Communications Laboratory of Naples - C.N.I.T. (Interuniversity Consortium for the Telecommunications) have decided to cooperate in a new research activity concerning the design, implementation, and metrological characterization of cost-effective measurement instruments for educational purposes.

In particular, a W-CDMA downlink transmitter, implemented on the EVM TMS320C6701TM Evaluation Module by Texas Instruments [9-10], generally exploited for audio applications, is described in the paper. It is fully compliant to 3GPP (Third Generation Partnership Project) specifications [11],[12]. Besides its inherent cost-effective nature, the proposed transmitter is characterized by (i) high portability, the EVM board can easily be hosted by any PC, and (ii) good flexibility, its digital signal processing

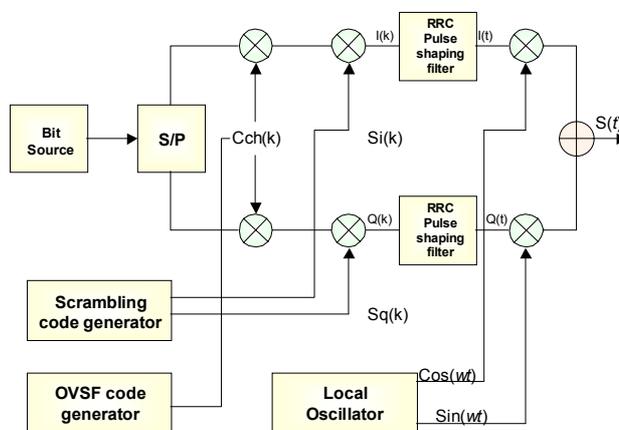


Fig. 1. W-CDMA transmitter scheme.

software can straightforwardly be updated to make it provide other types of communication signals. Its suitability to educational purposes regarding 3G (Third Generation) telecommunication systems is proved by the satisfying results of an exhaustive metrological characterization.

2. THE HARDWARE

The main blocks of a W-CDMA transmitter are: bit source, OVSF code generator, scrambling code generator and RRC (Root Raised Cosine) pulse-shaping filter (Fig. 1). The information source generates a bit pattern at a fixed rate [12],[20],[22].

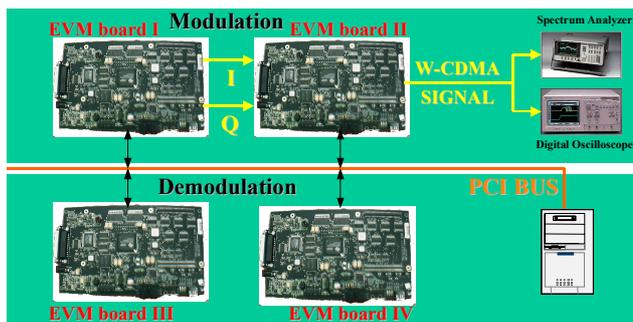


Fig. 2. Hardware platform.

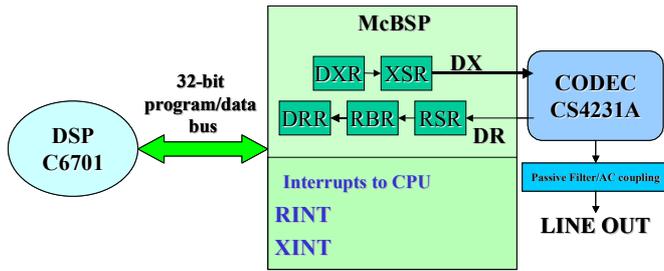


Fig. 3. Main devices hosted by EVM TMS320C6701™ board.

After being split in two components by the S/P (Serial-to-Parallel) converter, the bit stream is multiplied by the OVSF code. The obtained result is, then, multiplied by the scrambling code, and filtered by the RRC pulse-shaping filter. A QPSK modulator, then, modulates each component.

The realized W-CDMA transmitter relies upon the hardware architecture shown in Fig. 2. Four EVM TMS320C6701™ boards are used as plug-in-cards in a PCI expansion slot of a PC (Pentium III, 800 MHz, 256 MB RAM). The EVM is a relatively low-cost demonstration board allowing the assessment of the performance of ‘C6701 processors thanks to the availability of other devices on the board itself (Fig. 3). Only the EVM board I and II are exploited to synthesize the W-CDMA signal. The former generates both I and Q components, and the latter the QPSK modulated signal. Other two EVM boards complete the hardware architecture; they will be used for a future implementation of a W-CDMA receiver.

All analogue signals are synthesized by a 16-bit stereo audio CODEC CS4231A™ by Crystal, the generation frequency of which can be selected in the range 5.5 – 48 kHz, and the amplitude of the output signal can be raised up to 2.8 V_{pp}. It is specifically designed for audio applications. The CODEC and the DSP are directly interfaced by a programmable serial interface called Multichannel Buffered Serial Port (McBSP), which communicates with the DSP CPU through a 32-bit data bus. The data sent by the CPU to the McBSP are stored into the Data Transmit Register (DXR), and, then, shifted into the Transmit Shift Register (XSR). The data are, finally, sent to the CODEC by the Data Transmit (DX) terminal line. The McBSP receives the data from the audio CODEC through the terminal line Data Receive (DR). At first, they are stored into the Receive Shift Register (RSR), then, copied into the Receive Buffer Register (RBR), and, at the end, into the Data Receiver Register (DRR) for being sent to the CPU.

3. THE SOFTWARE

The algorithm has been designed and developed by using the Texas Instruments software development platform called Code Composer Studio 2.0™. The platform includes a number of software tools, which allow the creation of applications consisting of C/C++ or assembly source files, specific libraries, and a hardware configuration file.

The developed software is based on an appropriate interrupt service routine, which runs as soon as the audio CODEC is ready to process a new sample of the output signal, and enables the McBSP to send an interrupt transmit

request to the DSP CPU. Because the ISR processing time limits the minimum interval between two consecutive samples to be generated, two different ISRs have been designed in order to (i) satisfy 3 GPP recommendations as close as possible, and (ii) guarantee as high a generation rate of the output W-CDMA signal as possible. The first ISR, running on the DSP of the EVM board I, is mandated to the generation of the I and Q components, while the second ISR accounts for the QPSK modulation through the EVM board II.

As a result, the I/Q modulation is performed at the lowest generation rate (5512 S/s) available, while the CODEC on the EVM board II acquires them at a sample rate of 48 kS/s, and generates the W-CDMA signal at the same rate.

3.1. The Software on the EVM board I

The main blocks, shown in Fig. 4, are described in the following subsections:

A. RRC Pulse Shaping Filter Initialisation

According to 3GPP specifications, the shaping pulse filter is a root raise cosine with a roll-off coefficient equal to 0.22. It has been designed using the equiripple method in MATLAB™ environment [13]. So, a symmetric FIR filter having 25 tapped delays has been obtained. The initialisation of the filter is performed before the idle loop.

B. OVSF Code Generation

Although the related chip rate has been fixed equal to 3.84 Mchip/s, the W-CDMA system supports variable bit rate through the OVSF (Orthogonal Variable Spreading Factor) codes. These codes have a variable length, from 4 up

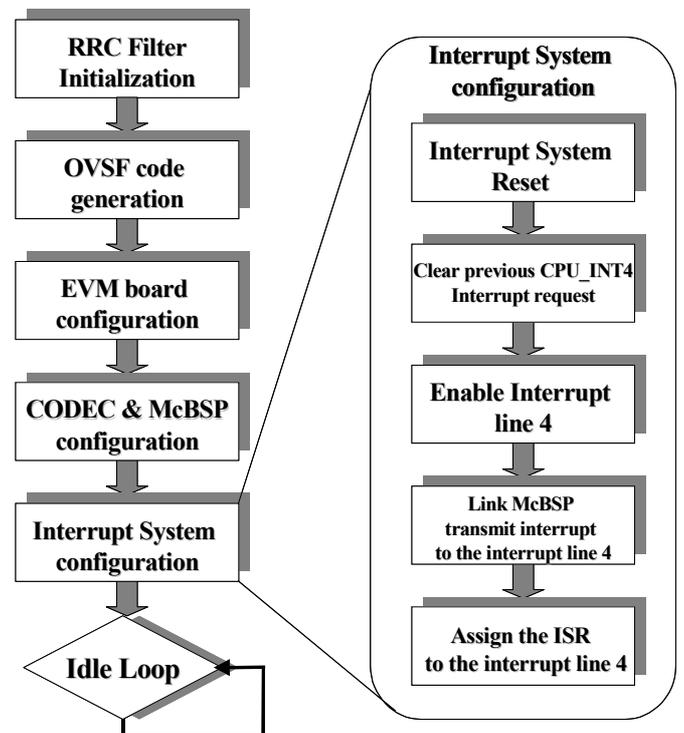


Fig. 4. Flow diagram of the main program running on the EVM board I.

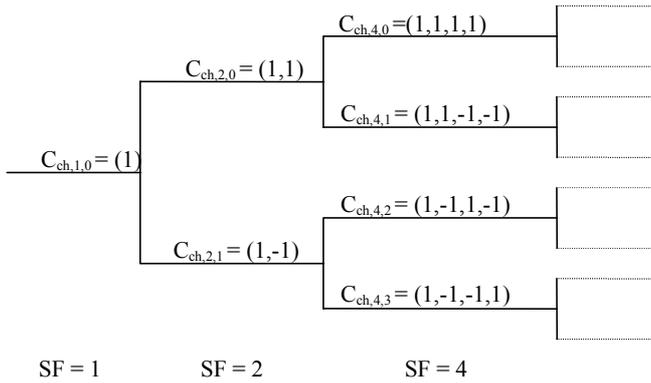


Fig. 5. OVSF code generation tree.

to 512. They are generated by a binary tree (Fig. 5): each code is characterized by the spreading factor (SF), used for locating the tree level, and a bit pattern, used for pointing out a specific path in the binary tree [12]. Once the desired SF has been fixed, the implemented algorithm generates the OVSF code by applying a recursive procedure to a vector of SF integers. In the first step, all vector elements are set to 0, but the first, which is set to 1. A different integer vector defines the path in the binary tree. In the k^{th} step, the first $2^{(k-1)}$ elements of the vector are recopied into the first 2^k positions. Their sign depends on the elements composing the specific pattern. The OVSF code generation procedure ends after $\log_2 \text{SF}$ steps.

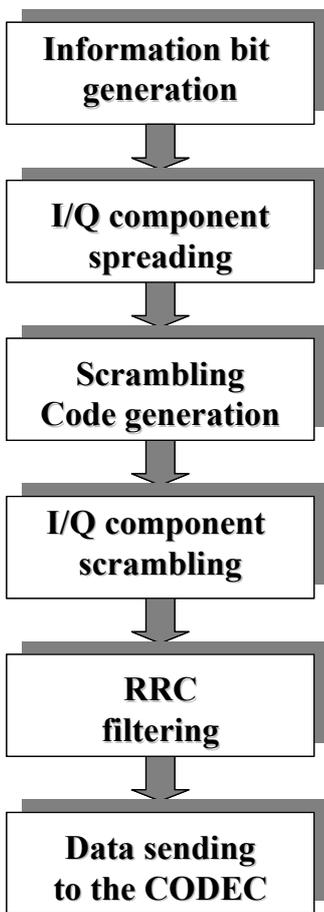


Fig. 6. ISR flow diagram.

C. EVM board initialisation

The board is reset and all device registers initialised.

D. CODEC and McBSP configuration

There are two available McBSP modules on the EVM board. The McBSP0 is here used and configured in order to send (receive) 32-bit data frames to (from) the 16-bit stereo CODEC (the CODEC serial interface has obviously been enabled). The McBSP0 is synchronized through a signal generated by the CODEC itself.

E. Interrupt System Configuration

The 'C67xx DSP family has 16 interrupt sources, and only 12 of them can be set by the users. So, they have to be mapped with the CPU interrupts INT4-INT15 by

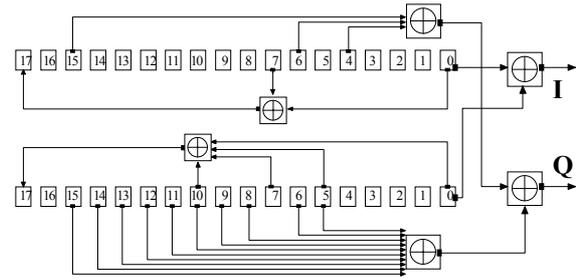


Fig. 7. Scrambling code generation scheme.

using two Interrupt Multiplexed Registers. The CPU interrupt INT4 is here enabled and coupled to the McBSP transmit interrupt request. Then, the interrupt service routine is assigned to INT4 by refreshing the Interrupt Service Table (IST). At the end, the interrupt system of the DSP is enabled.

3.2. The Interrupt Service Routine on the EVM board I

The interrupt service routine (ISR) plays a fundamental role in the software of the EVM board I. The serial communication is regulated by the audio CODEC. Specifically, the audio CODEC enables the McBSP0 to send an interrupt transmission request, XINT, to the CPU as soon as it is ready to process a new sample. Then, the associated ISR will be running during the endless idle loop. The ISR outputs the single W-CDMA complex chip after generating, spreading; scrambling and pulse shaping random data bits (Fig. 6).

The W-CDMA scrambling codes are generated by opportunely combining two Gold sequences. The polynomial generators are:

- $P_1(x) = 1 + x^7 + x^{18}$;
- $P_2(x) = 1 + x^5 + x^7 + x^{10} + x^{18}$;

At first, the shift registers are implemented by using the 18 least significant bits of two 32-bit integer numbers (Fig. 7).

3.3. The Software on the EVM board II

The software running on the EVM board II implements the QPSK modulation. The whole flow diagram is depicted in Fig. 8, but that related to ISR. During the initialisation and configuration stage, the interrupt system is configured in such a way as to associate the CPU interrupt INT4 with the McBSP0 receive interrupt RINT. So, the related ISR will be running as soon as

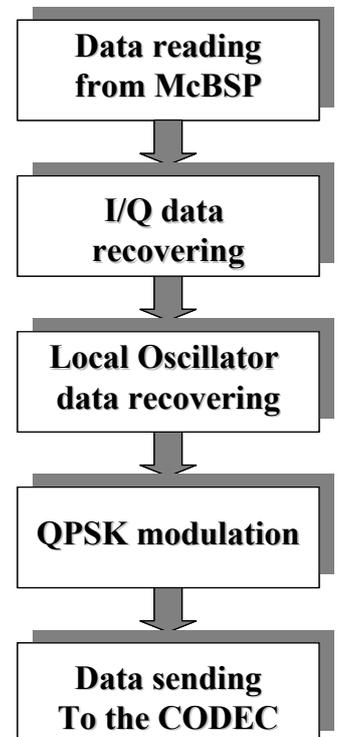


Fig.8. Flow diagram of the main program running on the EVM board II.

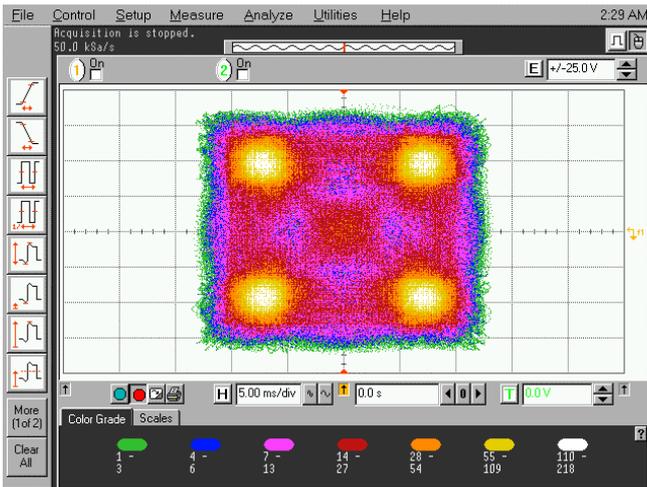


Fig. 9. Constellation diagram.

the audio CODEC acquires a single sample of the I/Q components synthesised by the EVM board I. As the McBSP0 can send (receive) 32-bit data to (from) the 16-bit audio CODEC, each datum conveys two samples: one related to the I component (the 16 least significant bits), and the other to the Q component (the 16 most significant bits). So, the first ISR step is to separate or recover the aforementioned samples by means of two hexadecimal masks. Then, the ISR reads the current value of the two quadrature carriers, generated by a look-up table that implements a digital local oscillator [14]. At the end, the modulation takes place, and the synthesized sample of W-CDMA signal is outputted through the left channel of the stereo CODEC.

3.4. Final considerations

The EVM board I generates the I/Q components at 5512 kS/s. The W-CDMA signal is synthesised by the EVM board II at a generation rate equal to 48 kHz. The obtained carrier frequency is equal to 11 kHz with a bandwidth equal to 2.6 kHz. The associated chip rate is fixed to 1378 chip/s according to a bit rate equal to 172 bit/s (SF = 8). The maximum amplitude of the output signal reaches the full-scale value ($2.8 V_{pp}$) of the CODEC.

4. METROLOGICAL CHARACTERIZATION

4.1. Main diagrams and power spectrum

The adopted digitising oscilloscope, namely Agilent Technologies 54820A™ (2 GS/s maximum sample rate, 500 MHz bandwidth), is used in normal mode for obtaining the polar diagram and, then, in colour grade mode for obtaining the constellation diagram. The sample rate has been chosen equal to 50 kS/s, the vertical scale equal to 300 mV/div, and the horizontal scale equal to 5 ms/div. It is so possible to view on the screen a 50 ms interval or 120 chips of the W-CDMA signal transmitted.

The constellation diagram is obtained by superposing a number of polar diagrams: the brighter the colour of a certain point, the more frequently the signal reaches the point. As it can be noted, the diagram shown in Fig. 9 matches the usual constellation of a QPSK modulated signal.

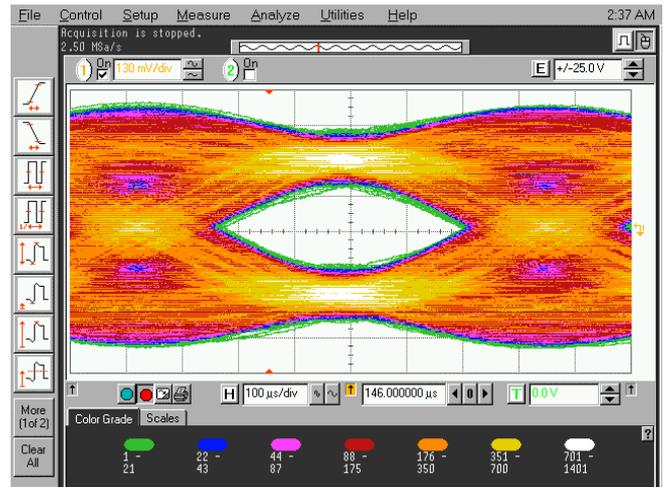


Fig. 10. Eye diagram.

The eye diagram has been evaluated by generating a synchronization signal through the DSP of the EVM board I. Fig. 10 shows the results provided by the oscilloscope with the vertical scale set to 300 mV/div and the horizontal scale to 100 μs/div. Several measurements of both width and height of the eye have been carried out. With regard to the width, the average value and experimental standard deviation of the obtained results have resulted equal respectively to 202.9 μs and 0.7 μs for the I component, and 206.7 μs and 2.1 μs for the Q component. As for the height, an average value of 764.4 mV and an experimental standard deviation of 7.8 mV have been experienced for the I component, while an average value of 760.0 mV and an experimental standard deviation of 9.9 mV has characterized the Q component.

Fig. 11 shows the power spectrum of the W-CDMA signal supplied by the proposed transmitter, as provided by the spectrum analyser, namely Agilent Technologies 8563EC™; the related bandwidth has resulted equal to 2.6 kHz.

4.2. EVM evaluation

All communication systems have a measure of modulation quality; a number of ways to measure it thus

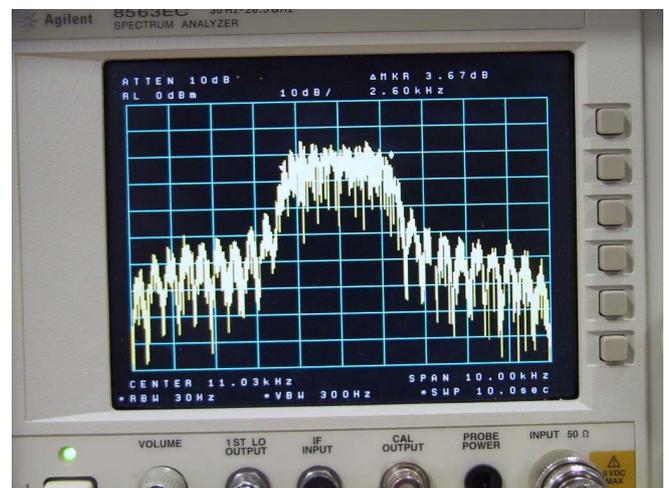


Fig. 11. Power Spectrum.

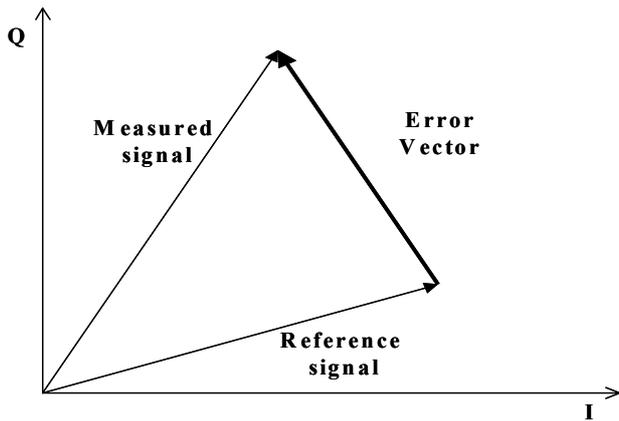


Fig. 12. Error vector definition.

exist. In FM-based systems FM deviation and distortion are accounted for; the global phase error is evaluated in GSM systems, while Error Vector Magnitude (EVM) is peculiar to W-CDMA systems [16-18].

The error vector is the difference, at each chip clock transition, between the ideal reference signal and the measured signal in the I/Q diagram (Fig. 12); EVM is its magnitude, the evolution of which versus time is also of great interest [15],[18]. There are different types of EVM measurements; in the following the QPSK EVM is referred to.

Demodulating the data bits from the received signal and then re-modulating these bits synthesize the reference signal. As the QPSK EVM measurement does not descramble and despread the signal into symbols and back into chips to calculate the appropriate reference, the OVSF spreading or complex scrambling errors cannot be detected. QPSK EVM is, in fact, expressly mandated to the evaluation of signal modulation quality at chip level only; it is so possible to better highlight the most common I/Q impairments, such as gain imbalance, quadrature error and offset voltages.

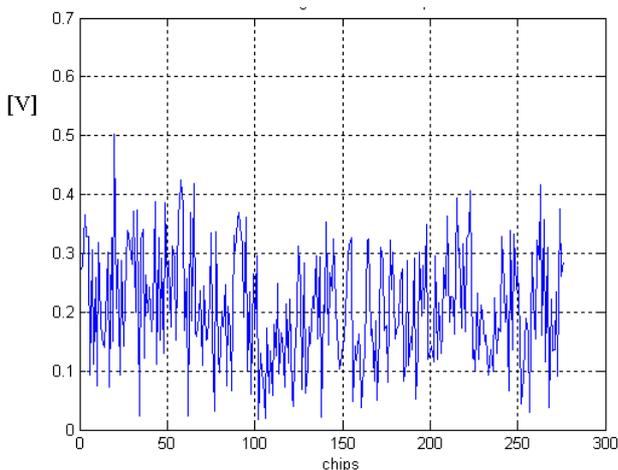


Fig. 13. QPSK EVM Evolution versus chips.

In Fig. 13 the evolution of the measured QPSK EVM versus chips is shown. It has been obtained through the

application of the measurement procedure depicted in Fig. 14.

5. CONCLUSIONS

The paper has presented the realization strategies along with characterization results of a DSP-based, W-CDMA transmitter. Its good portability, high flexibility, satisfactory metrological performance, and very low-cost make the proposed transmitter suitable to didactic purposes, especially in the field of measurements on telecommunication systems.

Future research activity is mainly oriented to:

- implement, on the same hardware platform, a W-CDMA multi-channel transmitter along with a proper receiver, which can allow the setting up of other fundamental measurements on telecommunication systems and apparatuses;
- integrate specific daughter boards on the adopted EVM boards in order to acquire and synthesize telecommunication signals with higher bandwidth and intermediate frequency than those characterizing the output signal of the proposed transmitter.
- develop other didactic applications by exploiting the whole set of instruments that CNIT has got.

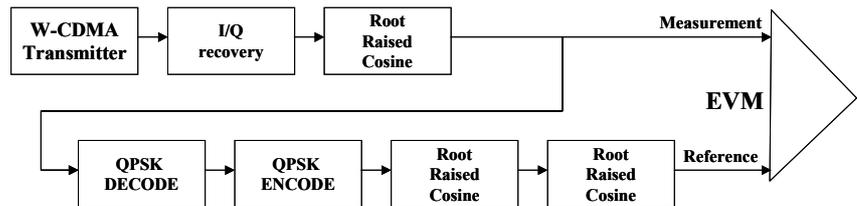


Fig. 14. QPSK EVM measurement procedure.

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