A Precise Amplifier for Digitally Synthesized Source

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ABSTRACT

A precise power amplifier is described in the paper. It was designed to amplify the output ac voltage of a digitally synthesized source from 5 V to 5, 10, 20, 30 or 50 V in 0… 1 kHz frequency range. The five voltage gain coefficients may be selected by GPIB and RS-232 interfaces or from the keyboard. The main application of the amplifier is the ac-dc voltage calibration system, especially useful for evaluation of thermal converters at low frequencies.

Keywords: precise amplifier, digitally synthesized source, calibrators, ac-dc transfer, thermal converter.

1. INTRODUCTION

The digitally synthesized source (DSS) generates a very stable sinusoidal signal in frequency range from 10 mHz to approximately 1 kHz. The DSS is mainly used to evaluate thermal converters (TC) in the low-frequency range [1] or to perform low-frequency ac-dc calibrations. The main distinction between voltage calibrator and the DSS is the higher stability of the output ac voltage of the latter at very low frequencies. The relative short-term stability of the ac voltage generated by the DSS is better than 10^{-5}. Moreover most of commercially available precision calibrators are unable to generate frequencies lower than 10 Hz.

Unfortunately the output ac voltage of the typical DSS is limited to about 7 V [2,3,4,5] while the low-frequency ac-dc calibrations will be in the near future performed up to 1000 V. The voltage gain of commercially available precision power amplifiers (for example Fluke 5205A) is fixed at 100 so they are not able to amplify the output voltage of the DSS to the required 1000 V.

A solution to these problems is the amplifier presented in this paper. It extends the ac voltage range of the DSS to approximately 50 V. Cascading the described amplifier with the Fluke 5205A it is possible to generate a 1000 V sinusoidal signal using the DSS. For ac-dc calibrations at voltage levels up to 50 V the amplifier can replace the Fluke 5205A amplifier.

2. REQUIREMENTS

The main part of the DSS is a digital-to-analog converter (dac) which reconstructs the low frequency sinusoidal signal from sine samples stored in the read only memory (ROM). The waveform at the output of the dac is distorted due to sampling, quantization, glitches, limited slew rate, noise and other effects (Fig.1). Reducing the energy of harmonics and glitches is possible by using a low-pass filter at the output of the waveform dac. A typical pass band of the filter is from dc to 5… 20 kHz, hence the fundamental of the reconstructed signal is almost unchanged.

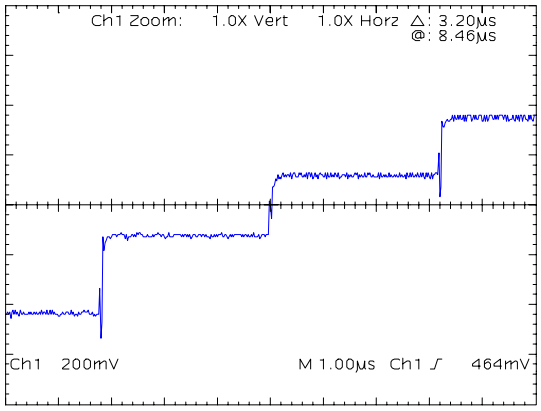

Fig.1 A typical unfiltered output waveform of the DSS

A common method to vary the output voltage of the DSS is to adjust the dc reference voltage applied to the input of a multiplying waveform dac. This method, though very convenient, leads to additional errors. This is because the glitch and noise effects remain nearly constant contrary to the main signal, which is proportional to the dc voltage applied to the dac reference input. Therefore the harmonic content of the dac output signal tends to increase with decreasing the output voltage of the DSS. It can lead to additional errors because of limited bandwidth of the calibrated instruments. Hence it is reasonable to keep the dc voltage at the dac reference input at a constant level. Of course there must be a way to change the ac voltage. In the particular application - the ac-dc transfer calibration with thermal converters - it is enough to use only a few ac voltage values. For example, for a typical step-up ac-dc calibration procedure the following ac voltages may be applied to the input of the TCs: 5; 10; 20; 30; 50 V. For 5 V ac output voltage of the DSS it implies the following gain coefficients of the amplifier: 1; 2; 4; 6; 10, respectively.

The rms output current of the amplifier has to be at least 30 mA for ac-dc calibration purposes. The 50 mA seems to be a more safe value.

All modern ac-dc calibration systems are fully automatized. The most often used interfaces in the calibration laboratories are GPIB and RS232. The amplifier should have built the both. For the operator convenience the amplifier should the keyboard as well.

3. THE AMPLIFIER DESIGN

The general schematic diagram of the amplifier is shown in Fig.2.

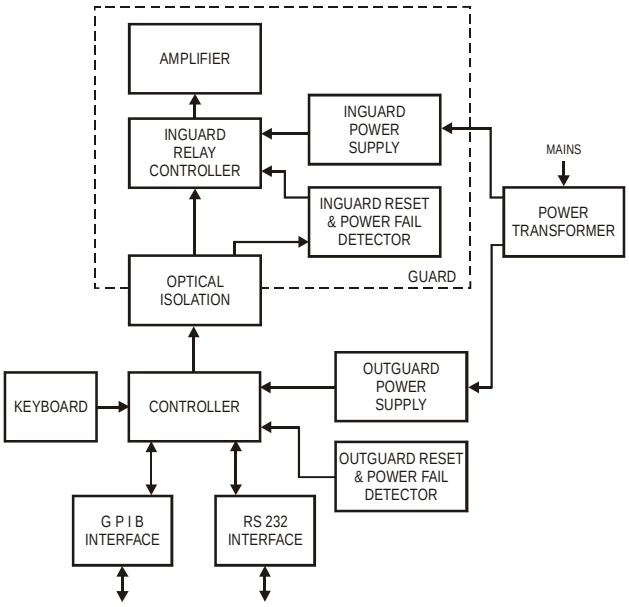

Fig.2. General schematic diagram of the amplifier

It is divided into three main sections:
- guarded analog and digital section (called inguard);
- earth-line referenced digital circuits (called outguard);
- triple shielded toroidal power transformer.

The simplified schematic diagram of the guarded analog part of the amplifier is shown in Fig.3. The input signal goes through the input bypass relay, which can switch off the amplifier providing a direct link between the input and output binding posts. Next, the signal enters the buffer relay. This relay switches on or off the precision buffer at the amplifier input. The buffer increases the input impedance of the amplifier to 10 MΩ || <200 pF. Without the buffer the input impedance of the amplifier is relatively small: 1… 10 kΩ, depending on the voltage gain. Next, the signal enters the composite amplifier input. The output of the amplifier is connected with the output bypass relay and operate/standby relay. The latter internally connects or disconnects the output binding posts from the amplifier. The power on state of this relay is standby. Not shown in Fig.3 is the local/remote sense relay which is located in the output sense high and low path. This relay switches between local sensing, i.e. sensing directly at the output binding posts or remote sensing – through additional sense high and sense low output binding posts.

The composite amplifier works in the inverting configuration shown in Fig.4. It is composed of three operational amplifiers forming a high performance, high-voltage operational amplifier.

In comparison with noninverting configuration the inverting one possesses the following advantages:

- the common-mode input voltage of the amplifier is nearly zero for symmetrical power supply. Therefore the linearity of the output vs. input voltage characteristics is not degraded by the change of the common-mode signal;
- it is much easier to improve the dc performance of the amplifier by using an additional zero-drift amplifier;
- there is no current injected to the signal (or high-quality, H.Q.) ground from the resistive feedback network;
- the slew rate of the inverting amplifier is higher than that of noninverting one because the common-mode input capacitance of the amplifier is not recharged during input voltage transients.

The main drawback of the inverting configuration is the low input impedance. This disadvantage must be overcome by using the four-wire connection (known as Kelvin or sense) of the input or by using an input buffer. The latter degrades the dc performance of the amplifier, but is necessary for DSS without four-wire output capability.

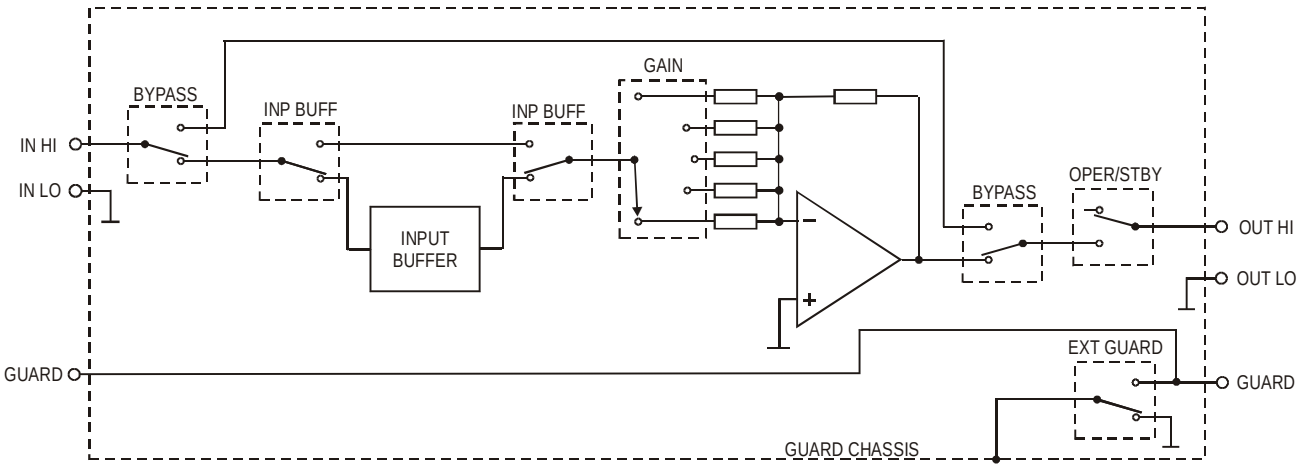

Fig.3. Simplified schematic diagram of the guarded analog part of the amplifier

The main amplifier U1 is a high-voltage hybrid power operational amplifier. This amplifier settles to 0.1% of the steady value typically within 1 μs and its slew rate is approximately 700 V/μs. The maximal peak output voltage of the U1 is approximately ±80 V making possible to achieve more than 50 V rms at the output. To minimize the input offset voltage and its drift of U1 an additional fast-settling (about 500 ns to 0.01%) and precision amplifier U2 was used. Its output controls the noninverting input of the U1.

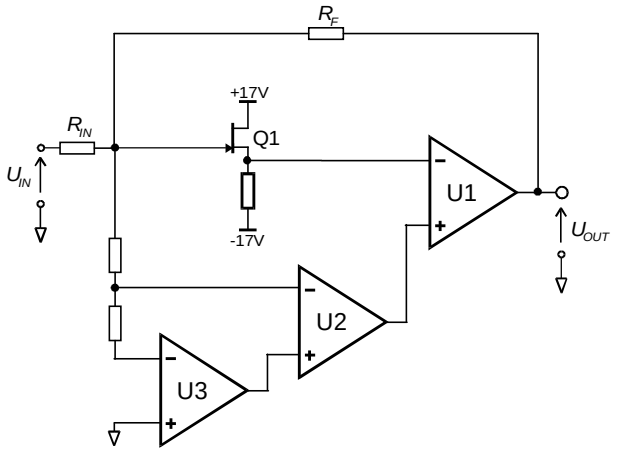

Fig.4.Schematic diagram of the composite amplifier

The small input offset voltage of U2 is further minimized by the third zero-drift amplifier U3. This amplifier has exceptional dc parameters: the typical input offset voltage is about 1 μV and its temperature drift can be as low as 5 nV/K. The amplifier was chosen not only because of its good dc parameters but also because of its randomized autozero clock frequency. The last property leads to negligibly small intermodulation with the amplified signal. The U3 amplifier contributes its own open-loop gain to the open-loop gains of the U1 and U2. The resulting open-loop gain of the composite amplifier is extremely high. At dc it exceeds 220 dB leading to high accuracy and stability.

To minimize the influence of the input bias current of U1 a high-speed source follower build with JFET transistor Q1 was used. The total input bias current of the composite amplifier is below 100 pA and its influence on the gain coefficient may be neglected.

4. GAIN SWITCHING

The amplifier has 5 fixed gain coefficients: -1; -2; -4; -6 and -10 V/V. The gain switching is shown in Fig.5. Five relays are used to switch on one of 5 resistors at the inverting input of the amplifier. Additional relay contacts switch the compensation capacitors $C_{F,n}$ parallel to the resistor R_F in the feedback loop. To minimize the thermoelectric effects in the relay contacts due to heat developed in the relay coil the bistable, two-coil relays are used. The relay coils are activated only for approximately 10 ms, therefore the heat developed in the coils is very small. To avoid excessive voltage transients at the amplifier output during gain switching, the relay coils are controlled by especially developed programmable logic device (PLD) chip. This is an advantage when using the amplifier in the ac-dc calibration system with thermal converters, because it reduces the temperature change of the TC heater due to switching. The second function of the PLD is to translate the 8-bit command and execute an appropriate switching sequence. The third function of the PLD is to reset all relays after powering on the amplifier or during power supply failure. To accomplish these functions a local power supply reset circuit was used. It generates the reset signal to the PLD chip in case the supply voltage is to low. The another reset signal comes from the main controller. It is able to detect the mains failure and to perform the reset using the energy accumulated in the power supply filter capacitors. The PLD senses the state of the outguard power supply. In case of a voltage drop or failure a power on state reset is performed. This was implemented to avoid overheating of the inguard section because the fans are supplied from the unregulated outguard power supply.

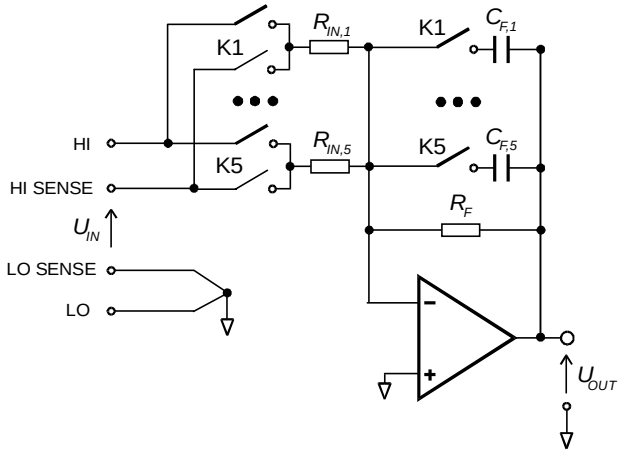

Fig.5. Gain switching (only two gain resistors are shown)

5. INPUT AND OUTPUT CONNECTIONS

To reduce the influence of cable- and connector impedances either the input like the output connections are realized using four-wire technique. This is important especially because of the relatively low input impedance of the amplifier. The input wiring is shown in Fig.5.

The design of the output sensing circuit is more complicated. Without any precautions there would be an essential error due to the current flowing in the feedback resistance R_F (or sense high wire) and through the sense low wire (Fig.6).

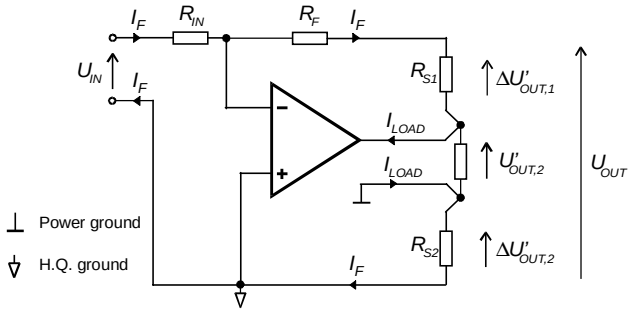

Fig.6. Gain error due to current I_F flowing in the sense paths

To reduce these errors a negative impedance converter (NIC) build with U6 was used to remove the current from the sense high path (Fig.7) [6]. The NIC delivers a current to the point SNSHI which cancels the feedback current I_F. The cancellation circuit reduces the sense high current below 50 μA at 1 kHz. For lower frequencies or dc the compensation is even more effective. The NIC injects a current to the signal ground through the resistors R (Fig.7). This current flowing through the sense low wire is the source of an additional error. To cancel this current an additional circuit with U7 was used. It sinks the current from R and returns it to the power supply.

The operator can configure the output sensing circuit of the amplifier in a local- or remote mode. In case of the local sensing mode the output voltage is sensed directly onto the output binding posts. The remote mode of sensing is useful when is impossible to connected the load directly to the output binding posts of the amplifier.

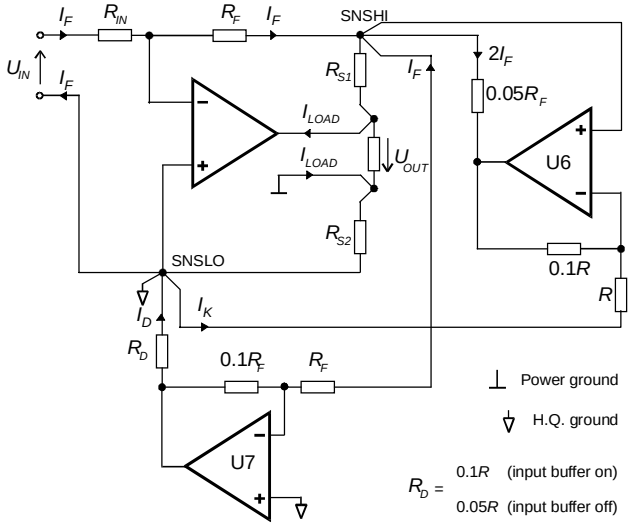

Fig.7. Sense current cancellation circuit

6. INPUT BUFFER

An input buffer is provided in case when the DSS connected to the amplifier input has no four-wire output. The input impedance of the buffer is fixed at 10 MΩ. A fast-settling and precision operational amplifier in hermetic enclosure (to increase long-term stability) was selected to be used in the input buffer. However, using the buffer degrades the dc performance of the amplifier. The input buffer can be switched on or off by the selected remote interface or with the keyboard. The input of the buffer is overvoltage protected.

7. GUARD, ASSEMBLY AND POWER SUPPLIES

To separate the amplifier from the digital circuits connected with line ground the whole analog circuitry was put into the internal metal enclosure called “guard”. The guard is electrically isolated from the main enclosure. A separate binding post electrically connected with the guard is provided at the front panel. The analog (or inguard section) is electrically isolated from the digital (or outguard) one. This electrical separation was easy because the digital section controls only the relay coils, electrically separated from the relay contacts. However, the pcb traces to the relay coils enter into the guard and increase the capacitive coupling between the inguard and outguard section. Therefore a separate power supply located in the guard was provided to control the relay coils. The both digital circuits: inguard and outguard are optically separated by means of optocouplers located at the edge of the guard assembly.

The analog part of the amplifier is supplied from ± 100 V and ± 17 V power supplies. These both supplies are located in the guard assembly. Because they develop a substantial amount of heat the force cooling has to be implemented inside the guard. To protect the sensitive input circuitry from the heat flow and associated thermal gradients a thermal shield was provided inside the guard. The shield physically separates the input section of the amplifier from the hot output section.

The all ac voltages necessary to supply the amp are provided by a triple-shielded toroidal transformer. The system of its internal shields provide ultimate separation between inguard and outguard sections and reduces the common-mode currents.

8. PROTECTION CIRCUITS

There are three overcurrent protection methods implemented. The first protection system is based on a power supply with foldback current limiting characteristic. In case of an short or overload at the output, the supply current is cut to about 120 mA. The power stage of the hybrid amplifier is additionally protected by means of a simple current limiter. It starts its limiting action at approximately 100 mA. The third protection is provided by slow-blow fuses in the secondary windings of the power supply transformer. These fuses protect the expensive toroidal transformer from damage in case of a power supply failure as well. The output of the amplifier has overvoltage protection. Diodes limit the voltage applied accidentally to the amplifier output to approximately ±80 V.

9. MAIN CONTROLLER, INTERFACES AND KEYBOARD

The main controller was built around 8051 series microcontroller. It features the power-down mode in which the clock oscillator is stopped and no clock noise is generated. The microcontroller can be waked up from the power down mode by an external interrupt caused by GPIB, RS-232 or keyboard event. After performing the appropriate action (for example gain switching) the microcontroller goes back to the power-down mode. To further minimize the noise the charge pump of the RS-232 interface is switched off when the serial interface is not selected or no serial transmission is performed.

The amplifier is controlled by GPIB, RS-232 interfaces and by a simple keyboard. A custom asynchronous GPIB controller implemented in PLD was developed [7]. The asynchronous design of the GPIB controller eliminates the clock noise.

10. FEATURES

A model of the amp was built and tested. The gain error in the 0… 1kHz frequency range is not greater than 0.01% and is determined mainly by the tolerance of the resistors. The full power 3 dB bandwidth and the slew rate of the output voltage is approximately 0.6 MHz and 100 V/μs, respectively . The maximum output current is 50 mA (rms value of the sinusoidal signal). The maximum offset dc voltage at the output depends on the voltage gain and is lower than 30 μV with the input buffer switched off. Fig.8 shows the step response of the amplifier for pure resistive load of 1.2 kΩ and 50 mA rms output current.

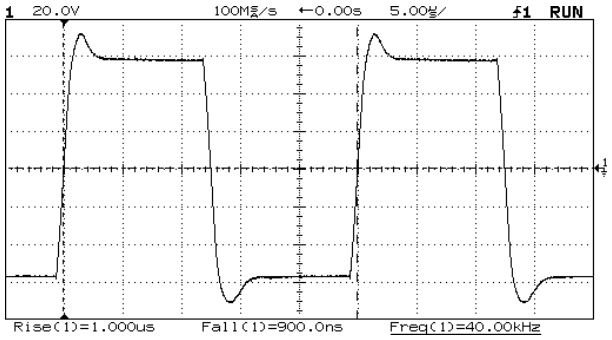

Fig.8. Step response of the amplifier for pure resistive load of 1.2 kΩ and 50 mA rms output current

The wideband noise measured at the output in 20 Hz… 10 MHz frequency range is below 3 mV.

The flatness of the gain vs. frequency characteristics was not measured. However, simulations show that ±1 ppm flatness is achievable in the dc to 1 kHz frequency range.

11. CONCLUSIONS AND PROSPECTS

The physical model of the amplifier is now tested in the German National Measurement Laboratory and will be a part of the calibration system for evaluation of low-frequency thermal converters used in ac-dc transfer. It can be, however, useful in other applications. For example it can increase the output voltage, current and power of function or arbitrary generators in the 0… 100 kHz frequency range. In the 0… 1kHz range, the four-wire output connections reduce the influence of the load resistance on the output voltage.

A 220 V ac/dc range amplifier for a low-frequency voltage calibrator is currently worked out basing on the described amplifier. Its maximal peak output voltage is ±320 V and the output current will be enough for performing ac-dc calibrations with thermal converters.

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