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CHARGE INJECTION PHENOMENA IN THE S^{2}I CELL APPLIED TO SECOND ORDER SIGMA DELTA MODULATOR

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Abstract: In this paper we present a method for the modelisation of charge injection phenomena in sigma-delta modulators before implementation using switched current S^{2}I techniques. Our study is focused on charge injection error modeling in MOS switches through a two steps sampling of memory cell modelled by MATLAB Software.

Keywords: SD Modulator, Switched current technique ,modelling.

1 INTRODUCTION

There is currently considerable interest in the application of switched-current (SI) techniques, specially, to the design of analogue sampled-data filters and data converters. However, charge injection has remained as a significant error in SI circuits due to its inherently signal dependent feature. Therefore, the use of two step switched current technique allows to reduce the charge injection. Besides, we propose, in this paper, a method for the theoretical calculations of the current error introduced by transistor imperfection in switched current memory S^{2}I cell. Simulation results exhibit that the proposed method gives the effect of charge injection and achieves excellent estimation of the behavior of the sigma delta modulator before implementation.

2 BASIC S^{2}I MEMORY CELL

The basic S^{2}I memory cell [1]-[3], shown in figure 1, achieves error cancellation through a two step sampling process. During the first coarse step (Φ_{1a}) the signal is sampled by the NMOS (M_{mn}) memory transistor and during the second fine step (Φ_{1b}), the error is sampled and stored in the PMOS (M_{mp}) memory transistor. On the output phase (Φ_{2i}) the output signal is derived from both memories to achieve a large degree of error cancellation . All types of error are reduced : output conductance errors from the memory transistor's drain conductance and drain–gate feedback capacitance's are reduced because the cell generates a virtual earth (V_{ref}) at its sampling instant (end of Φ_{1b}). The charge injection errors are limited due to the secondary sampling process diminishes the signal dependence of the error.

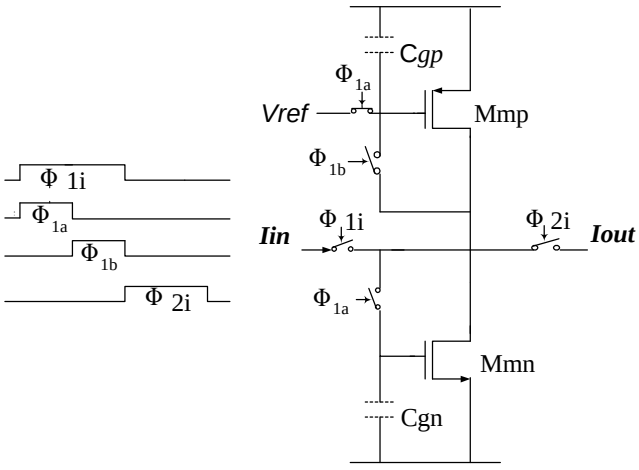

Figure 1. two step cell and clock wave.

3 CHARGE INJECTION MODELLING IN S^2I CELL

A switched current memory cell S^2I perform the function of a current copier, and it is ideally modeled by a delay line of a half clock period. The charge injection error is induced in the output current of a memory cell because the MOS transistor is used as a switch [2]. During the first coarse step Φ_{1a}, the gate voltage of the switch transistor T1 is set to V_H (High voltage of the clock signal). Therefore a charge Q_i is stored in its channel capacitance and the quantity of this charge depends on V_H and the gate voltage of the NMOS memory transistor. When the switch transistor is turned off a great part of this charge is injected in the gate sources capacitance of the memory transistor (figure 2), induced an error on the drain current ($I_d = I_e + \Delta_{inj}$), where Δ_{inj} is the error injection current in the phase Φ_{1a}, given by equation (1).

$$\Delta I_{inj} = \frac{K_n}{2}\left(\frac{W}{L}\right)V_{inj}^{\ 2} + K_n\left(\frac{W}{L}\right)_{M,n}\left(V_{GSM,n} - V_{T,M}\right)V_{inj} \tag{1}$$

Where kn, is the Boltzman constant, (W/L) the aspect ratio of memory transistor M_{mn}. The expression of V_{GSM} is:

$$V_{GS,M} = \sqrt{\frac{Ip + I_e}{K_n\left(\frac{W}{L}\right)_{M,n}}} + V_{T,M} \tag{2}$$

Where Ip is the bias current of memory transistor and Ie is the input current of memory cell S^2I. Or V_{inj} is a voltage error of the gate potential of the memory transistor M_{mn} is given by :
where C_{ch} and C_{ol} are respectively the channel capacitance and gate overlapping capacitance of the

$$V_{inj} = \frac{C_{ch}\left(V_h - V_g - V_t\right) + C_{ol}\left(V_g + V_t - V_l\right)}{C_{gs}} \tag{3}$$

switch transistor. Vg is the gate voltage of the memory transistor and V_t is the threshold voltage of the switch transistor T_1. V_h and V_l are high and low voltage of the clock signal.

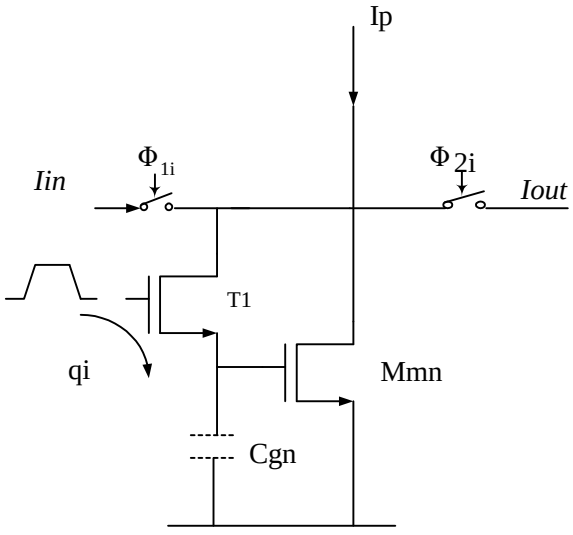

Figure 2. S^2I memory behaviour during the first (coarse) step.

During the second fine step Φ_{1b}, the gate potential of the switch transistor T_2 is forced to V_L (low voltage of the clock signal). Consequently a charge Q_{i1} is stored in its channel capacitance and the amount of this charge depends on V_L and the gate voltage of the memory transistor M_{mp} when the

switch transistor is turned off a great portion of this charge is injected in the gate source capacitance of the second memory transistor M_{mp} (figure 3)[4].
It introduces a voltage error on the gate potential of memory transistor M_{mp} given by expression (4) causing an error on the output current.

$$V_{inj1} = \frac{C_{ch}\left(V_{dd} - V_b - V_{g1} - V_{t1}\right) + C_{ol}\left(V_{g1} + V_{t1} + V_h - V_{dd}\right)}{C_{gs}} \tag{4}$$

The term of this output current error is given by (5) where C_{ch} and C_{col} are respectively the channel capacitance and gate overlapping capacitance of the second switch transistor T_2,V_{g1} is the gate of the M_{mp} transistor and V_{t1} is the threshold voltage of the second switch.

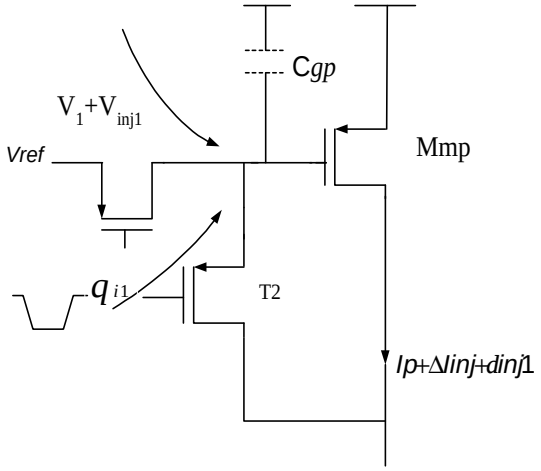

Figure 3. S^2I memory behaviour during the second (fine) step.

$$dI_{inj1} = \frac{K_P}{2}\left(\frac{W}{L}\right)V^2{}_{inj1} + K_p\left(\frac{W}{L}\right)_P\left(V_{SG,p} - \left|V_{T,p}\right|\right).V_{inj1} \tag{5}$$

Where the Kp is the Boltzman constant of M_{mp} and (W/L) the aspect ratio of memory transistor M_{mp}. The expression $V_{SG,p}$ and $V_{T,P}$ are respectively the gate to source and threshold voltages of memory transistor M_{mp}.

$$V_{SG,p} = \sqrt{\frac{I_P + \Delta I_{Iinj}}{K_P\left(\frac{W}{L}\right)_P}} + \left|V_{T,p}\right| \tag{6}$$

When we combine equation (1), (2), (3), (4) and (5), its results on an expression of the current error δI_{inj1} (µA) which will be equal to :

$$\delta I_{inj1} = ß_4 Ie^4 + ß_3 Ie^3 + ß_2 Ie^2 + ß_1 Ie + ß_0 \tag{7}$$

The calculus of these terms by Maple Software gives the values presented by table 1.

$ß_4$	$0.1156978662\ 10^{-6}$ (µA-3)
$ß_3$	$0.4819825862\ 10^{-6}$ (µA-2)
$ß_2$	$0.4584637184\ 10^{-2}$ (µA-1)
$ß_1$	$0.9548461946\ 10^{-2}$
$ß_0$	0.03400325401 (µA)

Table 1. Calculated values by MAPLE.

These estimated parameters ($ß_4$, $ß_3$, $ß_2$, $ß_1$ and $ß_0$) depend on bias current Ip and transistor parameter's of cell memory S^2I. Therefore the simply delay line of the two step memory cell is replaced by the model given in figure 4.

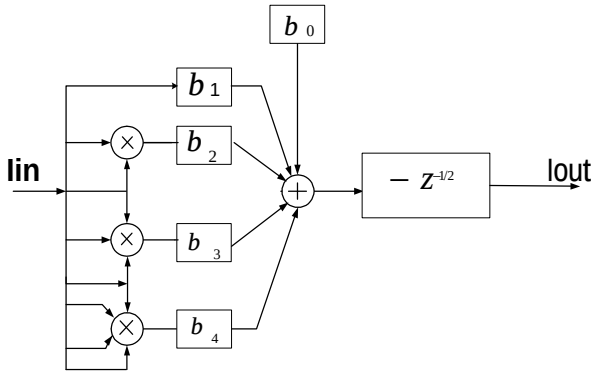

Figure 4 : Switched current memory cell two step model.

This model is used to study the behavior of second order Sigma-Delta modulator under MATLAB software.

4 BEHAVIOR OF SECOND ORDER SIGMA DELTA MODULATOR USING THE PROPOSED MODEL

The switched current integrator is the main block of the low-pass Sigma-Delta modulator. The functionality of the modulator depends on the integrator's performances. It is formed by two cell memory in cascade, then feeding back the output current of second cell to the input. A good modelling of integrator permits to detect the behavior of the Sigma Delta modulator. Second order switched current Sigma Delta modulator which simplified model is depicted in figure 5.

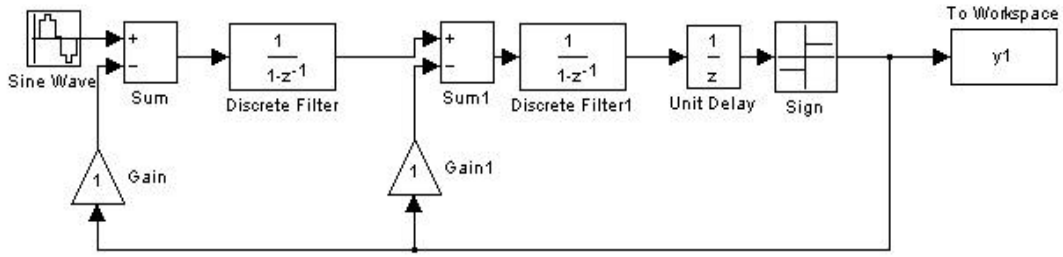

Figure. 5 Second order Sigma Delta Modulator.

This model allows an ideal behavioral analysis of the modulator. It is simulated for the following characteristics :

Sampling frequency	1.024Mhz
Signal frequency	1khz
Band frequency	8khz
Over Sampling Ratio	64
FFT	32768

Table 2. Main characteristics of simulated modulator.

The power spectrum of the output modulator is observed in figure 6. This spectrum shows that the noise slope level noise is 60 dB, which correspond to the characteristics of a second order modulator having 12 bit as resolution.

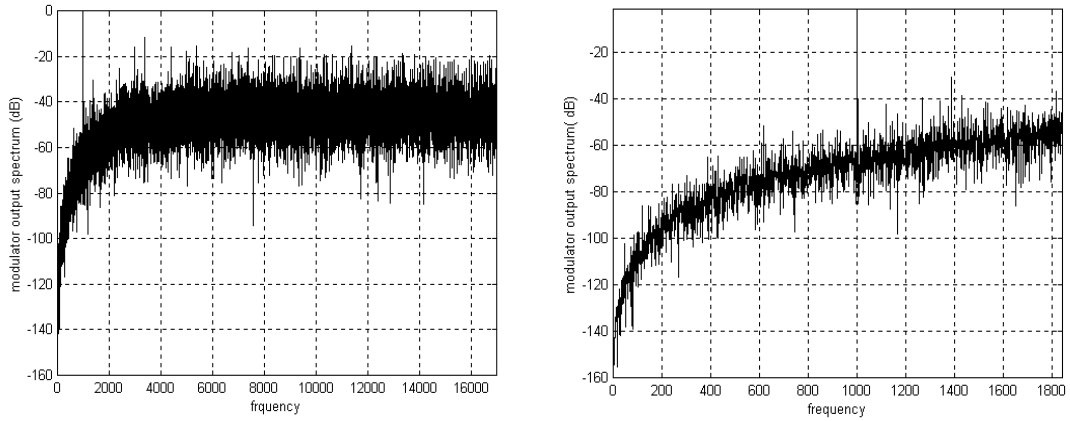

Figure 6. Ideal output spectrum of the modulator in nyquist and audio band.

Shown in figure 7 is the output spectrum of the sigma delta modulator using the proposed architecture for memory cell S^2I (figure 4). Therefore, this spectrum explained the influence of both linear and non linear components. The result proof a high rise of noise level and harmonic distortion .

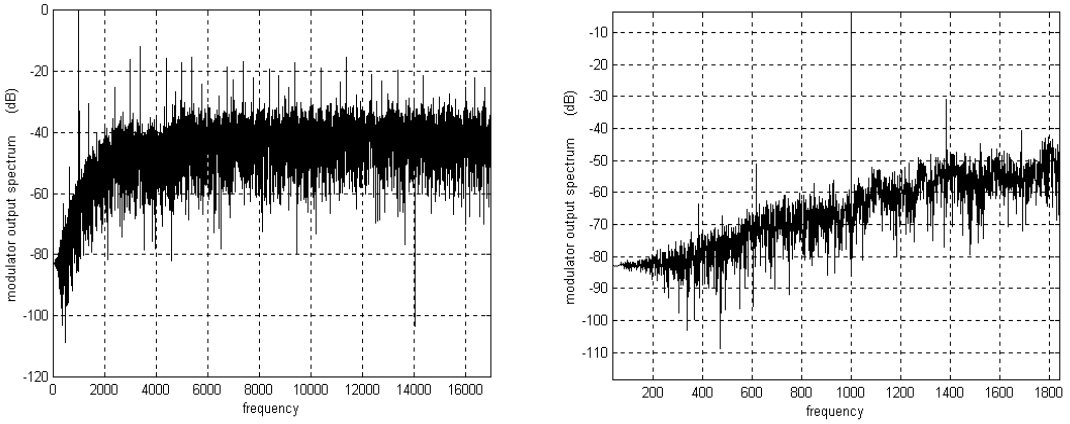

Figure 7. Output spectrum of the proposed model in nyquist and audio band.

One way to make these two components separated is to study the effect for each component on the output spectrum. Hence, the simulation results shows in figure 8 that the linear component has not a big effect on the output spectrum. However, non linear component in figure 9 is the principal cause of modulator distortions.

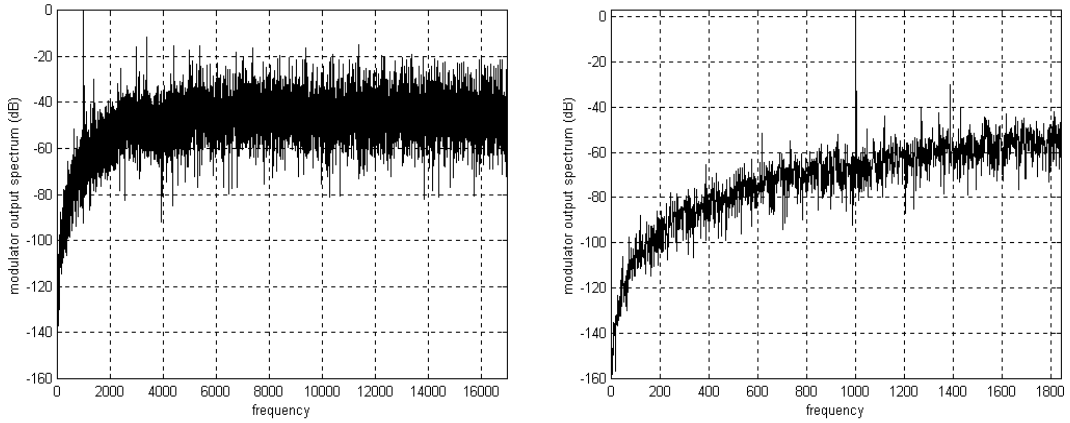

Figure 8 . Modulator output spectrum with only linear component.

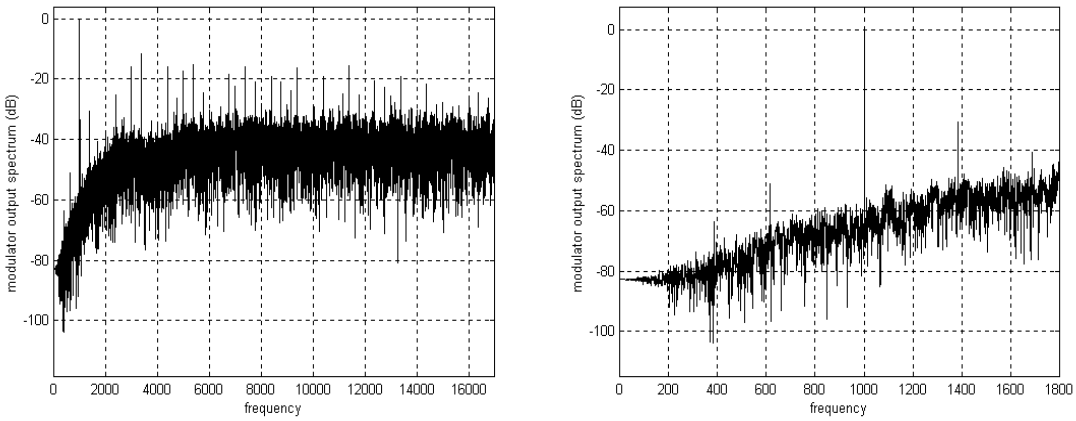

Figure 9. Modulator output spectrum with only non linear component.

Then, we conclude that to decrease the charge injection effect on Sigma Delta modulator based on S^2I memory cell is recommended to cancel non linear component. A S^2I switched current cell which has been described achieves greater reduction of charge injection error with little increase in complexity then the basic memory cell.

5 CONCLUSION

A charge injection modelling is presented in order to simulate Second order Sigma-Delta modulator. This phenomena has a big effect on the modulator output performance, however using S^2I technique this phenomena is reduced but is not canceled. In fact, this phenomena remains the most problem of the switched current techniques. The used method is an efficient way to analyze the behavior of the sigma delta modulator before implementation. In addition, other serious problem of the switched current technique is solved, while limiting an excessive time for simulation needed for the complex switched current circuit.

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