

# THE POSSIBILITY OF IMPLEMENTING A NONLINEAR SUCCESSIVE APPROXIMATION A/D CONVERTER USING FPGAs

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*Abstract: This paper presents our study regarding the possibility to implement an analog to digital converter with the following capabilities: bipolar and linear analog to digital conversion with 8/12 bits resolution, bipolar non-linear (logarithmic) analog to digital converter with variable resolution 6, 12 bits, bipolar and linear or non-linear analog to digital converter, depending on the measuring range. The main circuit of the converter is an FPGA (Field Programmable Gate Array). The converter has been tested using 500 kHz and 1MHz clock. The errors obtained with this converter were less than  $\pm 1$  LSB.*

*Keywords: nonlinear ADC, field programmable gate array (FPGA), measurement errors*

## 1 INTRODUCTION

FPGAs have gained a great popularity in the area of digital design because they permit, at a low cost, the rapid prototyping of digital circuits. The possibility to realize a non-linear (logarithmic) bipolar successive approximation ADC was presented in [1]. The bipolar and logarithmic characteristic was approximated by means of 13 segments (A-law) which were stored, point by point in an EPROM (in the EPROM is stored the characteristic only for the positive polarity of the measured voltage). This kind of converters can also be built by using specialized DACs [2,3]. The advantages of the converter described in [1] are: the possibility to modify the non-linear characteristic (useful when implementing the nonlinear characteristic of transducers), low capacity memory usage, the possibility to switch to a linear operation mode. In [4] it is presented the realization of a linear ADC (plus other features) using a Xilinx XC4010XL FPGA. In this paper we present a logarithmic ADC (plus other features) implemented using a Xilinx XC4010XL FPGA. In this case, the non-linearity also is implemented in the FPGA.

## 2 FUNCTIONAL BLOCK DESCRIPTION

The functional block diagram is presented in Figure 1.

The converter has two main parts: the digital part (implemented using the FPGA) and the analogous part. The blocks Sign Detector & Comparators, the successive approximation register SAR812 (8/12 bit), the multiplying DAC (12 bit resolution) and the reference voltage  $V_{ref}$  ( $\pm 4.096$  V) constitute a classic bipolar successive approximation ADC with 8-bit or 12-bit resolution. The non-linearity is implemented in the block NELIN. The multiplexer MUX 2:1 selects one of the following outputs: from the SAR812 (the converter operates as a linear ADC with 8/12-bit resolution) or from the NELIN (the converter operates as nonlinear ADC with a variable 6 to 12-bit resolution). The outputs DOUT [11,0] give the conversion result in binary code to which is attached the sign bit SIGN. The end of conversion is indicated by the signal EOC. The circuit allows the dynamic display of the conversion result by using four seven-segment LED displays. This is done by the following blocks: the binary to BCD block (BIN12BCD), the 4 to 1 multiplexer (MUX44), the decoder BCD to seven-segments (LEDDCD), the divisor by 4 ( $\div$ ) which generates the selection signals for MUX44, the decoder 2 to 4 (DECODER 2:4) which generates the multiplexing signals (units (U), tenths (T), hundreds (H), thousands (TH)) for the 4 seven-segment displays. The end of conversion from binary to BCD is indicated by signal E. It is obvious that the outputs of block BIN12BCD (four digits) can be connected to the external terminals of the XC4010XL chip so they can be used as the result of the BCD conversion. The clock frequencies necessary for different blocks of the converter are generated using the internal oscillator OSC4 available on the XC4010XL chip as follows: 500 kHz for the SAR block, 8 MHz for BINBCD block and 490 Hz for the displaying section.

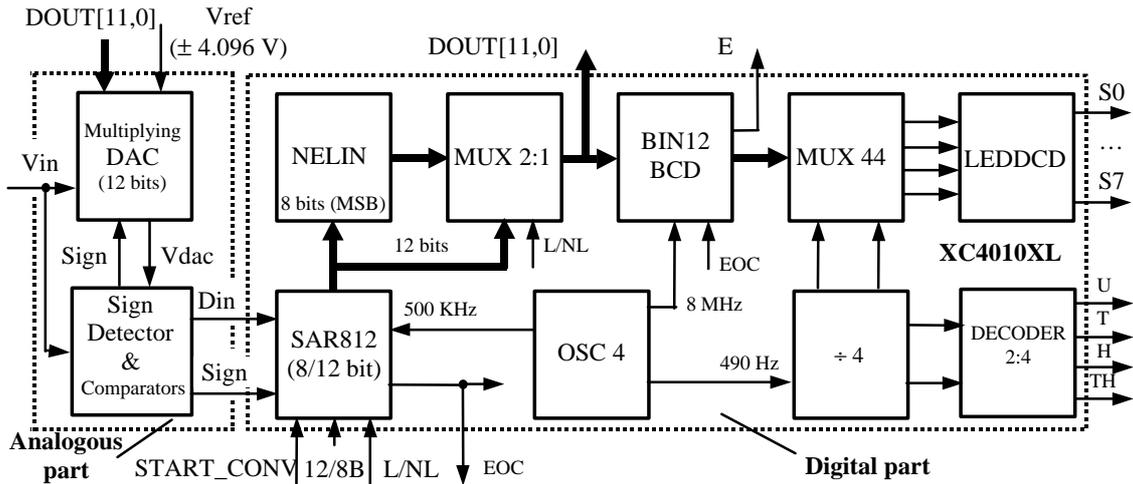


Figure 1. The functional block diagram.

This circuit allows the following operation modes:

- linear and bipolar 8-bit resolution ADC (conversion time is 8 clock SAR pulses);
- linear and bipolar 12-bit resolution ADC (conversion time is 12 clock SAR pulses);
- logarithmic and bipolar ADC with variable (6 to 12-bit) resolution (conversion time is 8 clock SAR pulses);
- the possibility for automatic switching between operation modes (nonlinear (logarithmic) ADC/linear ADC) related to the input signal level  $V_{in}$ . In this way it can be avoided the loose of resolution for high levels of the input signal  $V_{in}$ . The voltage threshold that triggers the change of operation mode can be provided by a comparator ( $V_{in}$  is compared with the threshold voltage) whose output directly activates the input L/NL (linear/nonlinear). The conversion time is 8 clock SAR pulses for nonlinear operation and 8/12 clock SAR pulses for linear operation;
- the display of conversion results.

The selection of the resolution and operation modes is made by using the inputs 12/8B and L/NL. The start of conversion is triggered by the rising-edge of the START\_CONV signal.

### 3 FUNCTIONAL DIGITAL PART DESCRIPTION

The schematic for the digital part of the converter, implemented in the XC4010XL circuit is presented in Figure 2. The digital part of the converter was realized using the design tools of Xilinx Foundation V1.5i, i.e. the Schematic Editor and the HDL editors (Abel and VHDL).

The SAR812 is a 12-bit successive approximation register. At the input SLI it is applied the signal DIN (the output of the comparator of a classic successive approximation analog to digital converter) exor-ed with signal SIGN (the signal that indicates the polarity of the measured voltage  $V_{in}$ ). For voltage  $V_{in} < 0$ , SIGN=1 so, the input SLI receives the signal  $\overline{DIN}$ . This ensures the correct operation of block SAR812 for both positive and negative  $V_{in}$  voltages. The clock signal, applied to input C, can be generated internally by the oscillator OSC4 existent on the chip. The internal oscillator OSC4 generates five frequencies: 15Hz, 490Hz, 16kHz, 500kHz and 8MHz. In our schematic we used the 500kHz frequency (obviously we can divide the 8MHz frequency to obtain other frequency clocks). The use of an external clock is available by means of input CK selectable using the CKSEL input of the M2\_1 multiplexer. The start of conversion signal is applied to input CLR and the conversion starts with the rising edge of START\_CONV signal; the rising edge is synchronized with the clock (U11,U12). The conversion takes 8 or 12 clock cycles. The end of conversion is realized by signal EOC applied to input CE. The EOC becomes active at the beginning of clock cycle 9 or 13. The selection is made using signals 12B and LIN\_NELIN. When LIN\_NELIN=1 (linear operation) and 12B=1 the conversion takes 12 clock pulses where as for 12B=0 the conversion takes only 8 clock pulses. When LIN\_NELIN=0 (non-linear operation) the conversion takes 8 clock pulses.

The block SAR812 has 12 outputs, P[11,0] which feed multiplexer L1. In the case of linear operation and 8 bits conversion, at the beginning of the 9<sup>th</sup> cycle, the output P3 is logic active. This output must be cleared which is done by and-ing it with signal 12B·LIN\_NELIN.

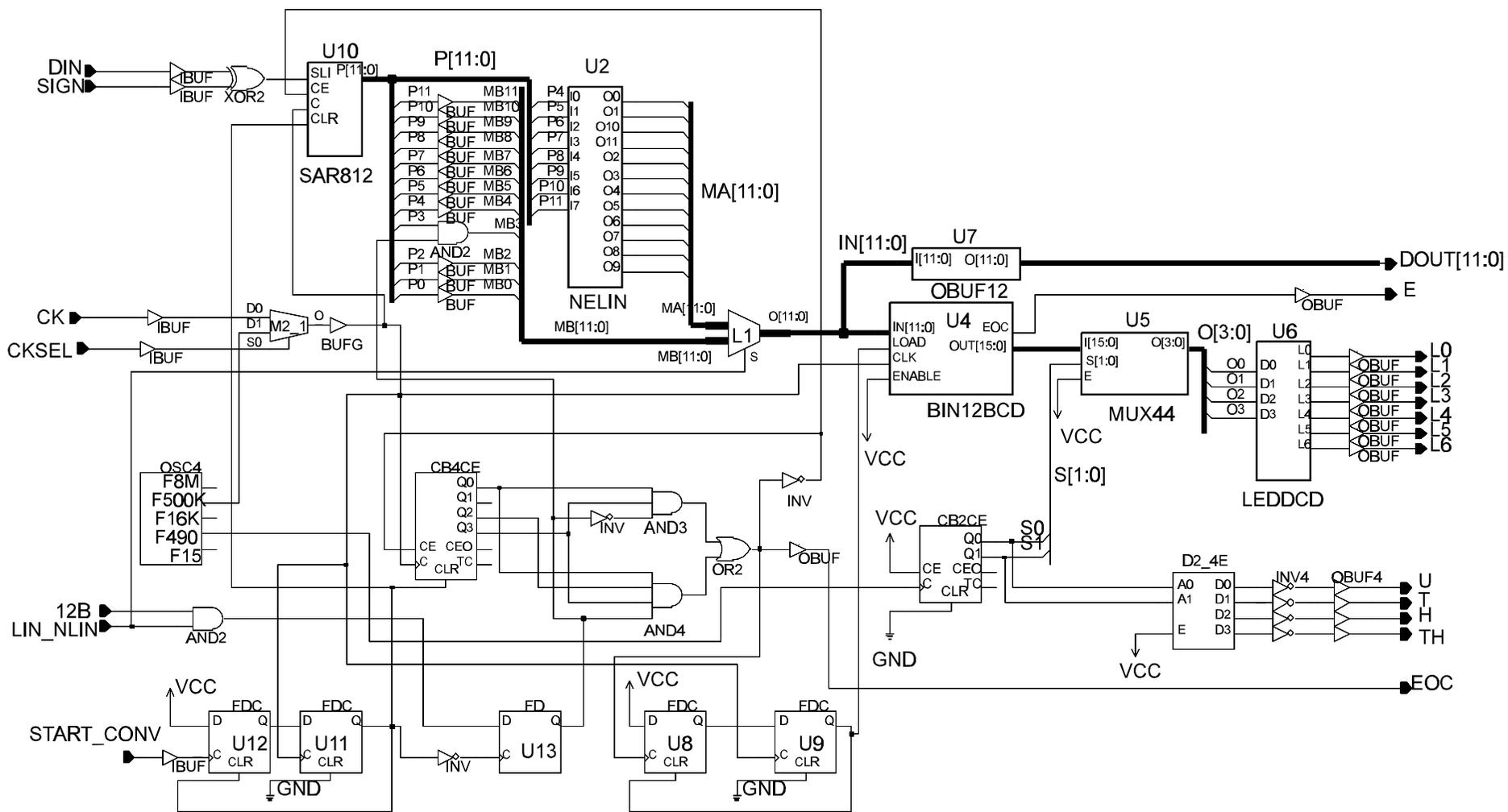


Figure 2. The digital part schematic.

The non-linear characteristic, i.e. the positive branch of the bipolar logarithmic curve approximated using 13 segments, is stored in NELIN block. The positive branch consists of 7 segments (the segment intersecting the origin is common for both positive and negative branches). At the inputs of NELIN block we apply the outputs P[11,4] of SAR812 (the 8 most significant outputs). The linearized characteristic is stored using  $2^8=256$  points. To each segment we allocate  $256/8=32$  points (to the origin segment is considered double and we allocate 64 points). The storing resolution for the linearized characteristic is different for each segment: 12 bits for the first segment, 11 for the second segment, ending with 6 bits for the last segment. The NELIN block was designed as a combinational circuit. The implementation of NELIN block is given in Figure 3.

```

module nelin
Title 'nelin'

Declarations

i7..i0 PIN;
i = [i7..i0];
o11..o0 PIN istype 'com';
o = [o11..o0];

Equations

TRUTH_TABLE

(i -> [o11,o10,o9,o8,o7,o6,o5,o4,o3,o2,o1,o0])
"segment 1 resolution 12 bits
0->[0,0,0,0,0,0,0,0,0,0,0,0];
1->[0,0,0,0,0,0,0,0,0,0,0,1];
2->[0,0,0,0,0,0,0,0,0,0,1,0];
:
62->[0,0,0,0,0,0,1,1,1,1,1,0];
63->[0,0,0,0,0,0,1,1,1,1,1,1];
"segment 2 resolution 11 bits
64->[0,0,0,0,0,1,0,0,0,0,0,1];
65->[0,0,0,0,0,1,0,0,0,0,1,1];
:
94->[0,0,0,0,0,1,1,1,1,1,0,1];
95->[0,0,0,0,0,1,1,1,1,1,1,1];
"segment 3 resolution 10 bits
96->[0,0,0,0,1,0,0,0,0,0,1,1];
97->[0,0,0,0,1,0,0,0,0,1,1,1];
:
126->[0,0,0,0,1,1,1,1,1,0,1,1];
127->[0,0,0,0,1,1,1,1,1,1,1,1];

"segment 4 resolution 9 bits
128->[0,0,0,1,0,0,0,0,0,1,1,1];
129->[0,0,0,1,0,0,0,0,1,1,1,1];
:
158->[0,0,0,1,1,1,1,1,0,1,1,1];
159->[0,0,0,1,1,1,1,1,1,1,1,1];
"segment 5 resolution 8 bits
160->[0,0,1,0,0,0,0,0,1,1,1,1];
161->[0,0,1,0,0,0,0,1,1,1,1,1];
:
190->[0,0,1,1,1,1,1,0,1,1,1,1];
191->[0,0,1,1,1,1,1,1,1,1,1,1];
"segment 6 resolution 7 bits
192->[0,1,0,0,0,0,0,1,1,1,1,1];
193->[0,1,0,0,0,0,1,1,1,1,1,1];
:
222->[0,1,1,1,1,1,0,1,1,1,1,1];
223->[0,1,1,1,1,1,1,1,1,1,1,1];
"segment 7 resolution 6 bits
224->[1,0,0,0,0,0,1,1,1,1,1,1];
225->[1,0,0,0,0,1,1,1,1,1,1,1];
:
254->[1,1,1,1,1,0,1,1,1,1,1,1];
255->[1,1,1,1,1,1,1,1,1,1,1,1];
end nelin

```

**Figure 3.** Implementation of the NELIN block.

The NELIN block outputs, MA[11,0] are input to multiplexer L1. Using this multiplexer, we select either the output of block SAR812 (linear operation) or the outputs of block NELIN (non-linear operation). The selection is done using signal LIN\_NELIN. The outputs of multiplexer L1 are connected to the output terminals of the chip DOUT[10,0] as they output the result of the conversion. These terminals are connected to a 12-bits multiplying digital to analog converter whose reference voltage is  $\pm 4,096V$ . The polarity of the reference voltage is selected using signal SIGN. In the case of linear operation the quantification step is  $\pm 1$  mV (12 bits resolution) whereas for the nonlinear operation the quantification step is between  $\pm 1$  mV and  $\pm 64$  mV.

The lost in resolution for the nonlinear operation for high levels of voltage  $V_{in}$  can be avoid if the LIN\_NELIN signal is the output of a voltage comparator. To the (+) input of the comparator we apply the  $V_{in}$  voltage whereas to the (-) input of the comparator we apply the threshold voltage over which the linear operation is desired (the 12B signal is used to select the resolution for the linear operation).

In the case of nonlinear operation, at the end of conversion, when LIN\_NELIN=1 at the outputs DOUT[11,0] we get the content of SAR812 which represent the logarithm of voltage  $V_{in}$ .

The proposed schematic, allows the display of conversion results using four digits by means of four 7segment displays. The conversion result is converted in decimal (4 digits) using block BIN12BCD. The BIN12BCD consists of a binary counter that at the end of conversion is loaded with the conversion result in binary code. Using the 8MHz clock, the content of the counter is downloaded into a decimal counter. At the end of transfer indicated by signal E, the content of the decimal counter represents the conversion result in decimal code.

The four decimal digits are selected one by one by means of multiplexer MUX44. The conversion from decimal to 7 segments is realized by the LEDDCD block. The control of the anodes of the seven segments is realized with signals S7-S0. The control of selection inputs S[1,0] of multiplexer MUX44 is realized by means of a divisor by 4. Signals U(units), T(tenths), H(hundreds) and TH(thousands), active low, control the common cathodes of the four 7 segments displays. These signals are created using a 2:4 decoder. The display system (MUX44, LEDDCD, divisor by 4, 2:4 decoder) is synchronized with the 490Hz clock.

#### 4 EXPERIMENTAL RESULTS AND CONCLUSIONS

The proposed ADC was implemented using the followings: Xess board XS40-010XL (contains a Xilinx XC4010XL FPGA), Foundation V1.5i software, an 12 bit multiplying DAC, reference voltage  $V_{ref} = \pm 4.096V$ , 3 clock signals (a 500 kHz clock for the SAR812, an 8 MHz clock for the BINBCD block and a 490 Hz clock for the displaying section of the circuit). All three clocks are generated using the internal oscillator (OSC4) of the FPGA chip.

The converter operation was tested also using an 1MHz external clock (for the SAR812 block). The measuring errors that have been obtained are bellow  $\pm 1$  LSB corresponding to measuring resolution.

The amount of FPGA resources that have been used in the implementation of the proposed ADC is about 25 %. The maximum input-output delay of the digital part is about 30 ns which indicates the possibility of the ADC to work at a clock frequency of at least 30 MHz. The limitation of the clock frequency is given by the analogous part of the ADC.

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