XVI IMEKO World Congress
Measurement - Supports Science - Improves Technology - Protects Environment ... and Provides Employment - Now and in the Future
Vienna, AUSTRIA, 2000, September 25-28

POSSIBILITIES TO IMPROVE THE MEASURING PERFORMANCES OF IMPEDANCES IN A WIDE FREQUENCY RANGE

L. Breniuc, M. Cretu and L. Nita
Department of Electrical Measurements and Electrical Materials
Faculty of Electrical Engineering
Technical University "Gh. Asachi" of Iasi, RO-6600 Iasi, Romania

Abstract: This paper presents our study regarding the possibility of using the non-linear conversion to measure impedances in a wide range of frequencies. In this case, impedance testing is done by using a multi-frequency signal with the crest factor as low as possible. The non-linear conversion (logarithmic) has as effect measurement error reduction for low levels contained in the measurement signal. From this point of view, non-linear conversion apear to be an alternative to the problem of minimization of the crest factor of the test signal.

Keywords: impedance measurement, nonlinear conversion, Fourier transform, measuring errors

1 INTRODUCTION

Usually, impedances are measured at a fixed frequency. Impedance measurement for another frequency implies the modification of the frequency of the test generator. From this point of view, the measurement is done serially. The draw back of this method is the long time of measurement process. A possibility of measuring the impedance in a wide range of frequencies is indicated in [1]. The block diagram of the measuring circuit is given in Figure 1.

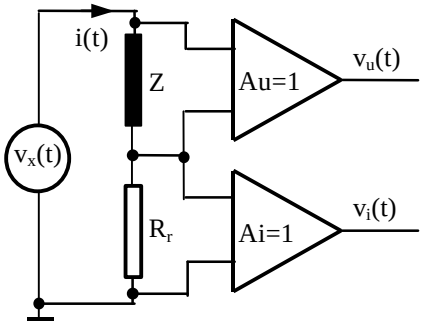

Figure 1. Block diagram of the measuring circuit.

In this picture, $v_x(t)$ is the test voltage, Z=R+jX is the unknown impedance (test impedance), R_r is a reference resistor which converts the current i(t) into voltage, A_u and A_i are two differential amplifiers. Testing impedances in a wide range of frequencies implies the use of a test voltage that should contain all the frequencies in the given range. The conditions imposed to the test voltage are: all frequencies in the range must have same amplitude, the crest factor of voltage $v_x(t)$ must be as small as possible. For a voltage v(t), the crest factor CF is defined with relation (1).

$$CF = \frac{V_{max} - V_{min}}{2V_{rms}} \tag{1}$$

In relation (1), V_{max}, V_{min}, V_{rms} represent the maximum, minimum and effective value of a voltage v(t), respectively.

There are several methods to minimize the crest factor. The solution in [1] is based on the idea of selecting initial phases for the frequencies in the range in a similar way the successive approximations are done. Thus, for the voltage $v_x(t)$ consisting of fundamental f and the first 25 odd and prime harmonics (the range f÷101f), using this method, we obtain a crest factor equal to 1.867. In this case, the voltage $v_x(t)$ is expressed with the relation (2).

$$v_x(t) = \sum_{i=1}^{i=26} \frac{1}{k \cdot A} \sin(2p\, f_i + j_i) \tag{2}$$

In this relation, f_i represent the frequencies in the range (f, 3f, 5f,…,101f), ö$_i$ are the initial phases, A=1, k is a factor chosen so that V_{max}=5 V and V_{min}=-5 V (the measurement range of an analog to digital converter). The shape of the voltage $v_x(t)$, for k=1.71 is depicted in Figure 2. The amplitude spectra of voltage $v_x(t)$ is given in Figure 3.

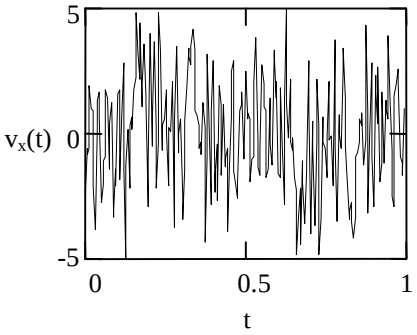

Figure 2. The test voltage $v_x(t)$ for k=1.71 and A=1.

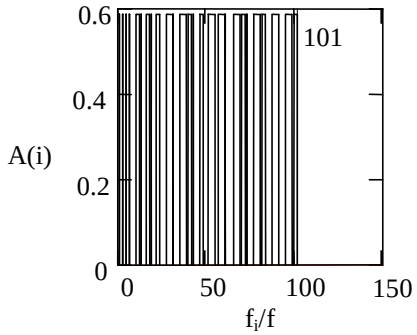

Figure 3. The amplitude spectra of voltage $v_x(t)$.

For every frequency in the spectrum $f_i=\omega_i/2\pi$, the impedance components can be expressed with relation (3).

$$Z(j\omega_i) = R + jX(\omega_i) = R_r \frac{F\{v_u(t)\}}{F\{v_i(t)\}} = Z(\omega_i) e^{j\,j\,(\omega_i)} \tag{3}$$

In this relation, $v_u(t)$ is the voltage across the impedance Z, and $v_i(t)$ is the voltage across the reference resistor.

In order to reduce to maximum the gain and phase errors (which depend on frequency), the gains of the two amplifiers A_u and A_i are chosen to equal 1. In this case, it is used the entire frequency bandwidth of the amplifiers (the bandwidth for unitary gain). In addition, the amplifiers are chosen to be identical, preferable on the same chip. This aspect is especially important when measuring impedances at high frequencies.

The computation of impedance components using relation (3) implies: sampling voltages $v_u(t)$ and $v_i(t)$, the analog to digital conversion of the samples and the computation of amplitude spectra by means of Fourier transform.

Using relation (3) we can determine either the rectangular components of the impedance (R, X(ω_i)) or the components in the polar co-ordinates (Z(ω_i), ö(ω_i)).

2 STUDY OF THE EFFICIENCY OF THE NONLINEAR CONVERSION

2.1 The case of test voltage with optimized crest factor

The measurement of the impedance in a large frequency and magnitude range has as effect a large variation of the ratio between $v_u(t)$ and $v_i(t)$. This situation has as result the increase of the errors for the analog to digital conversion, the increase of the errors in computing the Fourier transform and finally the increase of the errors in computing impedance components. Solutions to reduce the errors in computing the Fourier transform are given in [2]. In the study carried out in [2], it was taken into consideration three types of analog to digital converters: a bipolar linear analog to digital converter (ADC), a bipolar analog to digital converter with logarithmic characteristic (NADC) and a bipolar analog to digital converter with a logarithmic characteristic and with the possibility of working also in linear regime (NLADC). For the ADC, the resolution is constant and equal with N_b bits. For the NADC (the bipolar logarithmic characteristic was linearized using 13 segments, A-law), depending on the measuring range, the resolution is N_b+4, N_b+3, N_b+2, N_b+1, N_b, N_b-1 and N_b-2. For the NLADC (the characteristic in the nonlinear regime is identical to A-law), depending on the measuring range, the resolution is: N_b+4, N_b+3, N_b+2, N_b+1 and N_b (linear regime). All three types of converters have the same conversion time equal to $N_b \cdot T_c$, where T_c is the period of the converters clock.

The possibility of implementing these converters using programmable circuits XC4010 FPGA is indicated in [3].

Consider the voltage x(t) given by relation (4).

$$x(t)=\sum_{i=1}^{i=26}\frac{1}{k\cdot A}\cdot\sin(2p\ f_i+j_i) \tag{4}$$

In this relation, all parameters have the same meaning as in relation (2).

Consider that this voltage was sampled in N points and let N=256. In this case, the ideal value of frequency amplitudes in the spectrum is computed with relation (5).

$$A(i)=\sqrt{\frac{4}{N^2}[(\sum_{n=0}^{n=N-1}x(nt_e)\cos(\frac{2\delta}{N}nf_i))^2+(\sum_{n=0}^{n=N-1}x(nt_e)\sin(\frac{2\delta}{N}nf_i))^2]} \tag{5}$$

In this relation, i=1÷26, t_e is the sampling period (t_e=T/N, T is the period of fundamental f), $x(nt_e)$ is the value of the sample.

For a bipolar N_b bits ADC, the value of the amplitudes is given by relation (6).

$$A_c(i,N_b)=\sqrt{\frac{4}{N^2}[(\sum_{n=0}^{n=N-1}x_e(n,N_b)\cos(\frac{2\delta}{N}nf_i))^2+(\sum_{n=0}^{n=N-1}x_e(n,N_b)\sin(\frac{2\delta}{N}nf_i))^2]} \tag{6}$$

In this relation $x_e(n,N_b)=M(n,N_b)\cdot U_{lsb}(Nb)$, where $U_{lsb}(N_b)=\frac{10}{2^{N_b}}$ is the quantification step and $M(n,N_b)$ is the result of the analog to digital conversion for the sample $x(nt_e)$. The measuring range for the ADC was considered to be ±5´V.

The error of determining the amplitudes is given by relation (7).

$$e(i,N_b)\%=\frac{|A(i)-A_c(i,N_b)|}{A(i)}\cdot 100\% \tag{7}$$

For the NADC and NLADC we can determine similar relations with (6), but in this case the value $x_e(n,N_b)$ will be a multiple of the quantification step corresponding to the resolution with which the sample is measured. For example, for the approximation segment for which the resolution is N_b+4, we have $U_{lsb}=\frac{10}{2^{N_b+4}}$.

We designate by $e_{new}(i,N_b)$ and $e_{newl}(i,N_b)$ the errors obtained when computing amplitudes compared to ideal values A(i), in the case we use the NADC and the NLADC converter respectively.

In Figure 4 are depicted the errors obtained when determining the amplitudes of the fundamental using these three converter types for resolutions N_b equal to 8, 10 and 12 bits.

We can note that the smallest errors are obtained when using an NLADC converter and the greatest ones when using the ADC. It is obvious that the greater the resolution N_b is, the lower the errors are.

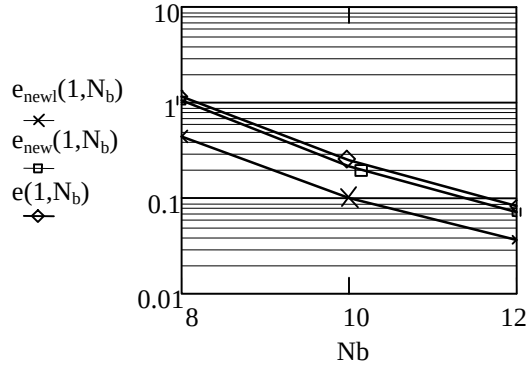

Figure 4. The errors for A=1 and i=1.

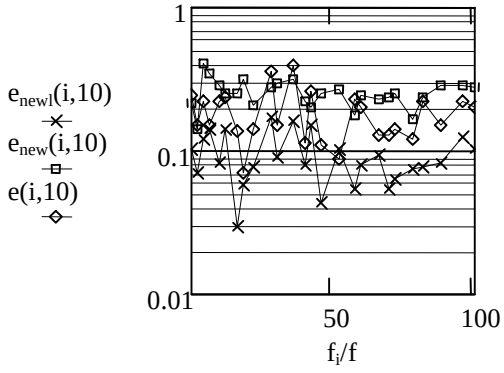

Figure 5. The errors for A=1 and N_b=10.

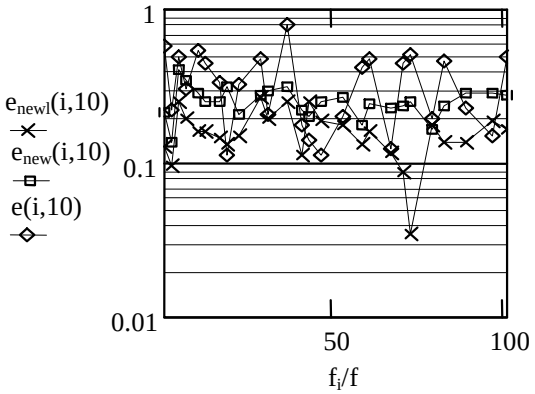

Figure 6. The errors for A=2 and N_b=10.

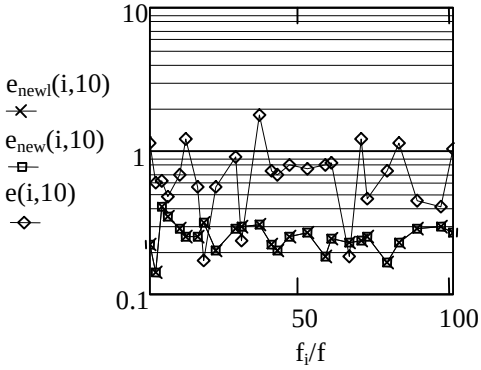

Figure 7. The errors for A=4 and N_b=10.

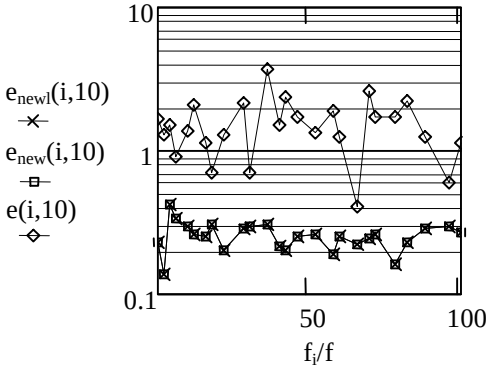

Figure 8. The errors for A=1/8 and N_b=10.

In Figures 5,6,7 and 8 are given the errors when determining the amplitudes for A=1,2,4 and 8 and for N_b=10 bits. From this figures results clearly the superiority of the NADC and NLADC compared to ADC. The NLADC has the lowest errors for all situations. For A>4, the errors in the case of NADC and NLADC are minimum, equal and approximately constant.

We can conclude that using NADC and NLADC we can measure impedance in a large value and frequency range without being necessary to choose different gains for amplifiers A_u and A_i.

2.2 The case of test voltage with non-optimized crest factor

No well-established mathematical methods exists to optimize (reduce) the crest factor of a signal. Thus, we try to study the effect of non-linear conversion applied to a signal with an non-optimized crest factor.

As in the previous case, consider a signal consisting of the fundamental and the 25 odd and prime harmonics but with initial phases equal to 0. This signal is given by relation (8) and is depicted in Figure 9.

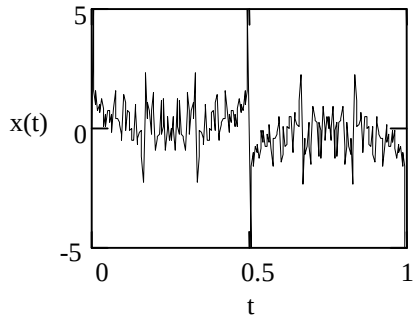

Figure 9. The voltage x(t) for k=3.4 and A=1.

$$x(t) = \sum_{i=1}^{i=26} \frac{1}{k \cdot A} \sin(2p\, f_i\, t) \tag{8}$$

For A=1 and the factor k=3.4, the variation range of the signal is ±5 V.

The crest factor for this voltage is 7.071. The amplitude spectrum is given in Figure 10 (A=1) and the errors obtained when determining the frequency amplitude of the fundamental for the three converter types are depicted in Figure 11. In this case also the errors given by NADC and NLADC are smaller then the errors given by the ADC.

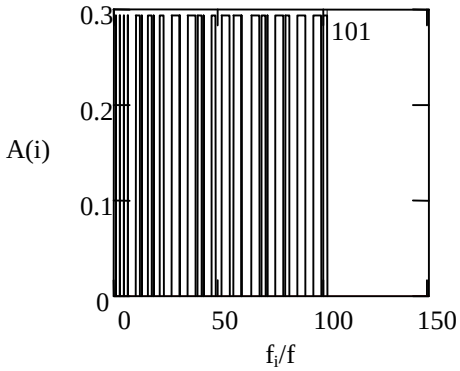

Figure 10. The amplitude spectra of voltage x(t).

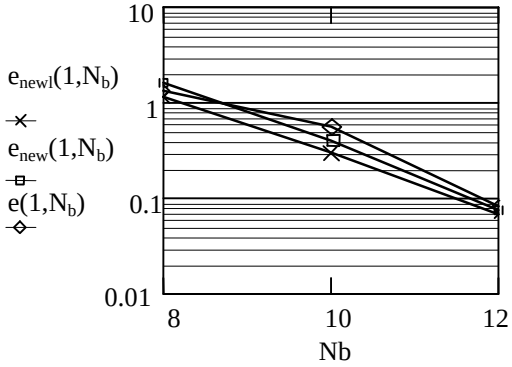

Figure 11. The errors for A=1

In Figures 12,13,14 and 15 are depicted the errors obtained when determining the amplitudes for A=1,2,4 and 8 and for N_b=10 bits. The results indicate the superiority of NADC and NLADC compared to the ADC.

For A>4 the errors given by NADC and NLADC are approximately equal with those that appear in the case of a signal with optimized crest factor.

The resulting conclusion is that from the point of view of the error that arise when computing the amplitude by using the NADC and the NLADC converters, the problem of minimizing the crest factor appears to be non-essential.

3 CONCLUSIONS

The use of non-linear (logarithmic) analog to digital conversion has as effect the reduction of the conversion errors for low levels of the measured signal. This aspect becomes so much important as the low levels are preponderant in the signal. This is the case of a test signal with non-optimized and even optimized crest factor.

For lower amplitudes (A>4), the differences that appear when processing the two signal types with converters NADC and NLADC are insignificant.

Keeping the same conversion time, the errors that appear at the analog to digital conversion, the computation of amplitudes and finally the computation of the impedance components are smaller when using NADC and NLADC converters compared to ADC converter. Therefore, the non-linear conversion (logarithmic) give better results when measuring impedances and it is an alternative to the problem of minimizing the crest factor of a multi-frequency signal.

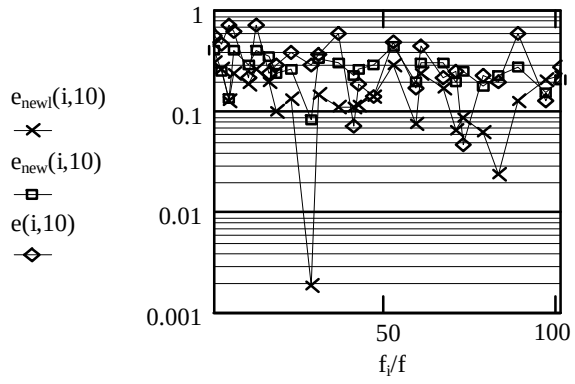

Figure 12. The errors for A=1 and N_b=10.

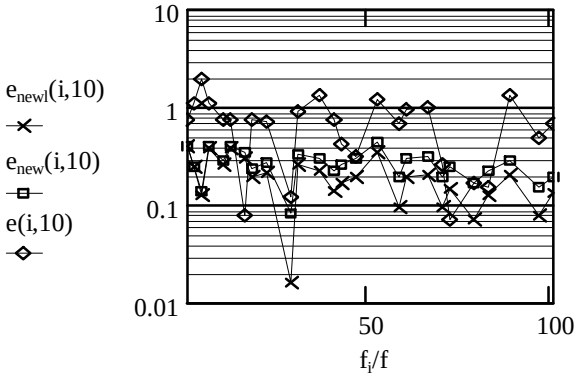

Figure 13. The errors for A=2 and N_b=10.

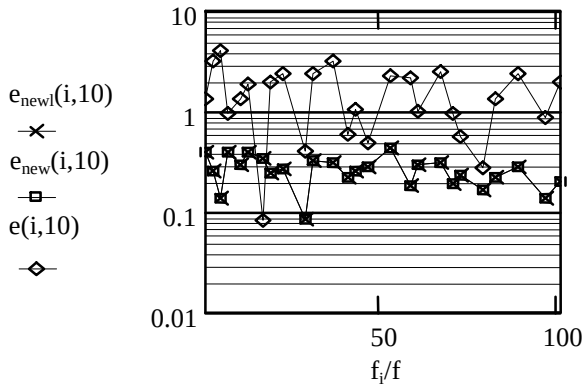

Figure 14. The errors for A=4 and N_b=10.

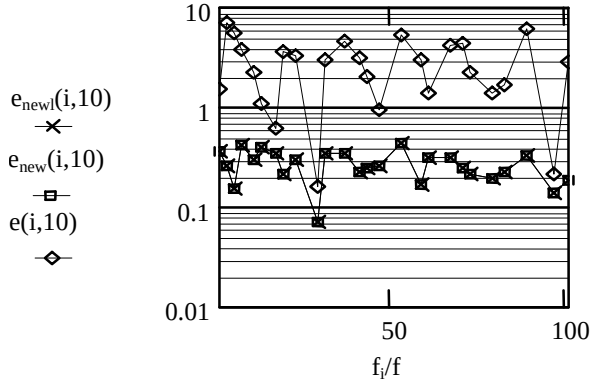

Figure 15. The errors for A=8 and N_b=10.

REFERENCES

[1] W. A. Evans, T. Ingersoll, Design of a Virtual LCR Component Meter, *IEE Proc.-Sci. Meas. Technol.*, **142** (2) (1995) 114 – 124.
[2] L. Breniuc, E. Cretu and C. G. Haba, A Study on the Efficiency of Nonlinear Conversion Used in the Fourier Transformate Computation, *Bul. Inst. Polit. Iasi*, t. XL(IL) f.5 s.III (1999) 210 – 214.
[3] L. Breniuc, C. G. Haba and C. Sarmasanu, The Possibility of Implementing a Nonlinear Successive Approximation A/D Converter Using FPGAs, *Proceedings of the "5th Workshop on ADC Modeling and Testing"*, (Viena, 26-28 September, 2000), Hofburg- Wien, Austria, 2000, in press.

AUTHORS: Assoc. Prof. Dr. L. BRENIUC, Prof. Dr. Mihai CRETU, Lecturer Dr. Lucian NITA, Department for Electrical Measurements, TU "Gh. Asachi", Iasi, Bd. D. Mangeron Nr. 53, RO-6600 Iasi, Romania, Phone: ++40 32 130718, Fax: ++40 32 130054, E-mail: lbreniuc@ee.tuiasi.ro.